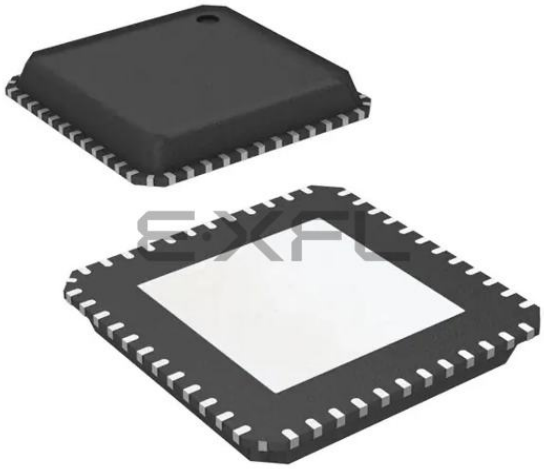

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Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9869qxa20xuma1

2 Block Diagram

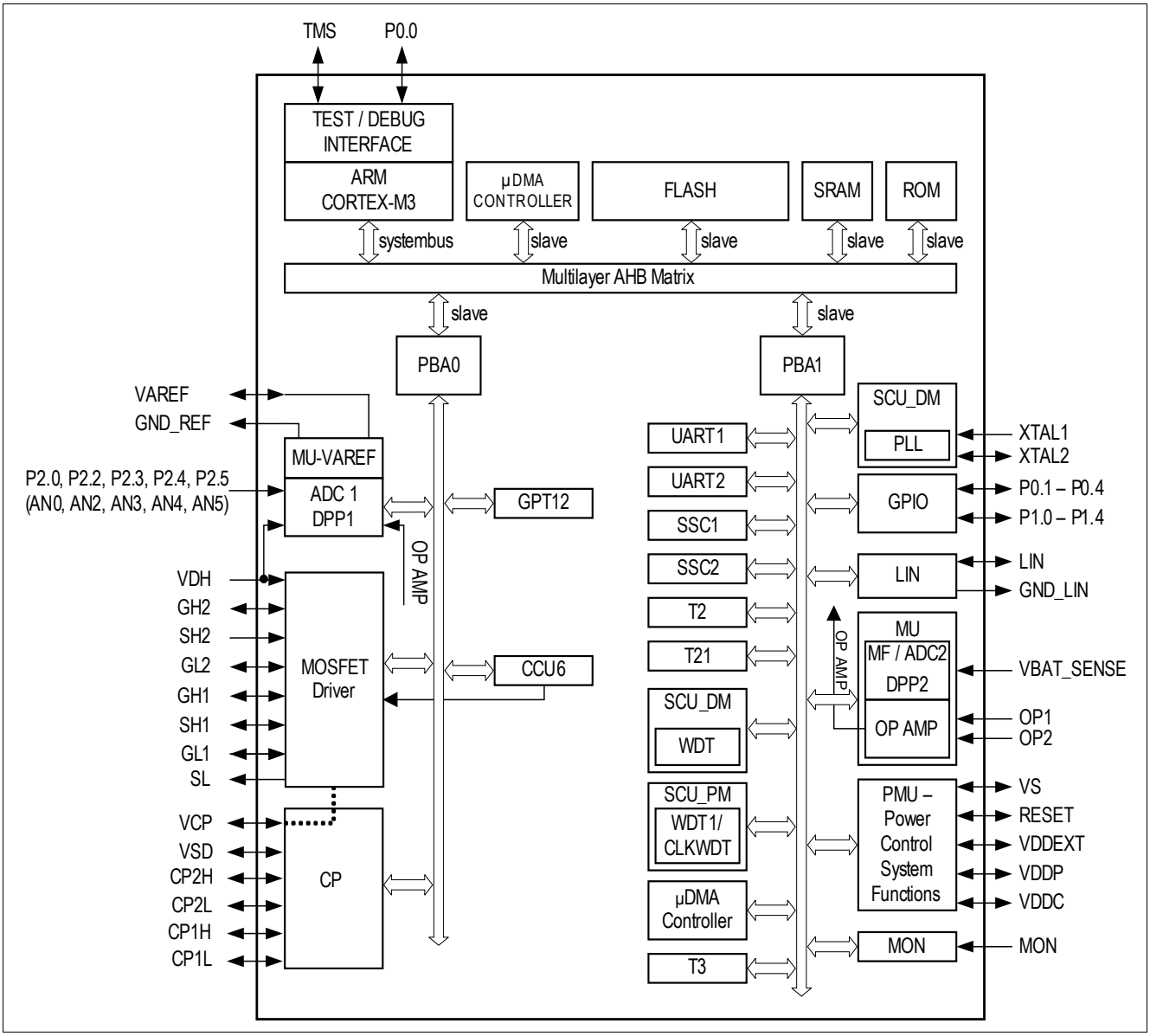

Figure 1 Block Diagram

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
SH1	8	P	–	Source High Side FET 1
GH1	9	P	–	Gate High Side FET 1
SL	10	P	–	Source Low Side FET
GL2	12	P	–	Gate Low Side FET 2
GL1	13	P	–	Gate Low Side FET 1
Others				
GND_REF	33	P	–	GND for VAREF
VAREF	34	I/O	–	5V ADC1 reference voltage, optional buffer or input
OP1	37	I	–	Negative operational amplifier input
OP2	36	I	–	Positive operational amplifier input
TMS	20	I I/O	I/PD	TMS Test Mode Select input SWD Serial Wire Debug input/output
RESET	22	I/O	–	Reset input, not available during Sleep Mode
VBAT_SENSE	46	I	–	Battery supply voltage sense input
EP	–	–	–	Exposed Pad, connect to GND

1) Only valid for digital IOs
2) Also named VDD5V.
3) Also named VDD1V5.

6.2.1 Block Diagram

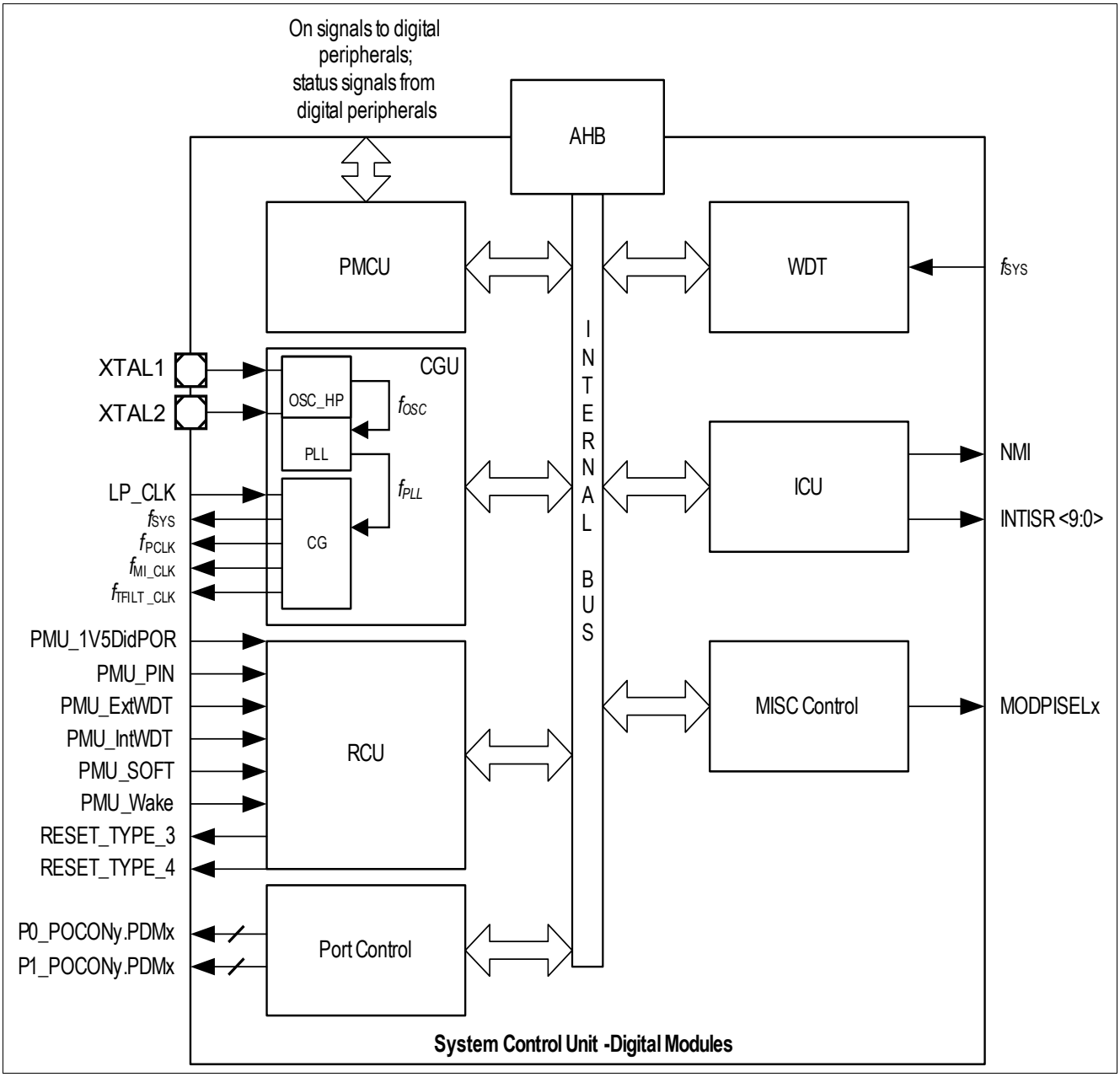

Figure 8 System Control Unit - Digital Modules Block Diagram

AHB (Advanced High-Performance Bus)

PMCU (Power Module Control Unit)

WDT (Watchdog Timer in SCU-DM)

- f_{SYS} System clock

CGU (Clock Generation Unit)

- f_{SYS} System clock
- f_{PCLK} Peripheral clock

- f_{MI_CLK} Measurement interface clock
- f_{TFILT_CLK} Analog module filter clock
- LP_CLK Clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- NMI (Non-Maskable Interrupt)
- INTISR<15,13:4,1,0> External interrupt signals

RCU (Reset Control Unit)

- PMU_1V5DidPOR Undervoltage reset of power down supply
- PMU_PIN Reset generated by reset pin
- PMU_ExtWDT WDT1 reset
- PMU_IntWDT WDT (SCU) reset
- PMU_SOFT Software reset
- PMU_Wake Sleep Mode/Stop Mode exit with reset
- RESET_TYPE_3 Peripheral reset (contains all resets)
- RESET_TYPE_4 Peripheral reset (without SOFT and WDT reset)

Port Control

- P0_POCONy.PDMx driver strength control
- P1_POCONy.PDMx driver strength control

MISC Control

- MODPISELx Mode selection registers for UART (source section) and Timer (trigger or count selection)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) enables a flexible clock generation for TLE9869QXA20. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9869QXA20 consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module with an internal oscillator (OSC_PLL), and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

WDT1 (System Watchdog)

- LP_CLK clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI supply prewarning NMI request
- PREWARN_SUP_INT supply prewarning interrupt
- grouping of peripheral interrupts for external interupt nodes:
  - grouping single peripheral interrupts for interrupt node INT<2> (Measurement Unit (MU))
  - grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - grouping single peripheral interrupts for interrupt node INT<10> (UART1-LIN Transceiver)
  - grouping single peripheral interrupts for interrupt node INT<14> (Bridge Driver)

14.3 TLE9869QXA20 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	LIN_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / LIN_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

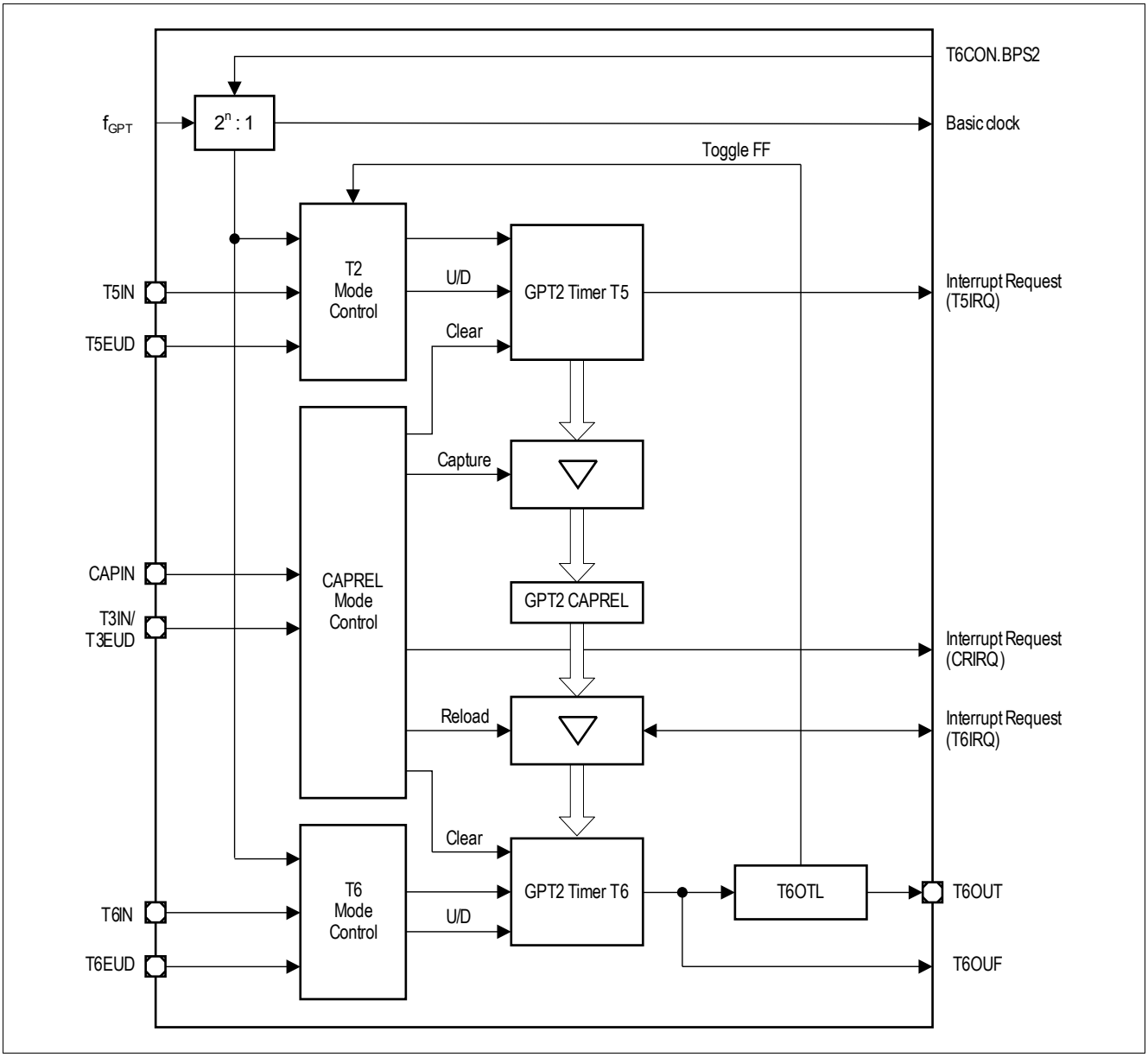

Figure 20 GPT2 Block Diagram (n = 1 … 4)

20 LIN Transceiver

20.1 Features

General Functional Features

- Compliant to LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (slew rate, receiver hysteresis)

Special Features

- Measurement of LIN master baudrate via Timer 2
- LIN can be used as input/output with SFR bits.
- TxD timeout feature (optional, on by default)

Operation Mode Features

- LIN Sleep Mode (LSLM)
- LIN Receive-Only Mode (LROM)
- LIN Normal Mode (LNM)
- High Voltage Input / Output Mode (LHVIO)

Supported Baud Rates

- Mode for a transmission up to 10.4 kBaud
- Mode for a transmission up to 20 kBaud
- Mode for a transmission up to 40 kBaud
- Mode for a transmission up to 115.2 kBaud

Slope Mode Features

- Normal Slope Mode (20 kbit/s)
- Low Slope Mode (10.4 kbit/s)
- Flash Mode (115.2 kbit/s)

Wake-Up Features

- LIN bus wake-up

21.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on TXD and RXD lines, which are normally connected to the MTSR (MasterTransmit/Slave Receive) and MRST (Master Receive/Slave Transmit) pins. The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

21.2.1 Block Diagram

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

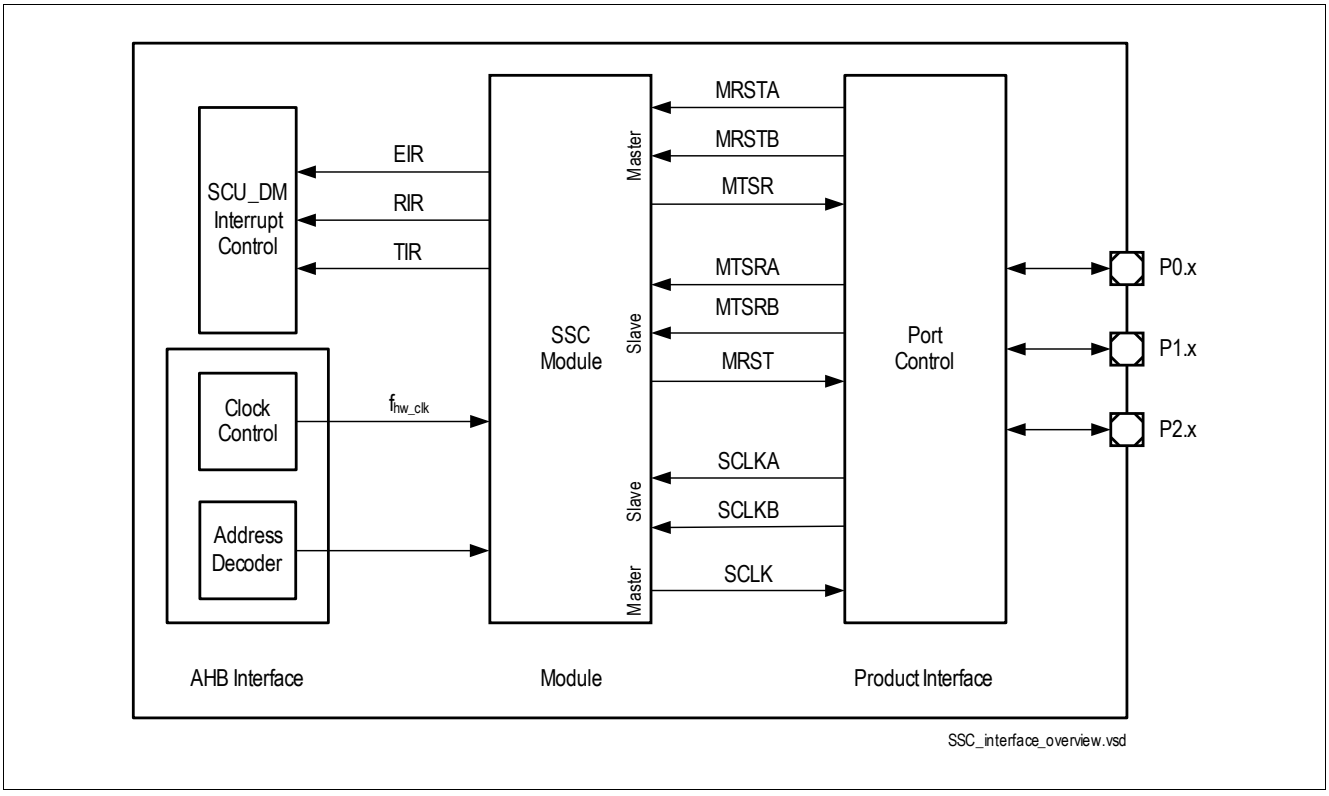

Figure 24 SSC Interface Diagram

22 Measurement Unit

22.1 Features

- 1 x 8-bit ADC with 10 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VBAT_SENSE**, **VS**, **VDDP** and **VDDC**.
- VBG monitoring of 8-bit ADC to guarantee functional safety requirements.
- Bridge Driver Diagnosis Measurement (VDH, VCP).
- Temperature Sensor for monitoring the chip temperature and PMU Regulator temperature.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

22.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 14 Measurement Functions and Associated Modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
8-bit ADC (ADC2)	8-bit ADC module with 10 multiplexed inputs, including HV input attenuator	5 high voltage full supply range capable inputs (2.5V...30,7V(FS)) 2 medium voltage inputs (0..5V/7V FS). 3 low voltage inputs (0..1.2V/1.6V FS) (allocation see following overview figure)
10-bit ADC (ADC1)	10-bit ADC module with 8 multiplexed inputs	Five (5V) analog inputs from Port 2.x
VDH Input Voltage Attenuator	VDH input voltage attenuator	Scales down V(VDH) to the input voltage range of ADC1.CH6
Temperature Sensor	Temperature sensor with two multiplexed sensing elements: • PMU located sensor • Central chip located sensor	Generates output voltage which is a linear function of the local chip (junction) temperature.
Measurement Core Module	Digital signal processing and ADC2 control unit	1. Generates the control signal for the 8-bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

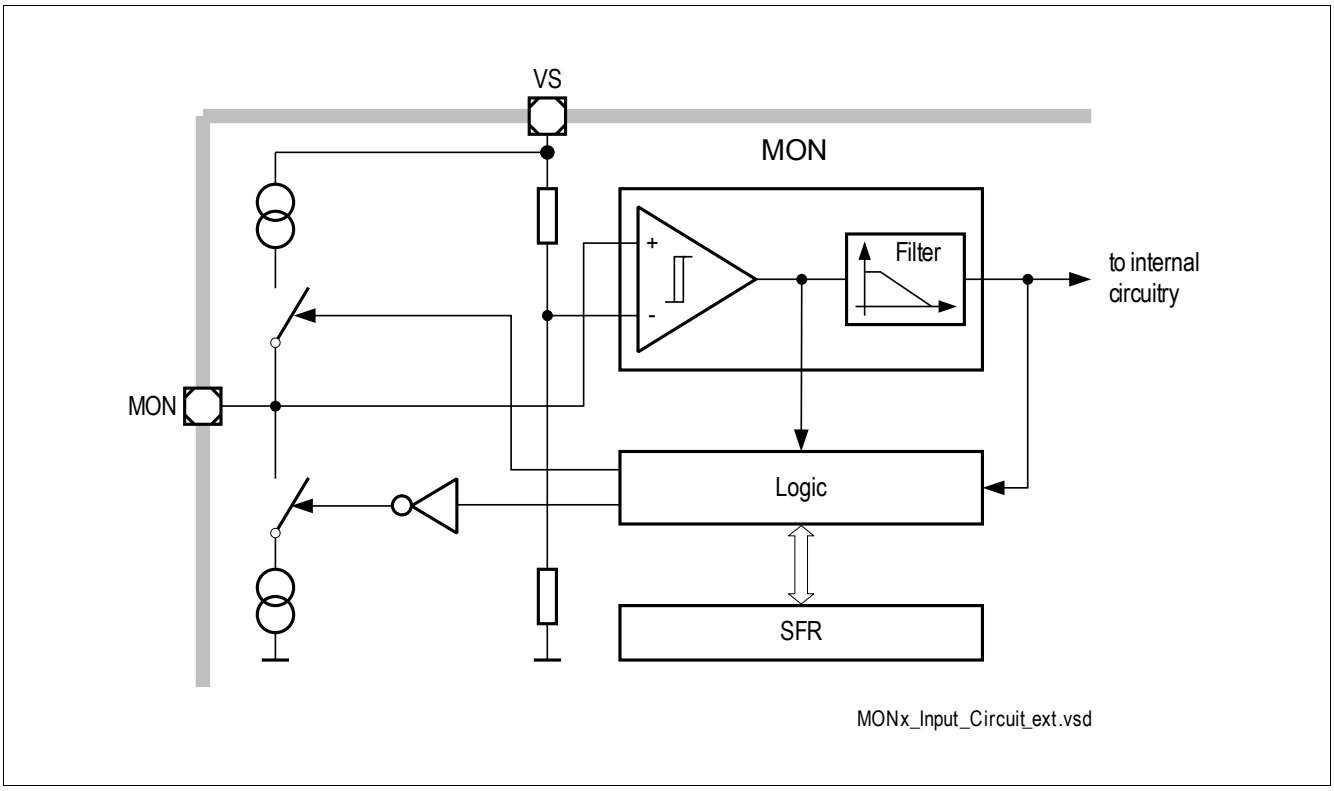

Figure 28 Monitoring Input Block Diagram

27 Current Sense Amplifier

27.1 Features

Main Features

- Programmable gain settings: G = 10, 20, 40, 60
- Differential input voltage: ± 1.5V / G
- Wide common mode input range ± 2 V
- Low setting time < 1.4 µs

27.2 Introduction

The current sense amplifier in **Figure 30** can be used to measure near ground differential voltages via the 10-bit ADC. Its gain is digitally programmable through internal control registers.

Linear calibration has to be applied to achieve high gain accuracy, e.g. end-of-line calibration including the shunt resistor.

Figure 30 shows how the current sense amplifier can be used as a low-side current sense amplifier where the motor current is converted to a voltage by means of a shunt resistor R_{SH}. A differential amplifier input is used in order to eliminate measurement errors due to voltage drop across the stray resistance R_{Stray} and differences between the external and internal ground. If the voltage at one or both inputs is out of the operating range, the input circuit is overloaded and requires a certain specified **recovery time**.

In general, the external low pass filter should provide suppression of EMI.

27.2.1 Block Diagram

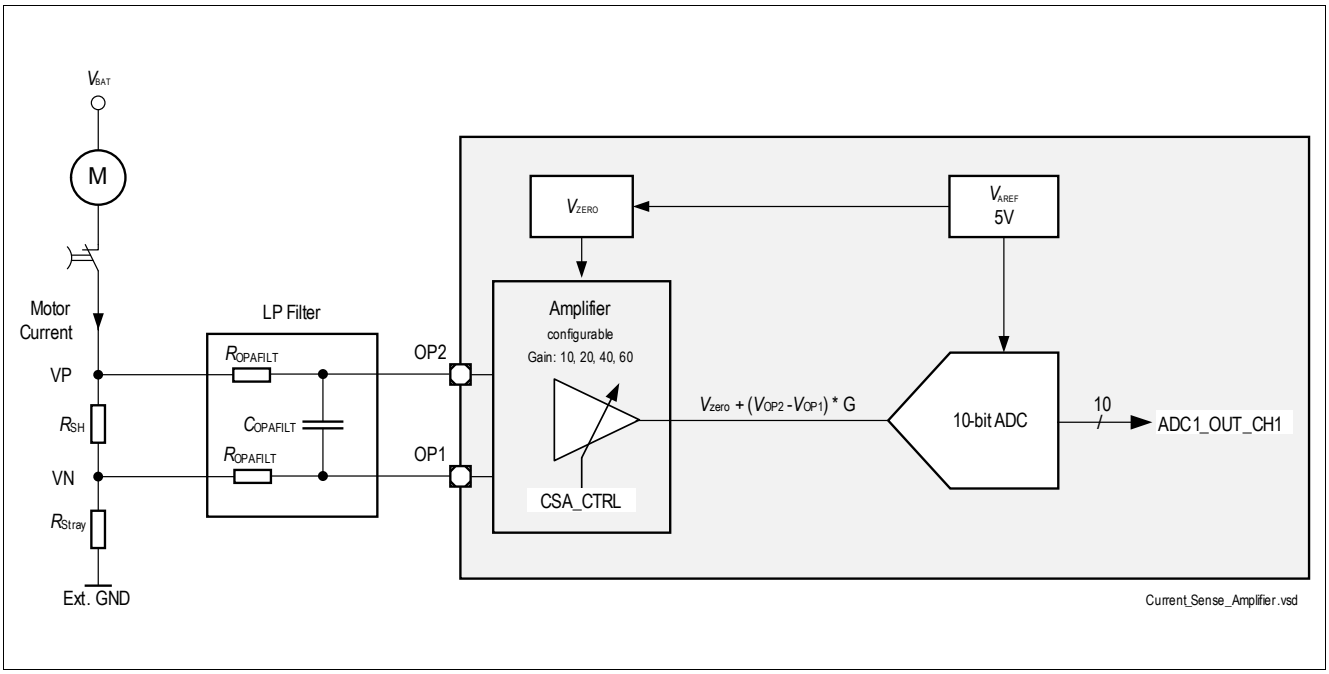

Figure 30 Simplified Application Diagram

29 Electrical Characteristics

This chapter includes all relevant electrical characteristics of the product TLE9869QXA20.

29.1 General Characteristics

29.1.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages – Supply Pins							
Supply voltage – VS	V_S	-0.3	–	40	V	Load dump	P_1.1.1
Supply voltage – VSD	V_{SD}	-0.3	–	48	V	–	P_1.1.2
Supply voltage – VSD	$V_{SD\_max\_extend}$	-2.8	–	48	V	Series resistor R_{VSD} = 2.2 Ω, t = 8 ms [2)]	P_1.1.32
Voltage range – VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_1.1.3
Voltage range – VDDP	$V_{DDP\_max\_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≥ 1V/µs; duration: t ≤ 150µs; C_{VDDP} ≤ 570 nF	P_1.1.41
Voltage range – VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_1.1.4
Voltage range – VDDEXT	$V_{DDEXT\_max\_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≥ 1V/µs; duration: t ≤ 150µs; C_{VDDEXT} ≤ 570 nF	P_1.1.42
Voltage range – VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_1.1.5
Voltages – High Voltage Pins							
Battery voltage VBAT_SENSE	V_{BAT_SENSE}	-28	–	40	V	[3)]	P_1.1.6
Input voltage at LIN	V_{LIN}	-28	–	40	V	–	P_1.1.7
Input voltage at MON	$V_{MON\_maxrate}$	-28	–	40	V	[4)]	P_1.1.8
Input voltage at VDH	$V_{VDH\_maxrate}$	-2.8	–	40	V	[5)]	P_1.1.38
Voltage range at GHx	V_{GH}	-8.0	–	48	V	[6)]	P_1.1.9
Voltage range at GHx vs. SHx	V_{GHvsSH}	14	–	–	V	–	P_1.1.44
Voltage range at SHx	V_{SH}	-8.0	–	48	V	–	P_1.1.11
Voltage range at GLx	V_{GL}	-8.0	–	48	V	[7)]–	P_1.1.13
Voltage range at GLx vs. SL	V_{GLvsSL}	14	–	–	V	–	P_1.1.45

29.2.3 VDDEXT Voltage Regulator (5.0V) Parameters

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDEXT}	0	–	20	mA	–	P_2.3.1
Specified output current	I_{VDDEXT}	0	–	40	mA	1)	P_2.3.21
Required decoupling capacitance	$C_{VDDEXT1}$	0.1	–	2.2	µF	3) 2)ESR < 1 Ω; the specified capacitor value is a typical value.	P_2.3.22
Required buffer capacitance for stability (load jumps)	$C_{VDDEXT2}$	1	–	2.2	µF	3)2)the specified capacitor value is a typical value.	P_2.3.20
Output voltage including line and load regulation	V_{DDEXT}	4.9	5.0	5.1	V	3) I_{load}<20mA; V_S > 5.5V	P_2.3.3
Output voltage including line and load regulation	V_{DDEXT}	4.8	5.0	5.2	V	I_{load}<40mA; V_S > 5.5V	P_2.3.23
Output drop @ Active Mode	V_S-V_{DDEXT}		50	+300	mV	3) I_{load} < 20mA; 3V < V_S < 5.0V	P_2.3.4
Output drop @ Active Mode	V_S-V_{DDEXT}		–	+400	mV	I_{load} < 40mA; 3V < V_S < 5.0V	P_2.3.14
Load regulation @ Active Mode	$V_{DDEXTLOR}$	-50	–	50	mV	2 ... 40mA; C =200nF	P_2.3.5
Line regulation @ Active Mode	$V_{VDDEXTLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.3.6
Power supply ripple rejection @ Active Mode	$P_{SSRVDDEXT}$	50	–	–	dB	3) V_S = 13.5V; f =0 ... 1KHz; Vr=2Vpp	P_2.3.7
Overvoltage detection	$V_{VDDEXTOV}$	5.18	–	5.4	V	V_S > 5.5V	P_2.3.8
Overvoltage detection filter time	$t_{FILT\_VDDEXTOV}$	–	735	–	µs	3)4)	P_2.3.24
Voltage OK detection range	$V_{VDDEXTOK}$	–	3	–	V	3)	P_2.3.25
Voltage stable detection range[5)]	$\Delta V_{VDDEXTSTB}$	- 220	–	+ 220	mV	3)	P_2.3.26
Undervoltage trigger	$V_{VDDEXTUV}$	2.6	2.8	3.0	V	6)	P_2.3.9
Overcurrent diagnostic	$I_{VDDEXTOC}$	50	–	160	mA	–	P_2.3.10
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	3)4)	P_2.3.27
Overcurrent diagnostic shutdown time	$t_{FILT\_VDDCOC\_SD}$	–	290	–	µs	3)4)	P_2.3.28

1) This use case requires the reduced utilization of VDDP output current by 20 mA, see P_2.1.22.
2) Ceramic capacitor.
3) Not subject to production test, specified by design.
4) This filter time and its variation is derived from the time base t_{LP_CLK} = 1 / f_{LP_CLK}.

5) The absolute voltage value is the sum of parameters V_{DDEXT} + $\Delta V_{DDEXTSTB}$.
6) When the condition is met, the Bit VDDEXT_CTRL.bit.SHORT will be set.

29.4 Flash Memory

This chapter includes the parameters for the 128 kByte embedded flash module.

29.4.1 Flash Parameters

Table 29 Flash Characteristics[1)]

V_S = 3.0 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.9
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[4)]Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.6

1) Not subject for production test, specified by design.

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.

3) Derived by extrapolation of lifetime tests.

4) T_j = 25 °C.

5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty2}	–	–	0.581		[4] duty cycle 2 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.2 (Par. 28)	P_6.1.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.23
Duty cycle D3 (for worst case at 10.4 kbit/s)	t_{duty1}	0.417	–	–		[4] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.2 (Par. 29)	P_6.1.24
Duty cycle D4 (for worst case at 10.4 kbit/s)	t_{duty2}	–	–	0.590		[4] duty cycle 4 TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.2 (Par. 30)	P_6.1.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.27
Receiver delay symmetry	$t_{sym,R}$	-1.5	–	1.5	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_6.1.28
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.31

29.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 40 A/D Converter Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	24	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	1)4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	1)	P_9.2.6
Wakeup time from analog powerdown, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wakeup time from analog powerdown, slow mode	t_{WAS}	–	–	15	µs	1)5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	-2	±1	+2	counts	6)7)Reference is internal V_{AREF}	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	-12	±6	+12	counts	7)8)Reference is internal V_{AREF}	P_9.2.22
DNL error	EA_{DNL}	-3	±0.8	+3	counts	–	P_9.2.10
INL error	$EA_{INL\_int\_VAREF}$	-5	±0.8	+5	counts	Reference is internal V_{AREF}	P_9.2.11
Gain error	$EA_{GAIN\_int\_VAREF}$	-10	±0.4	+10	counts	Reference is internal V_{AREF}	P_9.2.12
Offset error	EA_{OFF}	-2	±0.5	+2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	1)5)9)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	1)5)9)	P_9.2.15
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	1)5)9)	P_9.2.16

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
High level output voltage GLx vs. GND	V_{Gxx6}	8	–	–	V	V_{SD} = 6.4 V[1], C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.6
High level output voltage GLx vs. GND	V_{Gxx7}	7	–	–	V	V_{SD} = 5.4 V, C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.7
Rise time	t_{rise3_3nf}	–	200	–	ns	[1]CLoad = 3.3 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.8
Fall time	t_{fall3_3nf}	–	200	–	ns	[1]C_{Load} = 3.3 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.9
Rise time	$t_{risemax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.57
Fall time	$t_{fallmax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.58
Rise time	$t_{risemin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.14
Fall time	$t_{fallmin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.15
Absolute rise - fall time difference for all LSx	$t_{r\_f(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.35
Absolute rise - fall time difference for all HSx	$t_{r\_f(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.36
Resistor between GHx/GLx and GND	R_{GGND}	30	40	50	kΩ	[1]–	P_12.1.11

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resistor between SHx and GND	R_{SHGN}	30	40	50	kΩ	1)3) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0,6V typ. before it is discharged through the resistor.	P_12.1.10
Low RDSON mode (boosted discharge mode)	R_{ONCCP}	–	9	12	Ω	V_{VSD} = 13.5 V, V_{VCP} = V_{VSD} + 14.0 V; I_{CHARGE} = I_{DISCHG} = 31(max); 50mA forced into Gx, Sx grounded	P_12.1.50
Resistance between VDH and VSD	I_{BSH}	–	4	–	kΩ	1)	P_12.1.24
Input propagation time (LS on)	$t_{P(ILN)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, I_{Charge} =3(min), 25% of V_{Gxx1}	P_12.1.37
Input propagation time (LS off)	$t_{P(ILF)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, $I_{Discharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.38
Input propagation time (HS on)	$t_{P(IHN)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, I_{Charge} =3(min) 25% of V_{Gxx1}	P_12.1.39
Input propagation time (HS off)	$t_{P(IHF)min}$	–	1.5	3	µs	1)C_{Load} = 10 nF, $I_{Disharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.40
Input propagation time (LS on)	$t_{P(ILN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.26
Input propagation time (LS off)	$t_{P(ILF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.27
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.29