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Details

Product Status	Active
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2263m56f66labhxuma1

Summary of Features

Table 2 Synopsis of XC226xM Special Device Types (cont'd)

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules	ADC⁴⁾ Chan.	Interfaces⁴⁾
XC2264M-72FxxL	576 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1	8	2 CAN Nodes, 4 Serial Chan.
XC2264M-56FxxL	448 Kbytes	16/8 Kbytes 16 Kbytes	CC2 CCU60/1	8	2 CAN Nodes, 4 Serial Chan.
XC2263M-104FxxL	832 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.
XC2263M-72FxxL	576 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.
XC2263M-56FxxL	448 Kbytes	16/8 Kbytes 16 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in [Table 3](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in [Table 5](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
24	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input
28	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	CCU63_T12 HRB	I	In/A	External Run Control Input for T12 of CCU63
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
29	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
30	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1/2/3
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1/2/3
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
31	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC6 2	O2	St/B	CCU60 Channel 2 Output
	U3C0_SELO 1	O3	St/B	USIC3 Channel 0 Select/Control 1 Output
	AD2	OH / IH	St/B	External Bus Interface Address/Data Line 2
	CCU60_CC6 2INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
	U3C0_DX2B	I	St/B	USIC3 Channel 0 Shift Control Input
63	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO 0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO 1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COU T61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
	ESR2_8	I	St/B	ESR2 Trigger Input 8
65	P2.13	O0 / I	St/B	Bit 13 of Port 2, General Purpose Input/Output
	U2C1_SELO 2	O1	St/B	USIC2 Channel 1 Select/Control 2 Output
	RxDC2D	I	St/B	CAN Node 2 Receive Data Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO 3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	A23	OH	St/B	External Bus Interface Address Line 23
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input
	U3C1_DX0A	I	St/B	USIC3 Channel 1 Shift Data Input
67	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COU T60	O2	St/B	CCU60 Channel 0 Output
	AD3	OH / IH	St/B	External Bus Interface Address/Data Line 3
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
	U3C0_DX0A	I	St/B	USIC3 Channel 0 Shift Data Input
68	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output
	U1C1_SCLK OUT	O1	St/B	USIC1 Channel 1 Shift Clock Output
	U1C0_SELO 2	O2	St/B	USIC1 Channel 0 Select/Control 2 Output
	CCU61_COU T62	O3	St/B	CCU61 Channel 2 Output
	A5	OH	St/B	External Bus Interface Address Line 5
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input
	RXDC3E	I	St/B	CAN Node 3 Receive Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	CCU62_COU T61	O1	St/B	CCU62 Channel 1 Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
	RxDC5A	I	St/B	CAN Node 5 Receive Data Input
91	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input
92	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output
	CCU62_COU T60	O1	St/B	CCU62 Channel 0 Output
	U1C1_SELO 3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output
	$\overline{\text{BRKOUT}}$	O3	St/B	OCDS Break Signal Output
	A13	OH	St/B	External Bus Interface Address Line 13
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input

Functional Description

Table 8 XC226xM Memory Map (cont'd)¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
Data SRAM	00'A000 _H	00'DFFF _H	16 Kbytes	–
Reserved for DSRAM	00'8000 _H	00'9FFF _H	8 Kbytes	–
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	–

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed byte-wise or word-wise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LxBus (MultiCAN and the USIC modules). The LxBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections¹⁾:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes ... 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{\text{CS}}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.

Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

¹⁾ Bus modes are switched dynamically if several address windows with different mode settings are used.

3.8 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range or variation for the timer period and resolution and allows precise adjustments to the application-specific requirements. In addition, an external count input allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.

All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 9 Compare Modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible

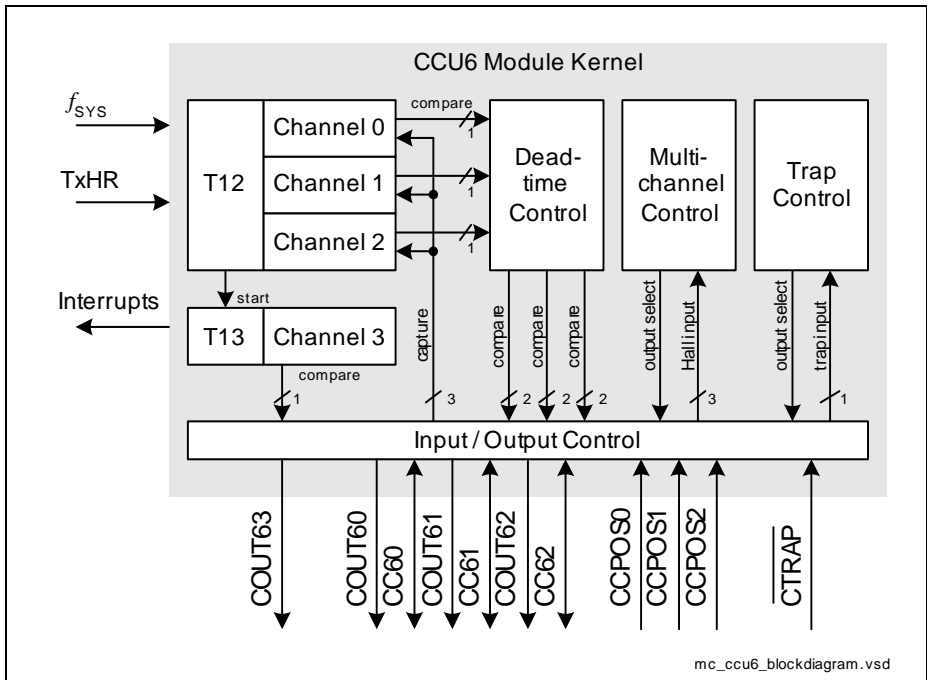


Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.18 Parallel Ports

The XC226xM provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in [Table 10](#).

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 10 Summary of the XC226xM's Ports

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7...A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15...A8), CCU6, USIC
P2	14	I/O	EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P4	4	I/O	EBC ($\overline{\text{CS3}}$... $\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC
P5	11	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	3	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P10	16	I/O	EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN
P15	5	I	Analog Inputs, GPT12E

3.20 Instruction Set Summary

Table 11 lists the instructions of the XC226xM.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 11 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Functional Description

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

- 1) The Enter Power Down Mode instruction is not used in the XC226xM, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

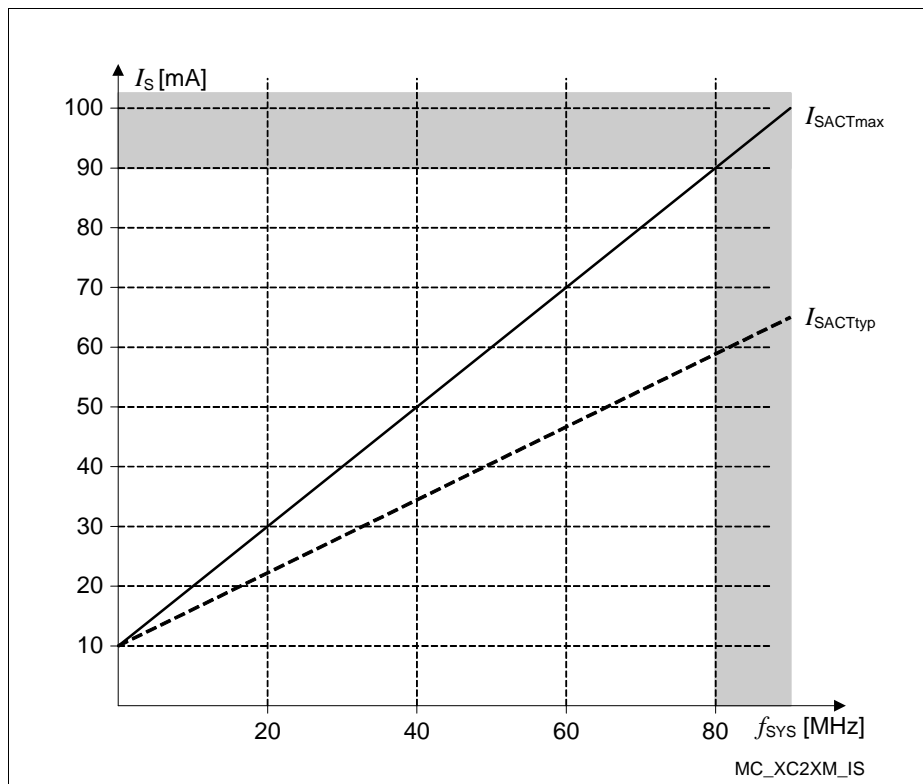


Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

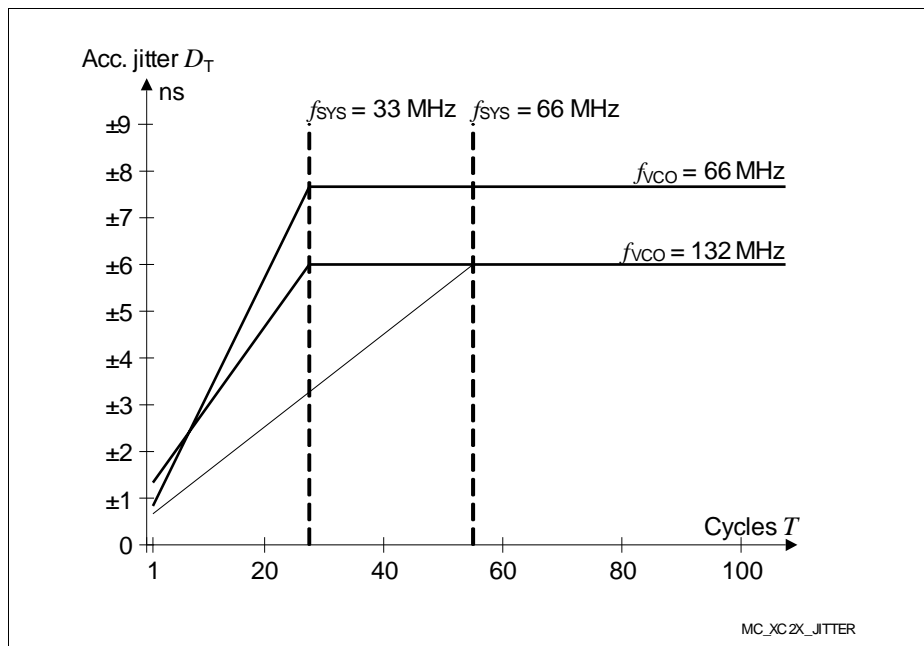


Figure 20 **Approximated Accumulated PLL Jitter**

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$.

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of $V_{PP} = 50 \text{ mV}$. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

4.6.4 Pad Properties

The output pad drivers of the XC226xM can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP} . The following table lists the pad parameters.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

4.6.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; $C_L = 20$ pF.

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{SYS} - 8^{1)}$	—	—	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{SYS} - 6^{1)}$	—	—	ns	
Data output DOUT valid time	t_3 CC	-6	—	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	—	—	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 33 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{SYS} - 10^{1)}$	—	—	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{SYS} - 9^{1)}$	—	—	ns	
Data output DOUT valid time	t_3 CC	-7	—	11	ns	

Table 35 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	7	—	—	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	7	—	—	ns	
Receive data input setup time to shift clock receive edge ¹⁾	t_{12} SR	7	—	—	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	5	—	—	ns	
Data output DOUT valid time	t_{14} CC	8	—	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

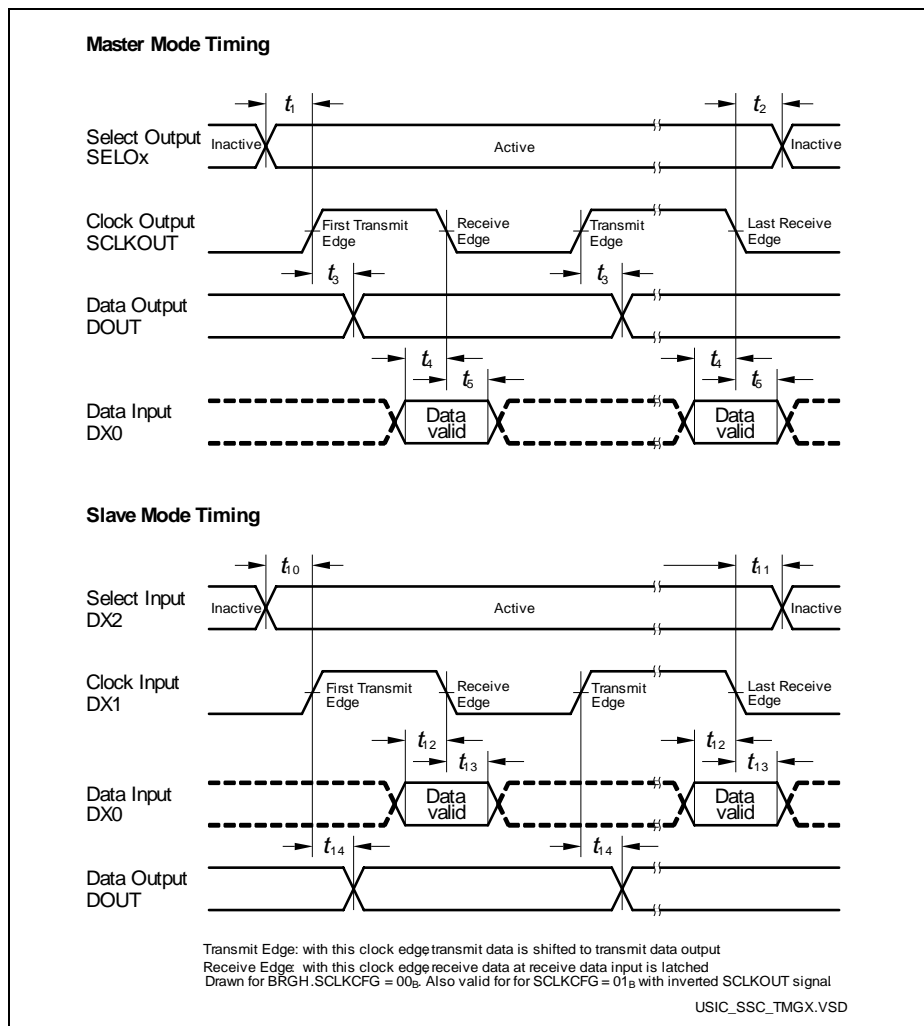


Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; $C_L = 20$ pF.

Table 38 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50 ¹⁾	—	—	ns	2)
TCK high time	t_2 SR	16	—	—	ns	
TCK low time	t_3 SR	16	—	—	ns	
TCK clock rise time	t_4 SR	—	—	8	ns	
TCK clock fall time	t_5 SR	—	—	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ³⁾	t_8 CC	—	25	29	ns	
TDO high impedance to valid output from TCK falling edge ⁴⁾³⁾	t_9 CC	—	25	29	ns	
TDO valid output to high impedance from TCK falling edge ³⁾	t_{10} CC	—	25	29	ns	
TDO hold after TCK falling edge ³⁾	t_{18} CC	5	—	—	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{\text{SYS}}$.

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.