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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2265m56f66laahxuma1

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General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TXDC4	O2	St/B	CAN Node 4 Transmit Data Output
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	U3C0_SCLK OUT	O1	St/B	USIC3 Channel 0 Shift Clock Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_CC26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output
	T2INA	I	St/B	GPT12E Timer T2 Count/Gate Input
	CCU62_CCP OS1B	I	St/B	CCU62 Position Input 1
48	U3C0_DX1B	I	St/B	USIC3 Channel 0 Shift Clock Input
	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO 0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO 1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
49	ESR2_6	I	St/B	ESR2 Trigger Input 6
	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CC2_CC27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	CS3	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUDA	I	St/B	GPT12E Timer T2 External Up/Down Control Input
49	CCU62_CCP OS2B	I	St/B	CCU62 Position Input 2

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
69	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	U3C0_DOUT	O3	St/B	USIC3 Channel 0 Shift Data Output
	AD4	OH / IH	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLKOUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COUT62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	AD5	OH / IH	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COUT63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U1C0_SELO0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / IH	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input
73	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD7	OH / IH	St/B	External Bus Interface Address/Data Line 7
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCP OS0A	I	St/B	CCU60 Position Input 0
	RxDC4C	I	St/B	CAN Node 4 Receive Data Input
	T4INB	I	St/B	GPT12E Timer T4 Count/Gate Input
74	P0.7	O0 / I	St/B	Bit 7 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	U1C0_SELO3	O2	St/B	USIC1 Channel 0 Select/Control 3 Output
	TxDC3	O3	St/B	CAN Node 3 Transmit Data Output
	A7	OH	St/B	External Bus Interface Address Line 7
	U1C1_DX0B	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTR APB	I	St/B	CCU61 Emergency Trap Input

Functional Description

Table 8 XC226xM Memory Map (cont'd)¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
Data SRAM	00'A000 _H	00'DFFF _H	16 Kbytes	–
Reserved for DSRAM	00'8000 _H	00'9FFF _H	8 Kbytes	–
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	–

- 1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.
- 2) The areas marked with "<" are slightly smaller than indicated. See column "Notes".
- 3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).
- 4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed byte-wise or word-wise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

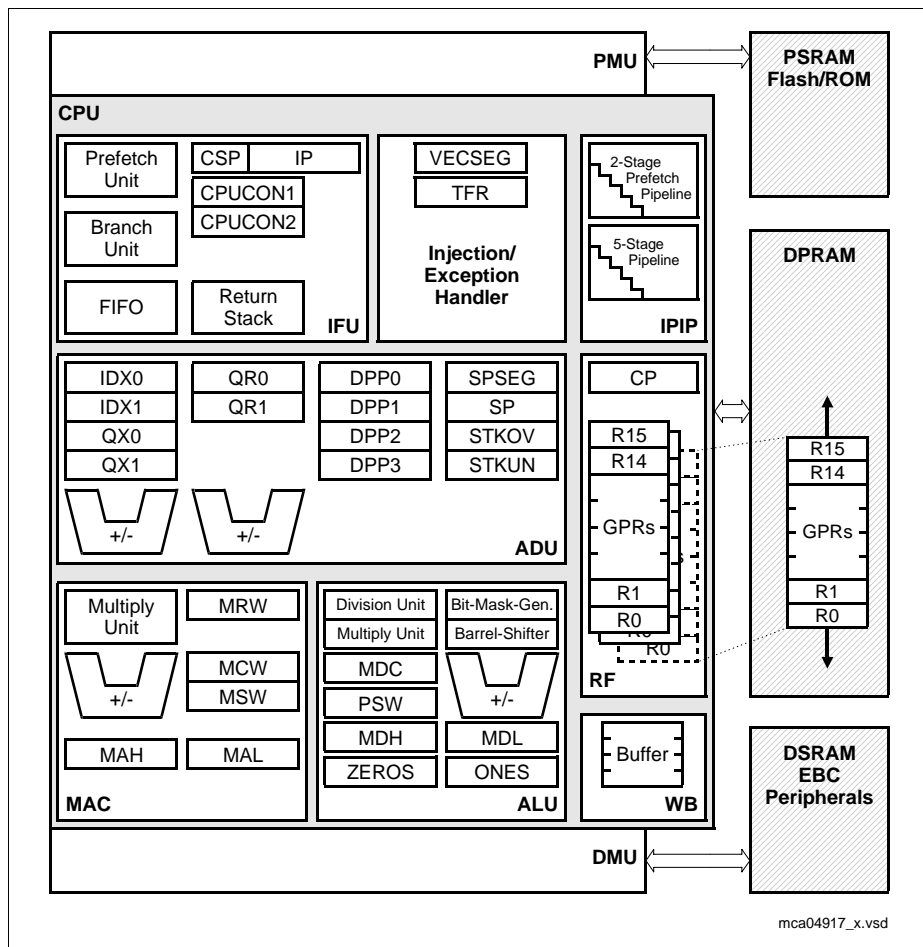


Figure 5 CPU Block Diagram

3.4 Memory Protection Unit (MPU)

The XC226xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XC226xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

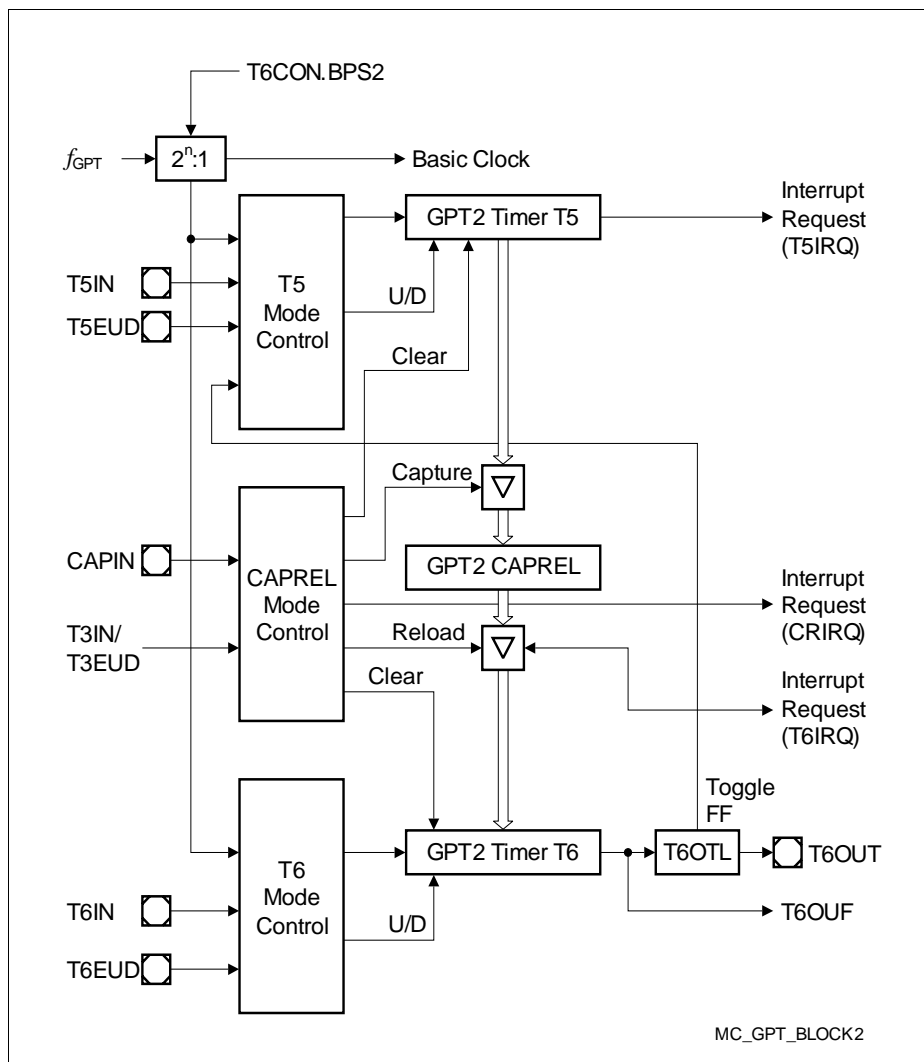


Figure 9 Block Diagram of GPT2

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

Functional Description

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction ¹⁾	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC226xM are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in [Section 4.6.4](#).

Supply Voltage Restrictions

The XC226xM can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

During power-on sequences, the supply voltages may only change with a maximum speed of $dV/dt < 5 \text{ V/}\mu\text{s}$, i.e. the target supply voltage may be reached earliest after approx. 1 μs .

Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins V_{DDPA}/V_{DDPB} is recommended.

Electrical Parameters

4.2.1 DC Parameters

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

Table 14 is valid under the following conditions:

$V_{DDP} \geq 4.5 \text{ V}$; $V_{DDPtyp} = 5 \text{ V}$; $V_{DDP} \leq 5.5 \text{ V}$

Table 14 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	$C_{IO} \text{ CC}$	–	–	10	pF	not subject to production test
Input Hysteresis ²⁾	$HYS \text{ CC}$	$0.11 \times V_{DDP}$	–	–	V	$R_S = 0 \text{ Ohm}$
Absolute input leakage current on pins of analog ports ³⁾	$ I_{OZ1} \text{ CC}$	–	10	200	nA	$V_{IN} > 0 \text{ V}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins. ³⁾¹⁾⁴⁾	$ I_{OZ2} \text{ CC}$	–	0.2	5	μA	$T_J \leq 110 \text{ }^\circ\text{C}$; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$
		–	0.2	15	μA	$T_J \leq 150 \text{ }^\circ\text{C}$; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$
Pull Level Force Current ⁵⁾	$ I_{PLF} \text{ SR}$	250	–	–	μA	⁶⁾
Pull Level Keep Current ⁷⁾	$ I_{PLK} \text{ SR}$	–	–	30	μA	⁶⁾
Input high voltage (all except XTAL1)	$V_{IH} \text{ SR}$	$0.7 \times V_{DDP}$	–	$V_{DDP} + 0.3$	V	
Input low voltage (all except XTAL1)	$V_{IL} \text{ SR}$	-0.3	–	$0.3 \times V_{DDP}$	V	
Output High voltage ⁸⁾	$V_{OH} \text{ CC}$	$V_{DDP} - 1.0$	–	–	V	$I_{OH} \geq I_{OHmax}$
		$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq I_{OHnom}$ ⁹⁾

Electrical Parameters

Table 14 DC Characteristics for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Low Voltage ⁸⁾	$V_{OL\ CC}$	—	—	1.0	V	$I_{OL} \leq I_{OLmax}$
		—	—	0.4	V	$I_{OL} \leq I_{OLnom}$ ⁹⁾

- 1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.
- 2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV} .
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times T_J)}$ [μA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 μA. Leakage derating depending on voltage level ($DV = V_{DDP} - V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax} - (1.6 \times DV)$ (μA). This voltage derating formula is an approximation which applies for maximum temperature.
- 5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{ILmax}$ for a pullup; $V_{PIN} \geq V_{IHmin}$ for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IHmin}$ for a pullup; $V_{PIN} \leq V_{ILmax}$ for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 9) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.

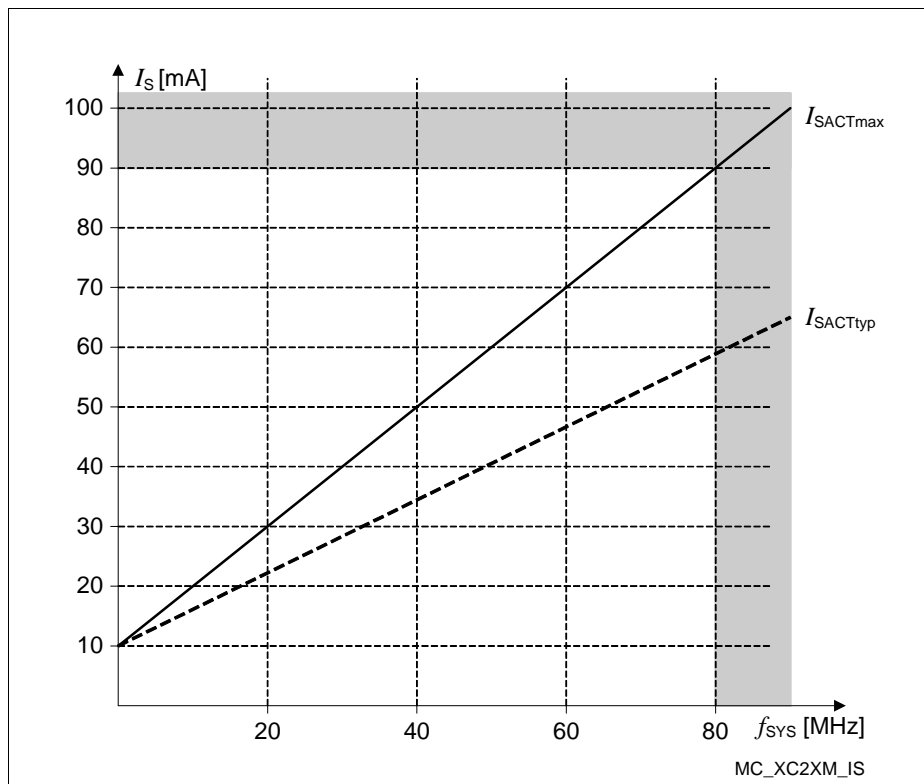


Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Electrical Parameters
Table 18 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND ²⁾	t_{BWG} CC	—	—	50	³⁾	
Broken wire detection delay against VAREF ²⁾	t_{BWR} CC	—	—	50	⁴⁾	
Conversion time for 8-bit result ²⁾	t_{c8} CC	$(11 + \text{STC}) \times t_{ADCI} + 2 \times t_{SYS}$				
Conversion time for 10-bit result ²⁾	t_{c10} CC	$(13 + \text{STC}) \times t_{ADCI} + 2 \times t_{SYS}$				
Total Unadjusted Error	TUE CC	—	1	2	LSB ⁵⁾	
Wakeup time from analog powerdown, fast mode ²⁾	t_{WAF} CC	—	—	4	μs	
Wakeup time from analog powerdown, slow mode ²⁾	t_{WAS} CC	—	—	15	μs	
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.05$	—	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	—	V_{AREF}	V ⁶⁾	
Analog reference voltage	V_{AREF} SR	$V_{AGND} + 1.0$	—	$V_{DDPA} + 0.05$	V ⁵⁾	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 μs . Result below 10% (66_H).

4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 μs . This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H).

5) TUE is tested at $V_{AREF} = V_{DDPA} = 5.0 \text{ V}$, $V_{AGND} = 0 \text{ V}$. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

6) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.

PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 24 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency (VCO controlled)	f_{VCO} CC	50	–	110	MHz	VCOSEL = 00 _B
		100	–	160	MHz	VCOSEL = 01 _B
VCO output frequency (VCO free-running)	f_{VCO} CC	10	–	40	MHz	VCOSEL = 00 _B
		20	–	80	MHz	VCOSEL = 01 _B

4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

$$f_{SYS} = f_{WU}$$

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.

Please refer to the Programmer's Guide.

Table 31 EBC External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for \overline{RD} , $\overline{WR}(L/H)$	t_{10} CC	–	11	20	ns	
Output valid delay for BHE, ALE	t_{11} CC	–	10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	10	22	ns	
Output valid delay for \overline{CS}	t_{14} CC	–	10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	10	22	ns	
Output hold time for \overline{RD} , $\overline{WR}(L/H)$	t_{20} CC	-2	8	10	ns	
Output hold time for \overline{BHE} , ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for \overline{CS}	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-9	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of \overline{RD} . Address changes before the end of \overline{RD} have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of \overline{RD} .

Electrical Parameters

Table 33 USIC SSC Master Mode Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	—	—	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 34 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	7	—	—	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	7	—	—	ns	
Receive data input setup time to shift clock receive edge ¹⁾	t_{12} SR	7	—	—	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	5	—	—	ns	
Data output DOUT valid time	t_{14} CC	7	—	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

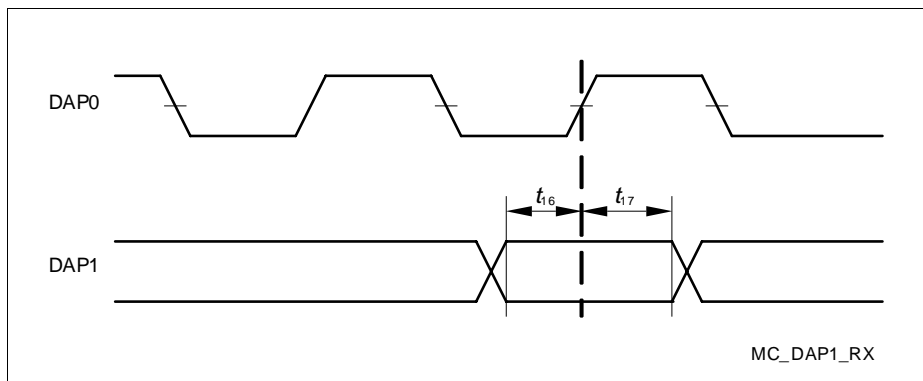


Figure 28 DAP Timing Host to Device

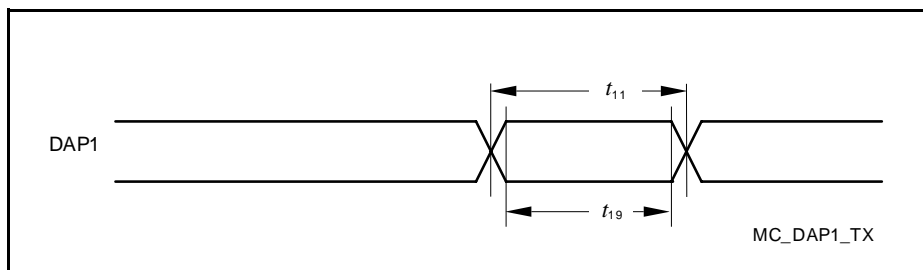


Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.