Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply. C_L = 20 pF .

Table 38 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50[1]			ns	[2]
TCK high time	t_2 SR	16			ns	
TCK low time	t_3 SR	16			ns	
TCK clock rise time	t_4 SR			8	ns	
TCK clock fall time	t_5 SR			8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6			ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6			ns	
TDO valid from TCK falling edge (propagation delay)[3]	t_8 CC		25	29	ns	
TDO high impedance to valid output from TCK falling edge[4][3]	t_9 CC		25	29	ns	
TDO valid output to high impedance from TCK falling edge[3]	t_{10} CC		25	29	ns	
TDO hold after TCK falling edge[3]	t_{18} CC	5			ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.
2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.
3) The falling edge on TCK is used to generate the TDO timing.
4) The setup time for TDO is given implicitly by the TCK cycle time.