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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2267m104f80lrabkxuma1

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XC226xM	
Revision H	listory: V2.1, 2011-07
Previous Ve	ersion(s):
V2.0, 2009-	-03
V1.3, 2008-	-11
V1.2, 2008-	-09
V1.1, 2008-	-06 Preliminary
V1.0, 2008-	-06 (Intermediate version)
Page	Subjects (major changes since last revisions)
42	ID registers added
90	ADC capacitances corrected (typ. vs. max.)
94	Conditions relaxed for Δf_{INT}
	Range for f_{WU} adapted according to PCN 2010-013-A
	Added startup time from power-on t_{SPO}
	More detailled specification of t _{SSB}
132	Quality declarations added

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General Device Information

Key to Pin Definitions

Ctrl.: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc.

Output signal OH is controlled by hardware.

- **Type**: Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Pin Symbol Ctrl. Function 3 TESTM L In/B **Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDBB}). An internal pull-up device will hold this pin high when nothing is driving it. 4 P7.2 00/1 St/B Bit 2 of Port 7. General Purpose Input/Output EMUX0 O1 St/B External Analog MUX Control Output 0 (ADC1) TxDC4 02 St/B CAN Node 4 Transmit Data Output O3 St/B TxDC5 CAN Node 5 Transmit Data Output CCU62 CCP L St/B CCU62 Position Input 0 OS0A TDI C IH St/B JTAG Test Data Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. 5 TRST L In/B Test-System Reset Input For normal system operation, pin TRST should be held low. A high level at this pin at the rising edge of PORST activates the XC226xM's debug system. In this case, pin TRST must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.

Table 6 Pin Definitions and Functions



General Device Information

Table	Table 6 Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
78	P1.0	O0 / I	St/B	Bit 0 of Port 1, General Purpose Input/Output		
	U1C0_MCLK OUT	01	St/B	USIC1 Channel 0 Master Clock Output		
	U1C0_SELO 4	O2	St/B	USIC1 Channel 0 Select/Control 4 Output		
	A8	ОН	St/B	External Bus Interface Address Line 8		
	ESR1_3	I	St/B	ESR1 Trigger Input 3		
	CCU62_CTR APB	I	St/B	CCU62 Emergency Trap Input		
	T6INB	1	St/B	GPT12E Timer T6 Count/Gate Input		
79	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output		
	U0C0_MCLK OUT	01	St/B	USIC0 Channel 0 Master Clock Output		
	U0C1_SELO 0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output		
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output		
	AD8	OH / IH	St/B	External Bus Interface Address/Data Line 8		
	CCU60_CCP OS1A	I	St/B	CCU60 Position Input 1		
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input		
	BRKIN_B	I	St/B	OCDS Break Signal Input		
	T3EUDB	I	St/B	GPT12E Timer T3 External Up/Down Control Input		



Table 6

XC2268M/67M, XC2265M/64M/63M XC2000 Family / Base Line

General Device Information

Pin	Symbol	Ctrl.	Туре	Function
2, 25, 27,	V _{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins.
50, 52, 75, 77, 100				Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V _{DDPB} .
1, 26, 51,	V _{SS}	-	PS/	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane.
76				Note: Also the exposed pad is connected internally to V_{SS} . To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

Pin Definitions and Functions (cont'd)

 To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.



Functional Description

3.9 Capture/Compare Units CCU6x

The XC226xM types feature the CCU60, CCU61, CCU62 and CCU63 unit(s).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage



Functional Description



Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.



Functional Description







Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time



Functional Description

3.18 Parallel Ports

The XC226xM provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 10**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15A8), CCU6, USIC
P2	14	I/O	EBC (READY, BHE, A23A16, AD15AD13, D15D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P4	4	I/O	EBC (CS3CS0), CC2, CAN, GPT12E, USIC
P5	11	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	3	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P10	16	I/O	EBC (ALE, RD, WR, AD12AD0, D12D0), CCU6, USIC, DAP/JTAG, CAN
P15	5	I	Analog Inputs, GPT12E

Table 10	Summary	y of the	XC226xM's	Ports
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4.1.3 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode. See also "Pad Properties" on Page 108.

4.1.4 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC226xM and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column "Symbol":

CC (Controller Characteristics):

The logic of the XC226xM provides signals with the specified characteristics.

SR (System Requirement):

The external system must provide signals with the specified characteristics to the XC226xM.



Sample time and conversion time of the XC226xM's A/D converters are programmable. The timing above can be calculated using **Table 19**.

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time ¹⁾ t _s
000000 _B	<i>f</i> _{SYS}	00 _H	$t_{ADCI} \times 2$
000001 _B	<i>f</i> _{SYS} / 2	01 _H	$t_{ADCI} \times 3$
000010 _B	<i>f</i> _{SYS} / 3	02 _H	$t_{ADCI} \times 4$
:	$f_{\rm SYS}$ / (DIVA+1)	:	$t_{ADCI} \times (STC+2)$
111110 _B	f _{SYS} / 63	FE _H	$t_{ADCI} \times 256$
111111 _B	f _{SYS} / 64	FF _H	$t_{ADCI} \times 257$

 Table 19
 A/D Converter Computation Table

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions:	$f_{\rm SYS}$	= 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03 _H , STC = 00 _H
Analog clock	$f_{\rm ADCI}$	$= f_{SYS} / 4 = 20 \text{ MHz}$, i.e. $t_{ADCI} = 50 \text{ ns}$
Sample time	t _S	$= t_{ADCI} \times 2 = 100 \text{ ns}$
Conversion 10	-bit:	
	<i>t</i> _{C10}	= $13 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 13×50 ns + 2×12.5 ns = 0.675 μ s
Conversion 8-b	oit:	
	t _{C8}	= $11 \times t_{ADCI}$ + 2 × t_{SYS} = 11 × 50 ns + 2 × 12.5 ns = 0.575 µs

Converter Timing Example B:

Assumptions:	$f_{\rm SYS}$	= 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02 _H , STC = 03 _H					
Analog clock	$f_{\rm ADCI}$	$= f_{SYS} / 3 = 13.3 \text{ MHz}$, i.e. $t_{ADCI} = 75 \text{ ns}$					
Sample time	t _S	$= t_{ADCI} \times 5 = 375 \text{ ns}$					
Conversion 10-bit:							
	t _{C10}	= $16 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 16×75 ns + 2×25 ns = 1.25 µs					
Conversion 8-bi	Conversion 8-bit:						
	t _{C8}	= $14 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 14×75 ns + 2×25 ns = 1.10 µs					



Electrical Parameters

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use the this warning level.



4.5 Flash Memory Parameters

The XC226xM is delivered with all Flash sectors erased and with no protection installed. The data retention time of the XC226xM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Parallel Flash module program/erase limit	$N_{PP}SR$	-	-	4 ¹⁾		$N_{\text{FL}_{\text{RD}}} \le 1,$ $f_{\text{SYS}} \le 80 \text{ MHz}$
depending on Flash read activity		-	-	1 ²⁾		$N_{\rm FL_RD}$ > 1
Flash erase endurance for security pages	$N_{\rm SEC}{ m SR}$	10	-	-	cycle s	t _{RET} ≥ 20 years
Flash wait states ³⁾	N _{WSFLAS} _H SR	1	-	-		$f_{SYS} \le 8 \text{ MHz}$
		2	-	-		$f_{SYS} \le 13 \text{ MHz}$
		3	-	-		$f_{SYS} \le 17 \text{ MHz}$
		4	-	-		$f_{\rm SYS}$ > 17 MHz
Erase time per sector/page	t _{ER} CC	-	7 ⁴⁾	8.0	ms	
Programming time per page	t _{PR} CC	-	34)	3.5	ms	
Data retention time	t _{RET} CC	20	-	-	year s	$N_{\rm Er} \le 1\ 000$ cycles
Drain disturb limit	$N_{\rm DD}~{ m SR}$	32	-	-	cycle s	

Table 23 Flash Parameters



The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and Figure 20).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS} . The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

 D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of $\mathbf{T} \times TCS$ the accumulated jitter D_T is determined by:

 D_{T} [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

 f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

 $D_{max} = \pm (220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

 $D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$

= 5.97 × [0.768 × 2 / 26.39 + 0.232]

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

 $D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

 $\begin{array}{l} \mathsf{D}_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) \ / \ (0.83 \times 33 - 1) + 0.058 \times 2] \\ = 7.63 \times [0.884 \times 2 \ / \ 26.39 + 0.116] \end{array}$





Figure 20 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$.

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.



PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
VCO output frequency	$f_{\rm VCO}$ CC	50	-	110	MHz	$VCOSEL = 00_B$
(VCO controlled)		100	-	160	MHz	$VCOSEL = 01_B$
VCO output frequency	$f_{\rm VCO}$ CC	10	-	40	MHz	$VCOSEL = 00_B$
(VCO free-running)		20	-	80	MHz	$VCOSEL = 01_B$

Table 24 System PLL Parameters

4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Variable Memory Cycles

External bus cycles of the XC226xM are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 29	Programmable Bus Cv	vcle Phases (see timino	diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase $(1 \dots 2 \text{ TCS})$ can be extended by $0 \dots 3 \text{ TCS}$ if the address window is changed	tpAB	1 2 (5)	TCS
Command delay phase	tpC	03	TCS
Write Data setup/MUX Tristate phase	tpD	0 1	TCS
Access phase	tpE	1 32	TCS
Address/Write Data hold phase	tpF	03	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply; $C_L = 20 \text{ pF}$.



Table 30 EBC External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	-	Test Condition
$\frac{\text{Output valid delay for }\overline{\text{RD}},}{\text{WR}(\text{L/H})}$	<i>t</i> ₁₀ CC	-	7	13	ns	
Output valid delay for BHE, ALE	<i>t</i> ₁₁ CC	-	7	14	ns	
Address output valid delay for A23 A0	<i>t</i> ₁₂ CC	-	8	14	ns	
Address output valid delay for AD15 AD0 (MUX mode)	<i>t</i> ₁₃ CC	-	8	15	ns	
Output valid delay for CS	t ₁₄ CC	-	7	13	ns	
Data output valid delay for AD15 AD0 (write data, MUX mode)	<i>t</i> ₁₅ CC	-	8	15	ns	
Data output valid delay for D15 D0 (write data, DEMUX mode)	<i>t</i> ₁₆ CC	-	8	15	ns	
Output hold time for \overline{RD} , WR(L/H)	<i>t</i> ₂₀ CC	-2	6	8	ns	
Output hold time for \overline{BHE} , ALE	<i>t</i> ₂₁ CC	-2	6	10	ns	
Address output hold time for AD15 AD0	<i>t</i> ₂₃ CC	-3	6	8	ns	
Output hold time for CS	t ₂₄ CC	-3	6	11	ns	
Data output hold time for D15 D0 and AD15 AD0	<i>t</i> ₂₅ CC	-3	6	8	ns	
Input setup time for READY, D15 D0, AD15 AD0	t ₃₀ SR	25	15	-	ns	
Input hold time READY, D15 D0, AD15 AD0 ¹⁾	<i>t</i> ₃₁ SR	0	-7	-	ns	

 Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.



Parameter	Symbol	Values			Unit	Note /			
		Min.	Тур.	Max.		Test Condition			
DAP0 clock period	<i>t</i> ₁₁ SR	25 ¹⁾	-	_	ns				
DAP0 high time	t ₁₂ SR	8	-	-	ns				
DAP0 low time	t ₁₃ SR	8	-	_	ns				
DAP0 clock rise time	t ₁₄ SR	-	-	4	ns				
DAP0 clock fall time	t ₁₅ SR	-	-	4	ns				
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	pad_type= stan dard			
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	pad_type= stan dard			
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	12	17	-	ns	pad_type= stan dard			

Table 37 DAP Interface Timing for Lower Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \ge t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



Figure 27 Test Clock Timing (DAP0)



Electrical Parameters



Figure 28 DAP Timing Host to Device



Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.