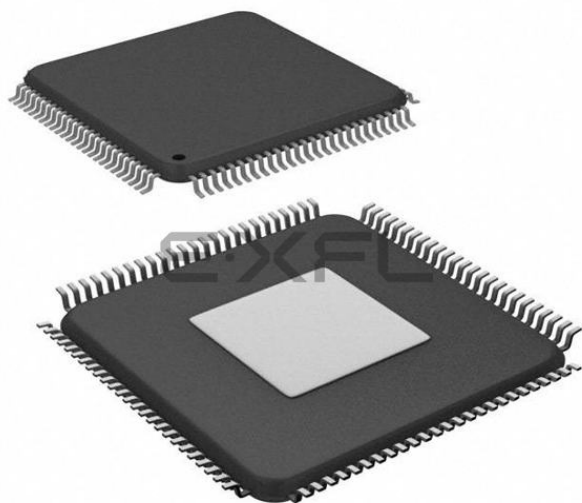




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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2267m72f80laakxuma1

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P6.2	O0 / I	DA/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	DA/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	DA/A	GPT12E Timer T6 Toggle Latch Output
	U1C1_SCLK OUT	O3	DA/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	DA/A	USIC1 Channel 1 Shift Clock Input
15	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
16	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5INA	I	In/A	GPT12E Timer T5 Count/Gate Input
17	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
18	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUDA	I	In/A	GPT12E Timer T6 External Up/Down Control Input
19	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
20	V _{AREF}	-	PS/A	Reference Voltage for A/D Converters ADC0/1
21	V _{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
22	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
23	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
32	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61
33	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0
	ADC1_CH11	I	In/A	Analog Input Channel 11 for ADC1
34	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
	CCU63_T13 HRF	I	In/A	External Run Control Input for T13 of CCU63
35	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
	RxDC2F	I	In/A	CAN Node 2 Receive Data Input
36	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO 3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	TXDC2	O3	St/B	CAN Node 2 Transmit Data Output
	READY	IH	St/B	External Bus Interface READY Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
53	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3	St/B	CCU61 Channel 0 IOutput
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC60INA	I	St/B	CCU61 Channel 0 Input
	ESR1_11	I	St/B	ESR1 Trigger Input 11
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3	St/B	CCU61 Channel 1 Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC61INA	I	St/B	CCU61 Channel 1 Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLK OUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output 1)
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
57	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input 1
58	TCK_A	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLK OUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC6 2	O3	St/B	CCU61 Channel 2 Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
58	CCU61_CC6 2INA	I	St/B	CCU61 Channel 2 Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC6 2	O2	St/B	CCU60 Channel 2 Output
	U3C0_SELO 1	O3	St/B	USIC3 Channel 0 Select/Control 1 Output
	AD2	OH / IH	St/B	External Bus Interface Address/Data Line 2
	CCU60_CC6 2INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
	U3C0_DX2B	I	St/B	USIC3 Channel 0 Shift Control Input
63	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO 0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO 1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COU T61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
	ESR2_8	I	St/B	ESR2 Trigger Input 8
65	P2.13	O0 / I	St/B	Bit 13 of Port 2, General Purpose Input/Output
	U2C1_SELO 2	O1	St/B	USIC2 Channel 1 Select/Control 2 Output
	RxDC2D	I	St/B	CAN Node 2 Receive Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
78	P1.0	O0 / I	St/B	Bit 0 of Port 1, General Purpose Input/Output
	U1C0_MCLK OUT	O1	St/B	USIC1 Channel 0 Master Clock Output
	U1C0_SELO 4	O2	St/B	USIC1 Channel 0 Select/Control 4 Output
	A8	OH	St/B	External Bus Interface Address Line 8
	ESR1_3	I	St/B	ESR1 Trigger Input 3
	CCU62_CTR APB	I	St/B	CCU62 Emergency Trap Input
	T6INB	I	St/B	GPT12E Timer T6 Count/Gate Input
79	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output
	U0C0_MCLK OUT	O1	St/B	USIC0 Channel 0 Master Clock Output
	U0C1_SELO 0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	AD8	OH / IH	St/B	External Bus Interface Address/Data Line 8
	CCU60_CCP OS1A	I	St/B	CCU60 Position Input 1
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input
	BRKIN_B	I	St/B	OCDS Break Signal Input
	T3EUDB	I	St/B	GPT12E Timer T3 External Up/Down Control Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
80	P10.9	O0 / I	St/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLKOUT	O2	St/B	USIC0 Channel 1 Master Clock Output
	AD9	OH / IH	St/B	External Bus Interface Address/Data Line 9
	CCU60_CCP OS2A	I	St/B	CCU60 Position Input 2
	TCK_B	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	GPT12E Timer T3 Count/Gate Input
81	P1.1	O0 / I	St/B	Bit 1 of Port 1, General Purpose Input/Output
	CCU62_COUT62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO5	O2	St/B	USIC1 Channel 0 Select/Control 5 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	A9	OH	St/B	External Bus Interface Address Line 9
	ESR2_3	I	St/B	ESR2 Trigger Input 3
	U2C1_DX0C	I	St/B	USIC2 Channel 1 Shift Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	CCU62_COU T61	O1	St/B	CCU62 Channel 1 Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
	RxDC5A	I	St/B	CAN Node 5 Receive Data Input
91	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input
92	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output
	CCU62_COU T60	O1	St/B	CCU62 Channel 0 Output
	U1C1_SELO 3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output
	BRKOUT	O3	St/B	OCDS Break Signal Output
	A13	OH	St/B	External Bus Interface Address Line 13
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input

3.1 Memory Subsystem and Organization

The memory space of the XC226xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC226xM Memory Map ¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
IMB register space	FF'FF00 _H	FF'FFFF _H	256 Bytes	–
Reserved (Access trap)	F0'0000 _H	FF'FEFF _H	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'8000 _H	EF'FFFF _H	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000 _H	E8'7FFF _H	32 Kbytes	With Flash timing
Reserved for PSRAM	E0'8000 _H	E7'FFFF _H	480 Kbytes	Mirrors PSRAM
Program SRAM	E0'0000 _H	E0'7FFF _H	32 Kbytes	Maximum speed
Reserved for Flash	CD'0000 _H	DF'FFFF _H	<1.25 Mbytes	–
Program Flash 3	CC'0000 _H	CC'FFFF _H	64 Kbytes	–
Program Flash 2	C8'0000 _H	CB'FFFF _H	256 Kbytes	–
Program Flash 1	C4'0000 _H	C7'FFFF _H	256 Kbytes	–
Program Flash 0	C0'0000 _H	C3'FFFF _H	256 Kbytes	³⁾
External memory area	40'0000 _H	BF'FFFF _H	8 Mbytes	–
Available Ext. IO area ⁴⁾	21'0000 _H	3F'FFFF _H	< 2 Mbytes	Minus USIC/CAN
Reserved	20'BC00 _H	20'FFFF _H	17 Kbytes	–
USIC alternate regs.	20'B000 _H	20'BFFF _H	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000 _H	20'AFFF _H	12 Kbytes	Accessed via EBC
Reserved	20'6000 _H	20'7FFF _H	8 Kbytes	–
USIC registers	20'4000 _H	20'5FFF _H	8 Kbytes	Accessed via EBC
MultiCAN registers	20'0000 _H	20'3FFF _H	16 Kbytes	Accessed via EBC
External memory area	01'0000 _H	1F'FFFF _H	< 2 Mbytes	Minus segment 0
SFR area	00'FE00 _H	00'FFFF _H	0.5 Kbyte	–
Dual-Port RAM	00'F600 _H	00'FDFF _H	2 Kbytes	–
Reserved for DPRAM	00'F200 _H	00'F5FF _H	1 Kbyte	–
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbyte	–
XSFR area	00'E000 _H	00'EFFF _H	4 Kbytes	–

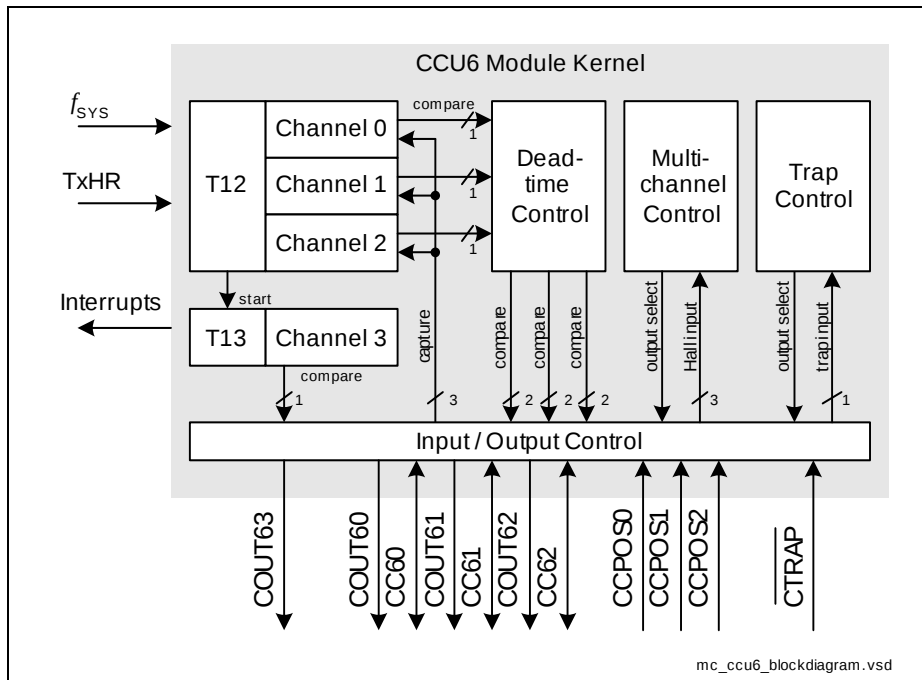


Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

Functional Description

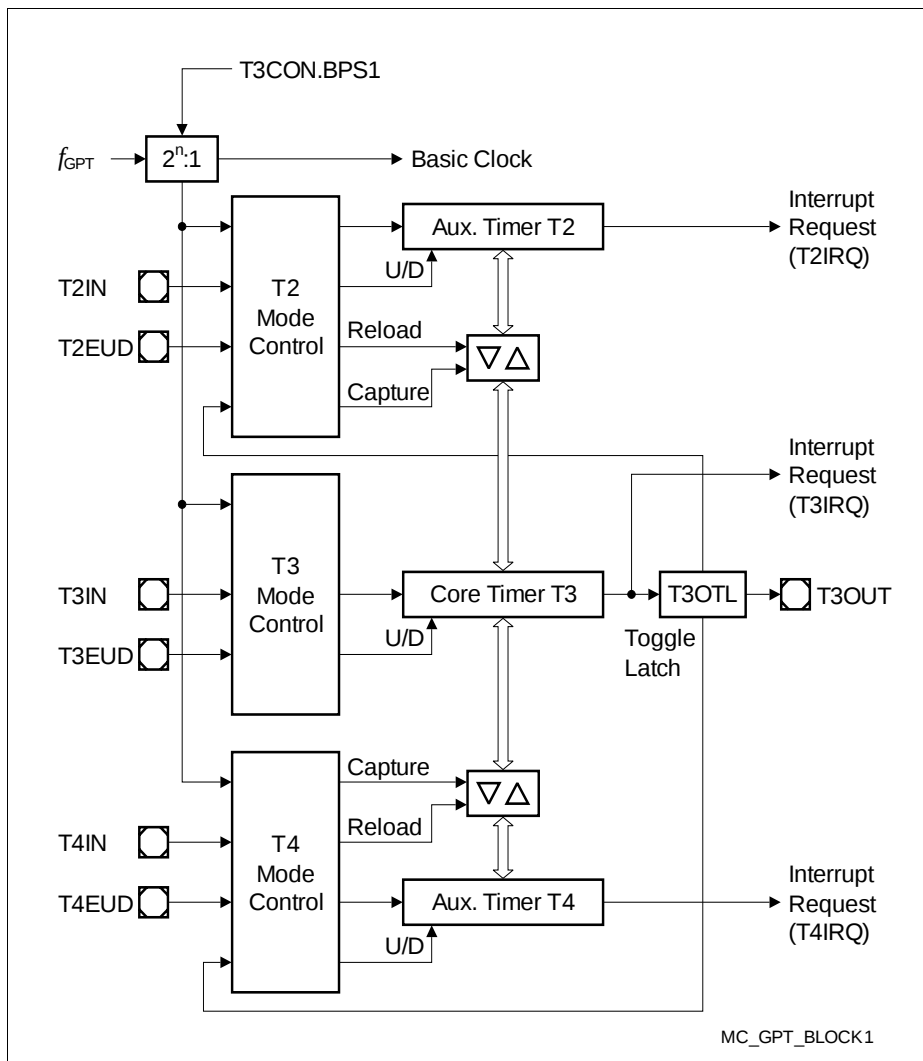


Figure 8 Block Diagram of GPT1

Functional Description

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

- 1) The Enter Power Down Mode instruction is not used in the XC226xM, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC226xM are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in [Section 4.6.4](#).

Supply Voltage Restrictions

The XC226xM can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

During power-on sequences, the supply voltages may only change with a maximum speed of $dV/dt < 5 \text{ V/}\mu\text{s}$, i.e. the target supply voltage may be reached earliest after approx. 1 μs .

Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins V_{DDPA}/V_{DDPB} is recommended.

4.6 AC Parameters

These parameters describe the dynamic behavior of the XC226xM.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

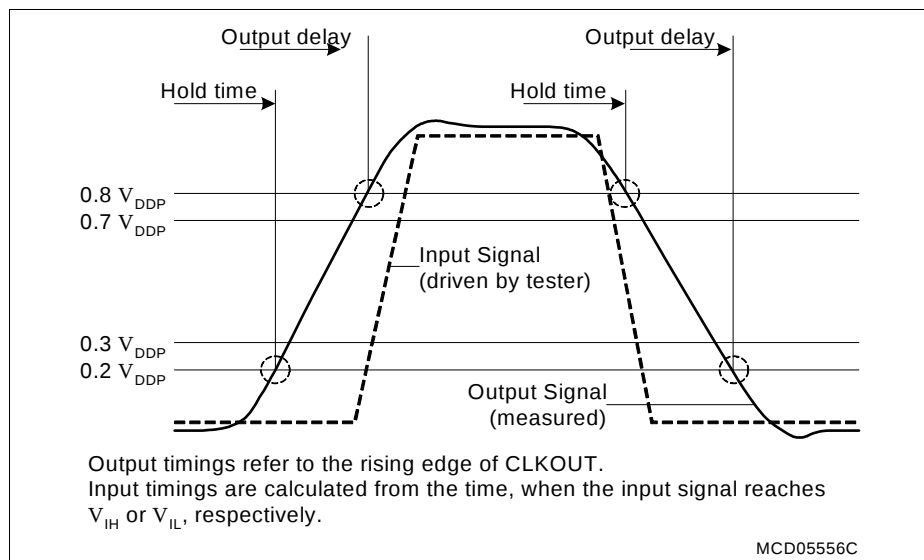


Figure 17 Input Output Waveforms

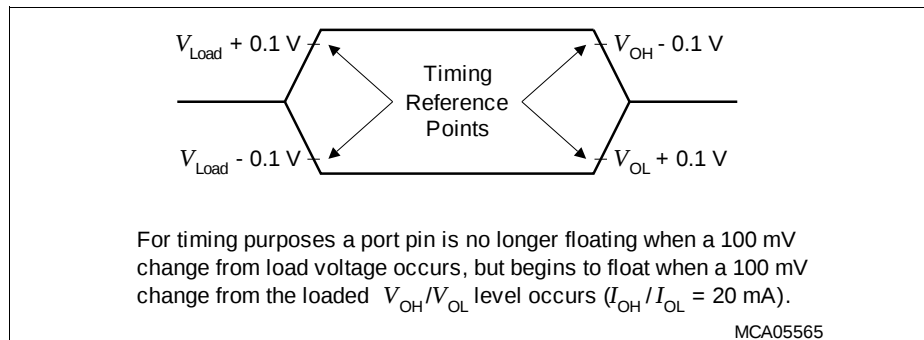


Figure 18 Floating Waveforms

Electrical Parameters

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and [Figure 20](#)).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS} . The number of VCO cycles is $K2 \times T$, where T is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

$$D_{Tmax} [ns] = \pm(220 / (K2 \times f_{SYS}) + 4.3)$$

This maximum value is applicable, if either the number of clock cycles $T > (f_{SYS} / 1.2)$ or the prescaler value $K2 > 17$.

In all other cases for a timeframe of $T \times TCS$ the accumulated jitter D_T is determined by:

$$D_T [ns] = D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and $K2 = 4$:

$$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97 \text{ ns (Not applicable directly in this case!)}$$

$$\begin{aligned} D_3 &= 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4] \\ &= 5.97 \times [0.768 \times 2 / 26.39 + 0.232] \\ &= 1.7 \text{ ns} \end{aligned}$$

Example, for a period of 3 TCSs @ 33 MHz and $K2 = 2$:

$$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63 \text{ ns (Not applicable directly in this case!)}$$

$$\begin{aligned} D_3 &= 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2] \\ &= 7.63 \times [0.884 \times 2 / 26.39 + 0.116] \\ &= 1.4 \text{ ns} \end{aligned}$$

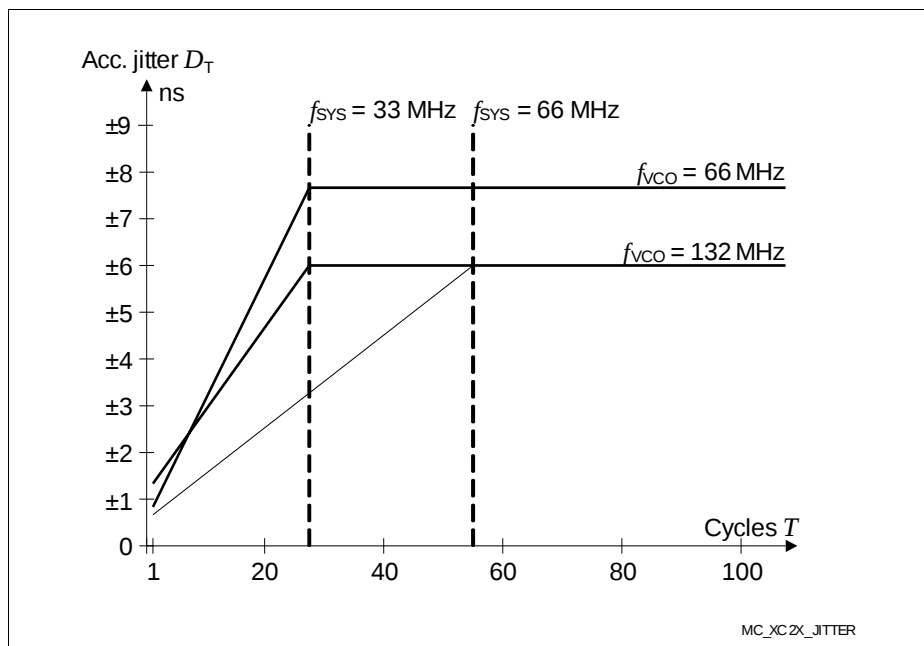


Figure 20 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$.

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of $V_{PP} = 50 \text{ mV}$. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

4.6.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; $C_L = 20$ pF.

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{SYS} - 8^{1)}$	—	—	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{SYS} - 6^{1)}$	—	—	ns	
Data output DOUT valid time	t_3 CC	-6	—	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	—	—	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 33 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{SYS} - 10^{1)}$	—	—	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{SYS} - 9^{1)}$	—	—	ns	
Data output DOUT valid time	t_3 CC	-7	—	11	ns	

4.6.7 Debug Interface Timing

The debugger can communicate with the XC226xM either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; $C_L = 20$ pF.

Table 36 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	25 ¹⁾	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period ²⁾	t_{19} CC	17	20	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{\text{SYS}}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

Table 37 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	25 ¹⁾	—	—	ns	
DAP0 high time	t_{12} SR	8	—	—	ns	
DAP0 low time	t_{13} SR	8	—	—	ns	
DAP0 clock rise time	t_{14} SR	—	—	4	ns	
DAP0 clock fall time	t_{15} SR	—	—	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	—	—	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	—	—	ns	pad_type= standard
DAP1 valid per DAP0 clock period ²⁾	t_{19} CC	12	17	—	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

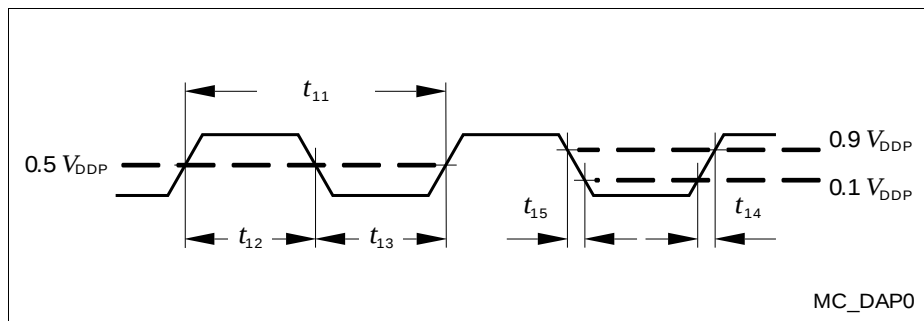


Figure 27 Test Clock Timing (DAP0)

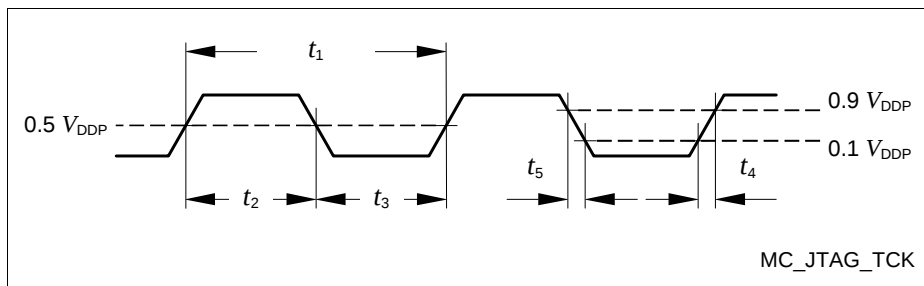


Figure 30 Test Clock Timing (TCK)

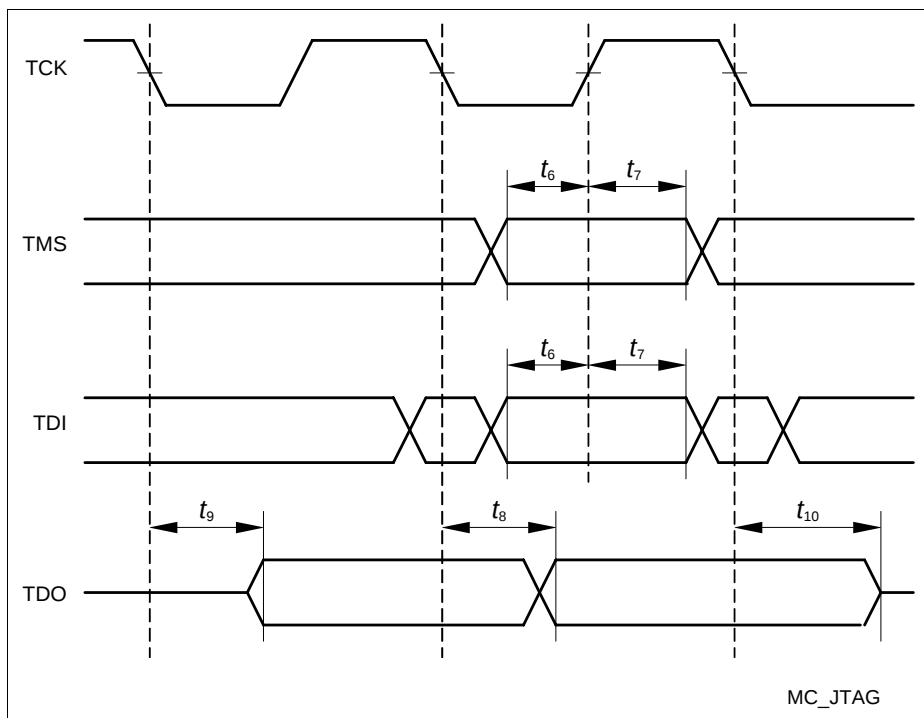


Figure 31 JTAG Timing