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Details

EXFL

2 0 0 0 0 0	
Product Status	Obsolete
Core Processor	C1665V2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2268m56f66laafxuma1

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General Device Information

2.1 Pin Configuration and Definition

The pins of the XC226xM are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.



Figure 3 XC226xM Pin Configuration (top view)



General Device Information

Tabl	able 6 Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
53	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output			
	U1C0_DOUT	01	St/B	USIC1 Channel 0 Shift Data Output			
	CCU61_CC6 0	O3	St/B	CCU61 Channel 0 IOutput			
	A0	OH	St/B	External Bus Interface Address Line 0			
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input			
	CCU61_CC6 0INA	I	St/B	CCU61 Channel 0 Input			
	ESR1_11	I	St/B	ESR1 Trigger Input 11			
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output			
	U0C1_SELO 0	01	St/B	USIC0 Channel 1 Select/Control 0 Output			
	U0C0_SELO 1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output			
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.			
	A20	OH	St/B	External Bus Interface Address Line 20			
	U0C1_DX2C	Į	St/B	USIC0 Channel 1 Shift Control Input			
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input			
	ESR2_7	I	St/B	ESR2 Trigger Input 7			
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output			
	U1C0_DOUT	01	St/B	USIC1 Channel 0 Shift Data Output			
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output			
	CCU61_CC6 1	O3	St/B	CCU61 Channel 1 Output			
	A1	OH	St/B	External Bus Interface Address Line 1			
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input			
	CCU61_CC6 1INA	I	St/B	CCU61 Channel 1 Input			
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input			



General Device Information

Table	Fable 6Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
86	P10.13	O0 / I	St/B	Bit 13 of Port 10, General Purpose Input/Output			
	U1C0_DOUT	01	St/B	USIC1 Channel 0 Shift Data Output			
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output			
	U1C0_SELO 3	O3	St/B	USIC1 Channel 0 Select/Control 3 Output			
	WR/WRL	ОН	St/B	External Bus Interface Write Strobe Output Active for each external write access, when \overline{WR} , active for ext. writes to the low byte, when \overline{WRL} .			
	U1C0_DX0D	I	St/B	USIC1 Channel 0 Shift Data Input			
87	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output			
	CCU62_COU T63	01	St/B	CCU62 Channel 3 Output			
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output			
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output			
	A11	ОН	St/B	External Bus Interface Address Line 11			
	ESR2_4	I	St/B	ESR2 Trigger Input 4			
	CCU62_T12 HRB	1	St/B	External Run Control Input for T12 of CCU62			
89	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output			
	U1C0_SELO 1	01	St/B	USIC1 Channel 0 Select/Control 1 Output			
	U0C1_DOUT	02	St/B	USIC0 Channel 1 Shift Data Output			
	U3C0_SCLK OUT	O3	St/B	USIC3 Channel 0 Shift Clock Output			
	RD	OH	St/B	External Bus Interface Read Strobe Output			
	ESR2_2	I	St/B	ESR2 Trigger Input 2			
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input			
	RxDC3C	I	St/B	CAN Node 3 Receive Data Input			
	U3C0_DX1A	I	St/B	USIC3 Channel 0 Shift Clock Input			



General Device Information

2.2 Identification Registers

The identification registers describe the current version of the XC226xM and of its modules.

Table 7 XC226xM Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820 _H	00'F07E _H	
SCU_IDCHIP	3801 _H	00'F07C _H	
SCU_IDMEM	30D0 _H	00'F07A _H	
SCU_IDPROG	1313 _H	00'F078 _H	
JTAG_ID	0017'E083 _H		marking EES-AA, ES-AA or AA



3.1 Memory Subsystem and Organization

The memory space of the XC226xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
IMB register space	FF'FF00 _H	FF'FFFF _H	256 Bytes	-
Reserved (Access trap)	F0'0000 _H	FF'FEFF _H	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'8000 _H	EF'FFFF _H	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000 _H	E8'7FFF _H	32 Kbytes	With Flash timing
Reserved for PSRAM	E0'8000 _H	E7'FFFF _H	480 Kbytes	Mirrors PSRAM
Program SRAM	E0'0000 _H	E0'7FFF _H	32 Kbytes	Maximum speed
Reserved for Flash	CD'0000 _H	DF'FFFF _H	<1.25 Mbytes	-
Program Flash 3	CC'0000 _H	CC'FFFF _H	64 Kbytes	-
Program Flash 2	C8'0000 _H	CB'FFFF _H	256 Kbytes	-
Program Flash 1	C4'0000 _H	C7'FFFF _H	256 Kbytes	-
Program Flash 0	C0'0000 _H	C3'FFFF _H	256 Kbytes	3)
External memory area	40'0000 _H	BF'FFFF _H	8 Mbytes	-
Available Ext. IO area ⁴⁾	21'0000 _H	3F'FFFF _H	< 2 Mbytes	Minus USIC/CAN
Reserved	20'BC00 _H	20'FFFF _H	17 Kbytes	-
USIC alternate regs.	20'B000 _H	20'BFFF _H	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000 _H	20'AFFF _H	12 Kbytes	Accessed via EBC
Reserved	20'6000 _H	20'7FFF _H	8 Kbytes	-
USIC registers	20'4000 _H	20'5FFF _H	8 Kbytes	Accessed via EBC
MultiCAN registers	20'0000 _H	20'3FFF _H	16 Kbytes	Accessed via EBC
External memory area	01'0000 _H	1F'FFFF _H	< 2 Mbytes	Minus segment 0
SFR area	00'FE00 _H	00'FFFF _H	0.5 Kbyte	-
Dual-Port RAM	00'F600 _H	00'FDFF _H	2 Kbytes	-
Reserved for DPRAM	00'F200 _H	00'F5FF _H	1 Kbyte	-
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbyte	-
XSFR area	00'E000 _H	00'EFFF _H	4 Kbytes	_

Table 8 XC226xM Memory Map ¹⁾



Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes			
Data SRAM	00'A000 _H	00'DFFF _H	16 Kbytes	-			
Reserved for DSRAM	00'8000 _H	00'9FFF _H	8 Kbytes	-			
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	-			

Table 8XC226xM Memory Map (cont'd)1)

 Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

 Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.



3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instructionfetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.







3.8 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range or variation for the timer period and resolution and allows precise adjustments to the application-specific requirements. In addition, an external count input allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.

All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible

Table 9 Compare Modes



3.20 Instruction Set Summary

Table 11 lists the instructions of the XC226xM.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "**Instruction Set Manual**".

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with Carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with Carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- \times 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2/4
OR(B)	Bitwise OR, (word/byte operands)	2/4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2/4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 11 Instruction Set Summary



Functional Description

Mnemonic	Description	Bytes				
NOP	Null operation	2				
CoMUL/CoMAC	Multiply (and accumulate)	4				
CoADD/CoSUB	Add/Subtract	4				
Co(A)SHR	(Arithmetic) Shift right	4				
CoSHL	Shift left	4				
CoLOAD/STORE	Load accumulator/Store MAC register	4				
CoCMP	Compare	4				
CoMAX/MIN	Maximum/Minimum	4				
CoABS/CoRND	Absolute value/Round accumulator	4				
CoMOV	Data move	4				
CoNEG/NOP	Negate accumulator/Null operation	4				

Table 11 Instruction Set Summary (cont'd)

1) The Enter Power Down Mode instruction is not used in the XC226xM, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.



			•	•	·	,
Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Output Low Voltage ⁸⁾	V _{OL} CC	-	-	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}$
		-	-	0.4	V	$I_{\rm OL} \leq I_{\rm OLnom}^{10}$

Table 15 DC Characteristics for Lower Voltage Range (cont'd)

 Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

- Not subject to production test verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm CV}$.
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x TJ-) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} <= V_{IL} for a pullup; V_{PIN} >= V_{IH} for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} >= V_{IH} for a pullup; V_{PIN} <= V_{IL} for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 9) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.
- 10) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



4.2.3 Power Consumption

The power consumed by the XC226xM depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current $I_{\rm S}$ depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current $I_{\rm S}$ and leakage current $I_{\rm LK}$ must be added:

 $I_{\text{DDP}} = I_{\text{S}} + I_{\text{LK}}.$

Note: The power consumption values are not subject to production test. They are verified by design/characterization.

To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

Active mode:

Regular operation, i.e. peripherals are active, code execution out of Flash.

Stopover mode:

Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

Standby mode:

Voltage domain DMP_1 switched off completely, power supply control switched off.

Note: The maximum values cover the complete specified operating range of all manufactured devices.

The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.

After a power reset, the decoupling capacitors for $V_{\rm DDIM}$ and $V_{\rm DDI1}$ are charged with the maximum possible current.

For additional information, please refer to Section 5.2, Thermal Considerations.

Note: Operating Conditions apply.



4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance. *Note: Operating Conditions apply.*

Table 18ADC Parameters

Parameter	Symbol	Values			Unit	Note /	
		Min.	Тур.	Max.		Test Condition	
Switched capacitance at an analog input	C _{AINSW} CC	-	4	5	pF	not subject to production test ¹⁾	
Total capacitance at an analog input	C _{AINT} CC	-	10	12	pF	not subject to production test ¹⁾	
Switched capacitance at the reference input	C _{AREFSW} CC	-	7	9	pF	not subject to production test ¹⁾	
Total capacitance at the reference input	C _{AREFT} CC	-	13	15	pF	not subject to production test ¹⁾	
Differential Non-Linearity Error	EA _{DNL} CC	-	0.8	1.0	LSB	not subject to production test	
Gain Error	EA _{GAIN} CC	-	0.4	0.8	LSB	not subject to production test	
Integral Non-Linearity	EA _{INL} CC	-	0.8	1.2	LSB	not subject to production test	
Offset Error	EA _{OFF} CC	-	0.5	0.8	LSB	not subject to production test	
Analog clock frequency	$f_{\rm ADCI}{\rm SR}$	0.5	-	20	MHz	Upper voltage range	
		0.5	-	16.5	MHz	Lower voltage range	
Input resistance of the selected analog channel	R _{AIN} CC	-	-	2	kOh m	not subject to production test ¹⁾	
Input resistance of the reference input	R _{AREF} CC	-	_	2	kOh m	not subject to production test ¹⁾	



Coding of bit fields LEVxV in SWD and PVC Configuration Registers

	•••••••••••••••••••••	
Code	Default Voltage Level	Notes ¹⁾
0000 _B	2.9 V	
0001 _B	3.0 V	LEV1V: reset request
0010 _B	3.1 V	
0011 _B	3.2 V	
0100 _B	3.3 V	
0101 _B	3.4 V	
0110 _B	3.6 V	
0111 _B	4.0 V	
1000 _B	4.2 V	
1001 _B	4.5 V	LEV2V: no request
1010 _B	4.6 V	
1011 _B	4.7 V	
1100 _B	4.8 V	
1101 _B	4.9 V	
1110 _B	5.0 V	
1111 _B	5.5 V	

Table 21 Coding of bit fields LEVxV in Register SWDCON0

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B	0.95 V	
001 _B	1.05 V	
010 _B	1.15 V	
011 _B	1.25 V	
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B	1.55 V	
111 _B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.



4.6 AC Parameters

These parameters describe the dynamic behavior of the XC226xM.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).



Figure 17 Input Output Waveforms







Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Variable Memory Cycles

External bus cycles of the XC226xM are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 29	Programmable Bus Cv	vcle Phases (see timino	diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase $(1 \dots 2 \text{ TCS})$ can be extended by $0 \dots 3 \text{ TCS}$ if the address window is changed	tpAB	1 2 (5)	TCS
Command delay phase	tpC	03	TCS
Write Data setup/MUX Tristate phase	tpD	0 1	TCS
Access phase	tpE	1 32	TCS
Address/Write Data hold phase	tpF	03	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply; $C_L = 20 \text{ pF}$.



Table 31 EBC External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
$\frac{\text{Output valid delay for }\overline{\text{RD}},}{\text{WR}(\text{L/H})}$	<i>t</i> ₁₀ CC	-	11	20	ns	
Output valid delay for BHE, ALE	<i>t</i> ₁₁ CC	-	10	21	ns	
Address output valid delay for A23 A0	<i>t</i> ₁₂ CC	-	11	22	ns	
Address output valid delay for AD15 AD0 (MUX mode)	<i>t</i> ₁₃ CC	-	10	22	ns	
Output valid delay for CS	<i>t</i> ₁₄ CC	-	10	13	ns	
Data output valid delay for AD15 AD0 (write data, MUX mode)	<i>t</i> ₁₅ CC	-	10	22	ns	
Data output valid delay for D15 D0 (write data, DEMUX mode)	<i>t</i> ₁₆ CC	-	10	22	ns	
$\frac{\text{Output hold time for } \overline{\text{RD}},}{\text{WR}(L/H)}$	<i>t</i> ₂₀ CC	-2	8	10	ns	
Output hold time for BHE, ALE	<i>t</i> ₂₁ CC	-2	8	10	ns	
Address output hold time for AD15 AD0	<i>t</i> ₂₃ CC	-3	8	10	ns	
Output hold time for CS	t ₂₄ CC	-3	8	11	ns	
Data output hold time for D15 D0 and AD15 AD0	<i>t</i> ₂₅ CC	-3	8	10	ns	
Input setup time for READY, D15 D0, AD15 AD0	<i>t</i> ₃₀ SR	29	17	-	ns	
Input hold time READY, D15 D0, AD15 AD0 ¹⁾	<i>t</i> ₃₁ SR	0	-9	-	ns	

 Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.



Electrical Parameters



Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.



Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
TCK clock period	t ₁ SR	50 ¹⁾	-	-	ns	2)
TCK high time	t_2 SR	16	-	-	ns	
TCK low time	t ₃ SR	16	-	-	ns	
TCK clock rise time	t_4 SR	-	-	8	ns	
TCK clock fall time	t ₅ SR	_	-	8	ns	
TDI/TMS setup to TCK rising edge	t ₆ SR	6	-	-	ns	
TDI/TMS hold after TCK rising edge	t ₇ SR	6	-	-	ns	
TDO valid from TCK falling edge (propagation delay) ³⁾	t ₈ CC	_	25	29	ns	
TDO high impedance to valid output from TCK falling edge ⁴⁾³⁾	<i>t</i> ₉ CC	_	25	29	ns	
TDO valid output to high impedance from TCK falling edge ³⁾	<i>t</i> ₁₀ CC	-	25	29	ns	
TDO hold after TCK falling edge ³⁾	<i>t</i> ₁₈ CC	5	_	_	ns	

Table 38JTAG Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \ge t_{SYS}$.

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.