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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4/M4F
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4cmp32ca-au

5.1.5.4 Wake-up, Anti-tamper and RTCOUT0 Pins

In all power supply figures shown above, if generic wake-up pins other than WKUP0/TMP0 are used either as a wake-up or a fast startup input, or as anti-tamper inputs, VDDIO must be present. This also applies to the RTCOUT0 pin.

5.1.5.5 General-purpose IO (GPIO) State in Low-power Modes

In dual-power supply schemes shown in Figure 5-3 and Figure 5-4, where Backup or Wait mode must be used, configuration of the GPIO lines is maintained in the same state as before entering Backup or Wait mode. Thus, to avoid extra current consumption on the VDDIO power rail, the user must configure the GPIOs either as an input with pull-up or pull-down enabled, or as an output with low or high level to comply with external components.

5.1.5.6 Default General-purpose IOs (GPIO) State after Reset

The reset state of the GPIO lines after reset is given in Table 11-5 “Multiplexing on PIO Controller A (PIOA)”, Section 11-6 “Multiplexing on PIO Controller B (PIOB)” and Table 11-7 “Multiplexing on PIO Controller C (PIOC)”. For further details about the GPIO and system lines, wake-up sources and wake-up time, and typical power consumption in different low-power modes, refer to Table 5-2 “Low-power Mode Configuration Summary”.

5.2 Clock System Overview

Figure 5-5 illustrates the typical operation of the whole SAM4CM clock system in case of single crystal (32.768 kHz) applications. Note:

- The 32 kHz crystal oscillator can be the source clock of the 8 MHz digital PLL (PLLA).
- The 8 MHz clock can feed the high frequency PLL (PLLB) input.
- The output of the PLLB can be used as a main clock for both cores and the peripherals.

Full details of the clock system are provided in Section 29. “Clock Generator” and Section 30. “Power Management Controller (PMC)”.

7. Configure PA30/PA31 (XIN/XOUT) into PIO mode according to their use.
8. Disable the JTAG lines using the SFR1 register in Matrix 0 (by default, internal pull-up or pull-down is disabled on JTAG lines).
9. Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR)[2].
10. Set the Flash Wait State (FWS) bit in the EEFC Flash Mode Register to 0.
11. Select one of the following methods to complete the sequence:
    a. To enter Wait mode using the WAITMODE bit:
        - Set the WAITMODE bit to 1 in the PMC Main Oscillator Register (CKGR_MOR).
        - Wait for Master Clock Ready MCKRDY = 1 in the PMC Status Register (PMC_SR).
    b. To enter Wait mode using the WFE instruction:
        - Select the 4/8/12 MHz fast RC Oscillator as Main Clock.
        - Set the FLPM field in the PMC Fast Startup Mode Register (PMC_FSMR).
        - Set Flash Wait State at 0.
        - Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR).
        - Write a 0 to the SLEEPDEEP bit of the Cortex-M4 processor.
        - Execute the Wait-For-Event (WFE) instruction of the processor.

Notes:
1. Any frequency can be chosen. The 12 MHz frequency will provide a faster start-up compared to the 4 MHz, but with the increased current consumption (in the µA range). Refer to Section 46. “Electrical Characteristics”.
2. Depending on the Flash Low-power Mode (FLPM) value, the Flash enters three different modes:
    - If FLPM = 0, the Flash enters Stand-by mode (Low consumption)
    - If FLPM = 1, the Flash enters Deep Power-down mode (Extra low consumption)
    - If FLPM = 2, the Flash enters Idle mode. Memory is ready for Read access

Whether the WAITMODE bit or the WFE instruction was used to enter Wait mode, the system exits Wait mode if one of the following enabled wake-up events occurs:

- WKUP[0–13] pins in Fast wake-up mode
- Anti-tamper event detection
- RTC alarm
- RTT alarm

After exiting Wait mode, the PIO controller has the same configuration state as before entering Wait mode. The SAM4CM is clocked back to the RC oscillator frequency which was used before entering Wait mode. The core will start fetching from Flash at this frequency. Depending on the configuration of the Flash Low-power Mode (FLPM) bits used to enter Wait mode, the application has to reconfigure it back to Read-idle mode.

5.5.3 Sleep Mode

The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clocks of CM4P0 and/or CM4P1 are stopped. Some of the peripheral clocks can be enabled depending on the application needs. The current consumption in this mode is application dependent. This mode is entered using Wait for Interrupt (WFI) or Wait for Event (WFE) instructions of the Cortex-M4.

The processor can be awakened from an interrupt if the WFI instruction of the Cortex-M4 is used to enter Sleep mode, or from a wake-up event if the WFE instruction is used. The WFI instruction can also be used to enter Sleep mode with the SLEEPONEXIT bit set to 1 in the System Control Register (SCB_SCR) of the Cortex-M. If the SLEEPONEXIT bit of the SCB_SCR is set to 1, when the processor completes the execution of an exception handler, it returns to Thread mode and immediately enters Sleep mode. This mechanism can be used in applications that require the processor to run only when an exception occurs. Setting the SLEEPONEXIT bit to 1 enables an interrupt-driven application in order to avoid returning to an empty main application.

12.6.12.6 MRS

Move the contents of a special register to a general-purpose register.

Syntax

```
MRS{cond} Rd, spec_reg
```

where:

cond — is an optional condition code, see “Conditional Execution”.

Rd — is the destination register.

spec_reg — can be any of: APSR, IPSR, EPSR, IEPSR, IAPSR, EAPSR, PSR, MSP, PSP, PRIMASK, BASEPRI, BASEPRI_MAX, FAULTMASK, or CONTROL.

Operation

Use MRS in combination with MSR as part of a read-modify-write sequence for updating a PSR, for example to clear the Q flag.

In process swap code, the programmers model state of the process being swapped out must be saved, including relevant PSR contents. Similarly, the state of the process being swapped in must also be restored. These operations use MRS in the state-saving instruction sequence and MSR in the state-restoring instruction sequence.

Note: BASEPRI_MAX is an alias of BASEPRI when used with the MRS instruction.

See “MSR”.

Restrictions

Rd must not be SP and must not be PC.

Condition Flags

This instruction does not change the flags.

Examples

```
MRS  R0, PRIMASK ; Read PRIMASK value and write it to R0
```

12.6.12.7 MSR

Move the contents of a general-purpose register into the specified special register.

Syntax

```
MSR{cond} spec_reg, Rn
```

where:

cond — is an optional condition code, see “Conditional Execution”.

Rn — is the source register.

spec_reg — can be any of: APSR, IPSR, EPSR, IEPSR, IAPSR, EAPSR, PSR, MSP, PSP, PRIMASK, BASEPRI, BASEPRI_MAX, FAULTMASK, or CONTROL.

17.6.1 RTC Control Register

Name: RTC_CR

Address: 0x400E1460

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	CALEVSEL	
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TIMEVSEL	
7	6	5	4	3	2	1	0
–	–	–	–	–	–	UPDCAL	UPDTIM

This register can only be written if the WPEN bit is cleared in the RTC Write Protection Mode Register.

- **UPDTIM: Update Request Time Register**

0: No effect or, if UPDTIM has been previously written to 1, stops the update procedure.

1: Stops the RTC time counting.

Time counting consists of second, minute and hour counters. Time counters can be programmed once this bit is set and acknowledged by the bit ACKUPD of the RTC_SR.

- **UPDCAL: Update Request Calendar Register**

0: No effect or, if UPDCAL has been previously written to 1, stops the update procedure.

1: Stops the RTC calendar counting.

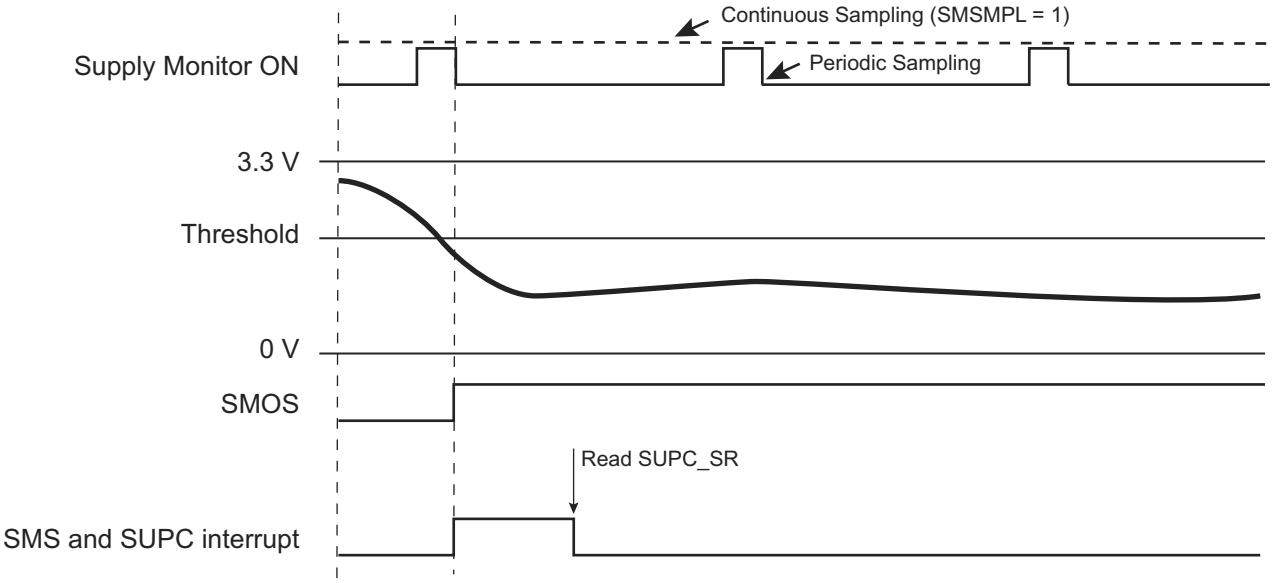
Calendar counting consists of day, date, month, year and century counters. Calendar counters can be programmed once this bit is set and acknowledged by the bit ACKUPD of the RTC_SR.

- **TIMEVSEL: Time Event Selection**

The event that generates the flag TIMEV in RTC_SR depends on the value of TIMEVSEL.

Value	Name	Description
0	MINUTE	Minute change
1	HOUR	Hour change
2	MIDNIGHT	Every day at midnight
3	NOON	Every day at noon

Figure 20-2. Supply Monitor Status Bit and Associated Interrupt



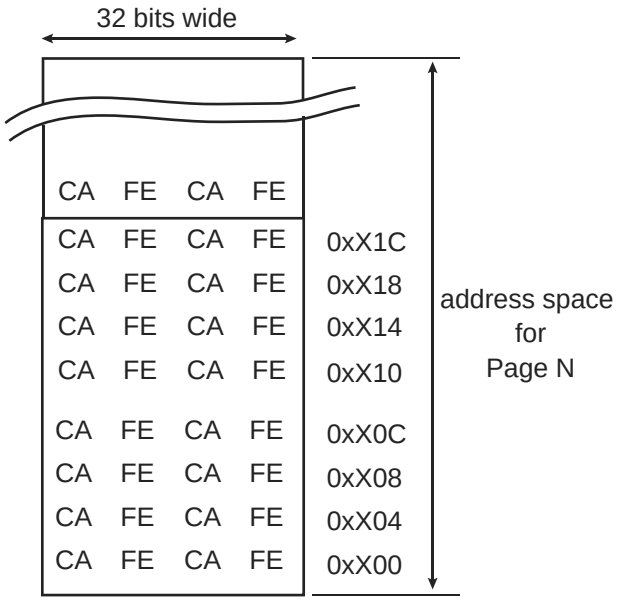
20.4.7 Backup Power Supply Reset

20.4.7.1 Raising the Backup Power Supply

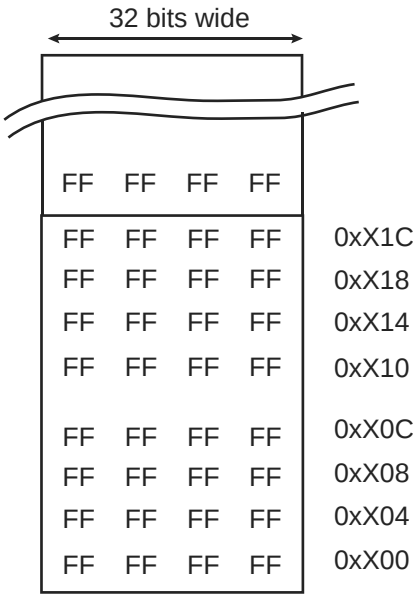
As soon as the backup voltage VDDBU_SW rises, the 32 kHz RC oscillator is powered up and the zero-power power-on reset cell maintains its output low as long as VDDBU_SW has not reached its target voltage. During this time, the SUPC is reset. When the VDDBU_SW voltage becomes valid and zero-power power-on reset signal is released, a counter is started for five slow clock cycles. This is the period required for the 32 kHz RC oscillator to stabilize.

After this time, the SHDN pin is asserted high and the core voltage regulator is enabled. The core power supply rises and the brownout detector provides the core regulator status as soon as the core voltage VDDCORE is valid. The system reset signal is then released to the Reset Controller after the core voltage status has been confirmed as being valid for at least one slow clock cycle.

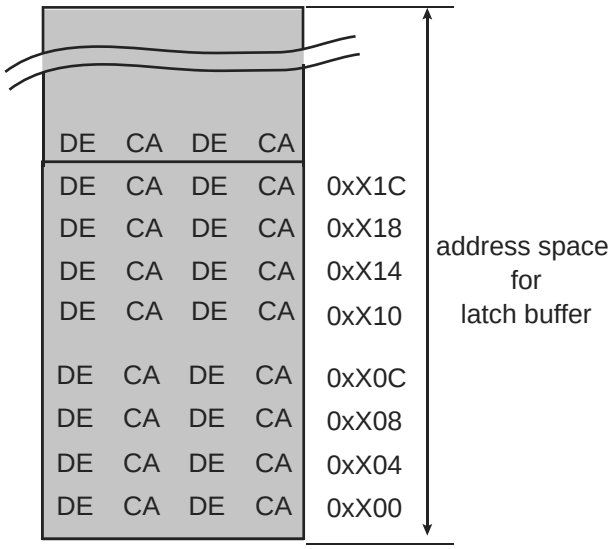
Figure 22-8. Full Page Programming



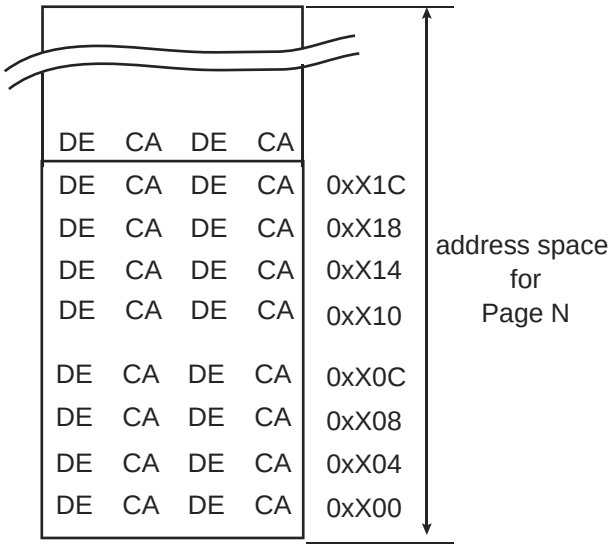
Before programming: Unerased page in Flash array



Step 1: Flash array after page erase



Step 2: Writing a page in the latch buffer



Step 3: Page in Flash array after issuing WP command and FRDY=1

31.3.2 Chip ID Extension Register

Name: CHIPID_EXID

Address: 0x400E0744

Access: Read-only

31	30	29	28	27	26	25	24
EXID							

23	22	21	20	19	18	17	16
EXID							

15	14	13	12	11	10	9	8
EXID							

7	6	5	4	3	2	1	0
EXID							

- **EXID: Chip ID Extension**

This field is cleared if CHIPID_CIDR.EXT = 0.

Value	Name	Description
0x1	SAM4CMP	SAM4C + 3-phase EMAFE
0x2	SAM4CMS	SAM4C + 2-phase EMAFE

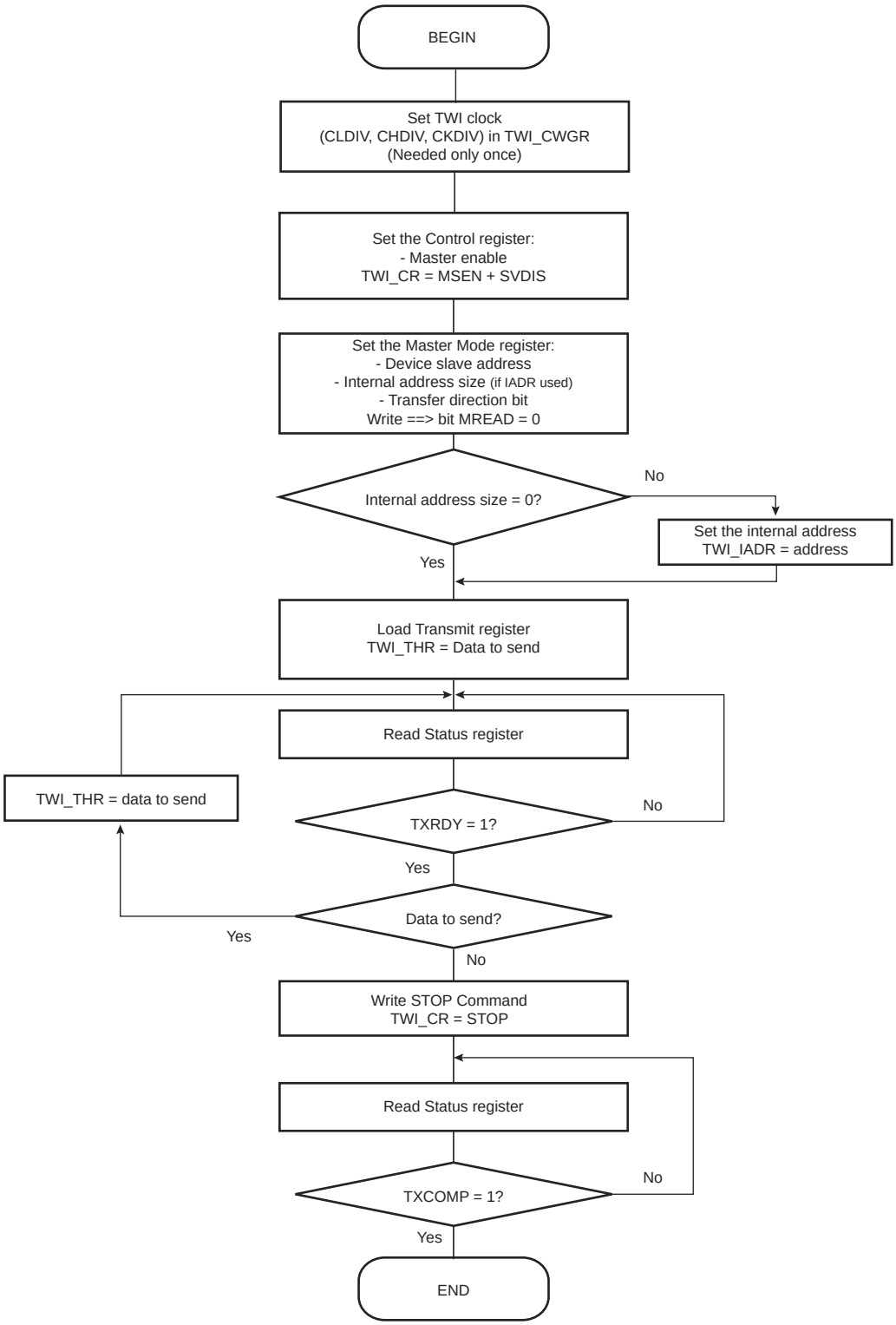
32.6 Parallel Input/Output Controller (PIO) User Interface

Each I/O line controlled by the PIO Controller is associated with a bit in each of the PIO Controller User Interface registers. Each register is 32-bit wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero. If the I/O line is not multiplexed with any peripheral, the I/O line is controlled by the PIO Controller and PIO_PSR returns one systematically.

Table 32-4. Register Mapping

Offset	Register	Name	Access	Reset
0x0000	PIO Enable Register	PIO_PER	Write-only	–
0x0004	PIO Disable Register	PIO_PDR	Write-only	–
0x0008	PIO Status Register	PIO_PSR	Read-only	(1)
0x000C	Reserved	–	–	–
0x0010	Output Enable Register	PIO_OER	Write-only	–
0x0014	Output Disable Register	PIO_ODR	Write-only	–
0x0018	Output Status Register	PIO_OSR	Read-only	0x00000000
0x001C	Reserved	–	–	–
0x0020	Glitch Input Filter Enable Register	PIO_IFER	Write-only	–
0x0024	Glitch Input Filter Disable Register	PIO_IFDR	Write-only	–
0x0028	Glitch Input Filter Status Register	PIO_IFSR	Read-only	0x00000000
0x002C	Reserved	–	–	–
0x0030	Set Output Data Register	PIO_SODR	Write-only	–
0x0034	Clear Output Data Register	PIO_CODR	Write-only	
0x0038	Output Data Status Register	PIO_ODSR	Read-only or(2) Read/Write	–
0x003C	Pin Data Status Register	PIO_PDSR	Read-only	(3)
0x0040	Interrupt Enable Register	PIO_IER	Write-only	–
0x0044	Interrupt Disable Register	PIO_IDR	Write-only	–
0x0048	Interrupt Mask Register	PIO_IMR	Read-only	0x00000000
0x004C	Interrupt Status Register(4)	PIO_ISR	Read-only	0x00000000
0x0050	Multi-driver Enable Register	PIO_MDER	Write-only	–
0x0054	Multi-driver Disable Register	PIO_MDDR	Write-only	–
0x0058	Multi-driver Status Register	PIO_MDSR	Read-only	0x00000000
0x005C	Reserved	–	–	–
0x0060	Pull-up Disable Register	PIO_PUDR	Write-only	–
0x0064	Pull-up Enable Register	PIO_PUER	Write-only	–
0x0068	Pad Pull-up Status Register	PIO_PUSR	Read-only	(1)
0x006C	Reserved	–	–	–

Figure 34-17. TWI Write Operation with Multiple Data Bytes with or without Internal Address



35.6.3 UART Interrupt Enable Register

Name: UART_IER

Address: 0x400E0608 (0), 0x48004008 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	RXBUFF	TXBUFE	–	TXEMPTY	–
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	–	TXRDY	RXRDY

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

- **RXRDY: Enable RXRDY Interrupt**
- **TXRDY: Enable TXRDY Interrupt**
- **ENDRX: Enable End of Receive Transfer Interrupt**
- **ENDTX: Enable End of Transmit Interrupt**
- **OVRE: Enable Overrun Error Interrupt**
- **FRAME: Enable Framing Error Interrupt**
- **PARE: Enable Parity Error Interrupt**
- **TXEMPTY: Enable TXEMPTY Interrupt**
- **TXBUFE: Enable Buffer Empty Interrupt**
- **RXBUFF: Enable Buffer Full Interrupt**

- **CPOL: SPI Clock Polarity**

Applicable if USART operates in SPI mode (slave or master, USART_MODE = 0xE or 0xF):

0: The inactive state value of SPCK is logic level zero.

1: The inactive state value of SPCK is logic level one.

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with CPHA to produce the required clock/data relationship between master and slave devices.

- **CLKO: Clock Output Select**

0: The USART does not drive the SCK pin.

1: The USART drives the SCK pin if USCLKS does not select the external clock SCK.

- **WRDBT: Wait Read Data Before Transfer**

0: The character transmission starts as soon as a character is written into US_THR (assuming TXRDY was set).

1: The character transmission starts when a character is written and only if RXRDY flag is cleared (Receive Holding Register has been read).

36.7.15 USART Baud Rate Generator Register

Name: US_BRGR

Address: 0x40024020 (0), 0x40028020 (1), 0x4002C020 (2), 0x40030020 (3), 0x40034020 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	FP		

15	14	13	12	11	10	9	8
CD							

7	6	5	4	3	2	1	0
CD							

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

- **CD: Clock Divider**

	USART_MODE ≠ ISO7816			
	SYNC = 0		**SYNC = 1 or USART_MODE = SPI (Master or Slave)**	**USART_MODE = ISO7816**
CD	**OVER = 0**	**OVER = 1**		
0	Baud Rate Clock Disabled			
1 to 65535	CD = Selected Clock / (16 × Baud Rate)	CD = Selected Clock / (8 × Baud Rate)	CD = Selected Clock / Baud Rate	CD = Selected Clock / (FI_DI_RATIO × Baud Rate)

- **FP: Fractional Part**

0: Fractional divider is disabled.

1–7: Baud rate resolution, defined by FP × 1/8.

36.7.21 USART Manchester Configuration Register

Name: US_MAN

Address: 0x40024050 (0), 0x40028050 (1), 0x4002C050 (2), 0x40030050 (3), 0x40034050 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	DRIFT	ONE	RX_MPOL	–	–	RX_PP	

23	22	21	20	19	18	17	16
–	–	–	–	RX_PL			

15	14	13	12	11	10	9	8
–	–	–	TX_MPOL	–	–	TX_PP	

7	6	5	4	3	2	1	0
–	–	–	–	TX_PL			

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

- **TX_PL: Transmitter Preamble Length**

0: The transmitter preamble pattern generation is disabled

1–15: The preamble length is TX_PL × Bit Period

- **TX_PP: Transmitter Preamble Pattern**

The following values assume that TX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

- **TX_MPOL: Transmitter Manchester Polarity**

0: Logic zero is coded as a zero-to-one transition, Logic one is coded as a one-to-zero transition.

1: Logic zero is coded as a one-to-zero transition, Logic one is coded as a zero-to-one transition.

- **RX_PL: Receiver Preamble Length**

0: The receiver preamble pattern detection is disabled

1–15: The detected preamble length is RX_PL × Bit Period

- **RX_PP: Receiver Preamble Pattern detected**

The following values assume that RX_MPOL field is not set:

Value	Name	Description
00	ALL_ONE	The preamble is composed of ‘1’s
01	ALL_ZERO	The preamble is composed of ‘0’s
10	ZERO_ONE	The preamble is composed of ‘01’s
11	ONE_ZERO	The preamble is composed of ‘10’s

37. Timer Counter (TC)

37.1 Description

A Timer Counter (TC) module includes three identical TC channels. The number of implemented TC modules is device-specific.

Each TC channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each channel has three external clock inputs, five internal clock inputs and two multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

The TC embeds a quadrature decoder (QDEC) connected in front of the timers and driven by TIOA0, TIOB0 and TIOB1 inputs. When enabled, the QDEC performs the input lines filtering, decoding of quadrature signals and connects to the timers/counters in order to read the position and speed of the motor through the user interface.

The TC block has two global registers which act upon all TC channels:

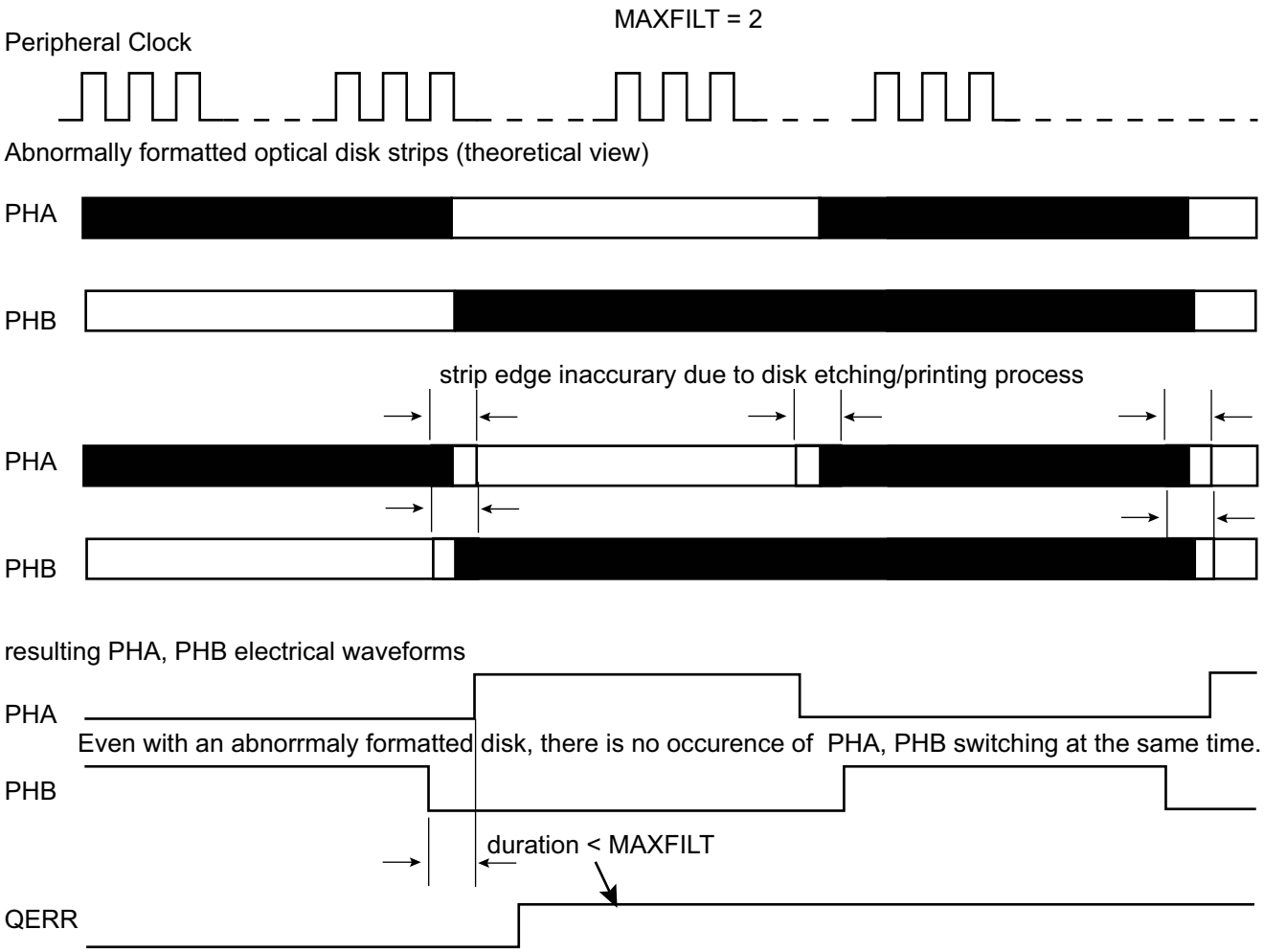
- Block Control Register (TC_BCR)—allows channels to be started simultaneously with the same instruction
- Block Mode Register (TC_BMR)—defines the external clock inputs for each channel, allowing them to be chained

37.2 Embedded Characteristics

- Total number of TC channels: three
- TC channel size: 16-bit
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
  - Quadrature decoder
  - 2-bit gray up/down count for stepper motor
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five Internal clock inputs
  - Two multi-purpose input/output signals acting as trigger event
- Internal interrupt signal
- Register Write Protection

configurable and corresponds to (MAXFILT + 1) × $t_{peripheral\ clock}$ ns. After being filtered there is no reason to have two edges closer than (MAXFILT + 1) × $t_{peripheral\ clock}$ ns under normal mode of operation.

Figure 37-19. Quadrature Error Detection



MAXFILT must be tuned according to several factors such as the peripheral clock frequency, type of rotary sensor and rotation speed to be achieved.

37.6.14.4 Position and Rotation Measurement

When the POSEN bit is set in the TC_BMR, the motor axis position is processed on channel 0 (by means of the PHA, PHB edge detections) and the number of motor revolutions are recorded on channel 1 if the IDX signal is provided on the TIOB1 input. The position measurement can be read in the TC_CV0 register and the rotation measurement can be read in the TC_CV1 register.

Channel 0 and 1 must be configured in Capture mode (TC_CMR0.WAVE = 0). ‘Rising edge’ must be selected as the External Trigger Edge (TC_CMR.ETRGEDG = 0x01) and ‘TIOA’ must be selected as the External Trigger (TC_CMR.ABETRG = 0x1).

In parallel, the number of edges are accumulated on timer/counter channel 0 and can be read on the TC_CV0 register.

Therefore, the accurate position can be read on both TC_CV registers and concatenated to form a 32-bit word.

The timer/counter channel 0 is cleared for each increment of IDX count value.

Values which are not listed in the table must be considered as “reserved”.

If a PDC transfer is used, configure SMOD to 0x2. Refer to Section 42.4.4.3 “PDC Mode” for more details.

- **KEYSIZE: Key Size**

Value	Name	Description
0	AES128	AES Key Size is 128 bits
1	AES192	AES Key Size is 192 bits
2	AES256	AES Key Size is 256 bits

Values which are not listed in the table must be considered as “reserved”.

- **OPMOD: Operation Mode**

Value	Name	Description
0	ECB	ECB: Electronic Code Book mode
1	CBC	CBC: Cipher Block Chaining mode
2	OFB	OFB: Output Feedback mode
3	CFB	CFB: Cipher Feedback mode
4	CTR	CTR: Counter mode (16-bit internal counter)
5	GCM	GCM: Galois/Counter mode

Values which are not listed in the table must be considered as “reserved”.

For CBC-MAC operating mode, set OPMOD to CBC and LOD to 1.

- **LOD: Last Output Data Mode**

0: No effect.

After each end of encryption/decryption, the output data are available either on the output data registers (Manual and Auto modes) or at the address specified in the Receive Pointer Register (AES_RPR) for PDC mode.

In Manual and Auto modes, the DATRDY flag is cleared when at least one of the Output Data registers is read.

1: The DATRDY flag is cleared when at least one of the Input Data Registers is written.

No more Output Data Register reads is necessary between consecutive encryptions/decryptions (see Section 42.4.5 “Last Output Data Mode”).

Warning: In PDC mode, reading to the Output Data registers before the last data encryption/decryption process may lead to unpredictable results.

- **CFBS: Cipher Feedback Data Size**

Value	Name	Description
0	SIZE_128BIT	128-bit
1	SIZE_64BIT	64-bit
2	SIZE_32BIT	32-bit
3	SIZE_16BIT	16-bit
4	SIZE_8BIT	8-bit

Values which are not listed in table must be considered as “reserved”.

43.6.1 ICM Configuration Register

Name: ICM_CFG

Address: 0x40044000

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	DAPROT					
23	22	21	20	19	18	17	16
–	–	HAPROT					
15	14	13	12	11	10	9	8
UALGO			UIHASH	–	–	DUALBUFF	ASCD
7	6	5	4	3	2	1	0
BBC				–	SLBDIS	EOMDIS	WBDIS

- **WBDIS: Write Back Disable**

0: Write Back Operations are permitted.

1: Write Back Operations are forbidden. Context register CDWBN bit is internally set to one and cannot be modified by a linked list element. The CDWBN bit of the ICM_RCFG structure member has no effect.

When ASCD bit of the ICM_CFG register is set, WBDIS bit value has no effect.

- **EOMDIS: End of Monitoring Disable**

0: End of Monitoring is permitted

1: End of Monitoring is forbidden. The EOM bit of the ICM_RCFG structure member has no effect.

- **SLBDIS: Secondary List Branching Disable**

0: Branching to the Secondary List is permitted.

1: Branching to the Secondary List is forbidden. The NEXT field of the ICM_RNEXT structure member has no effect and is always considered as zero.

- **BBC: Bus Burden Control**

This field is used to control the burden of the ICM system bus. The number of system clock cycles between the end of the current processing and the next block transfer is set to 2^{BBC}. Up to 32,768 cycles can be inserted.

- **ASCD: Automatic Switch To Compare Digest**

0: Automatic mode is disabled.

1: When this mode is enabled, the ICM controller automatically switches to active monitoring after the first Main List pass. Both CDWBN and WBDIS bits have no effect. A one must be written to the EOM bit in ICM_RCFG to terminate the monitoring.

- **DUALBUFF: Dual Input Buffer**

0: Dual Input buffer mode is disabled.

1: Dual Input buffer mode is enabled.

43.6.10 ICM Hash Area Start Address Register

Name: ICM_HASH

Address: 0x40044034

Access: Read/Write

31	30	29	28	27	26	25	24
HASA							
23	22	21	20	19	18	17	16
HASA							
15	14	13	12	11	10	9	8
HASA							
7	6	5	4	3	2	1	0
HASA	–	–	–	–	–	–	–

- **HASA: Hash Area Start Address**

This field points at the Hash memory location. The address must be a multiple of 128 bytes.

Table 46-4. Recommended Operating Conditions on Power Supply Inputs at Powerup

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RR_{VDDBU}	Rise Rate on VDDBU	(1)	660	–	300k	V/s
V_{ST_VDDBU}	VDDBU voltage at powerup	(1)	3.0	–	–	V
V_{ST_VDDIO}	VDDIO and VDDIN voltage at powerup	–	3.0	–	–	V
V_{VDDIO_VDDBU}	Voltage on VDDIO and VDDIN while VDDBU < 1.6V	(1)	–	–	V_{VDDBU}	V
RR_{VDDIO}	Rise Rate on VDDIO and VDDIN	–	330	–	300k	V/s

Note: 1. Applies whenever VDDBU is restarted from below 1.35V.

46.2.3 Recommended Operating Conditions on Input Pins

Table 46-5. Recommended Operating Conditions on Input Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$AD[x]_{IN}$	Input voltage range on 10-bit ADC analog inputs	On AD[0..x]	0	–	Min (VDDIN, VDDIO)	V
$EMAFE_{IN}$	Input voltage range on EMAFE input pins	On $I_{P\{0,1,2,3\}}$, $I_{N\{0,1,2,3\}}$ and $V_{P\{1,2,3\}}$	-0.25	–	0.25	V
V_{GPIO_IN}	Input voltage range on GPIOs referenced to VDDIO	On any pin configured as a digital input	0	–	VDDIO	V
V_{VDDBU_IN}	Input voltage range on inputs referenced to VDDBU	On FWUP, TMP0 and XIN32 inputs	0	–	VDDBU	V

46.2.4 Recommended Thermal Operating Conditions

Table 46-6. Recommended Thermal Operating Conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_A	Ambient temperature range	–		-40	–	+85	°C
T_J	Junction temperature range	–		-40	–	100	
R_{JA}	Junction-to-ambient thermal resistance	LQFP100 (SAM4CM16/8/4)		–	43	–	°C/W
		LQFP100 (SAM4CM32)		–	41	–	
P_D	Power dissipation	LQFP100 (SAM4CM16/8/4)	T_A = 70°C	–	–	700	mW
			T_A = 85°C	–	–	350	
		LQFP100 (SAM4CM32)	T_A = 70°C	–	–	730	
			T_A = 85°C	–	–	365	

46.3 Electrical Parameters Usage

The tables that follow further on in Section 46.4 “I/O Characteristics”, Section 46.5 “Embedded Analog Peripherals Characteristics”, Section 46.6 “Embedded Flash Characteristics”, and Section 46.7 “Power Supply Current Consumption” define the limiting values for several electrical parameters. Unless otherwise noted, these values are valid over the ambient temperature range T_A= [-40°C + 85°C]. Note that these limits may be affected by the board on which the MCU is mounted. Particularly, noisy supply and ground conditions must be avoided and care must be taken to provide:

- a PCB with a low impedance ground plane (unbroken ground planes are strongly recommended)

Table 46-30 summarizes recommendations for 32.768 kHz crystal selection.

Table 46-30. Recommended Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor ($R_{S)}$	Crystal @ 32.768 kHz	–	50	100	kΩ
C_M	Motional capacitance	Crystal @ 32.768 kHz	0.6	–	3	fF
C_{SHUNT}	Shunt capacitance	Crystal @ 32.768 kHz	0.6	–	2	pF

46.5.12 3- to 20-MHz Crystal Oscillator

Table 46-31. 3- to 20-MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDIO}	Supply voltage range (VDDIO)	–	1.62	3.3	3.6	V
V_{DDPLL}	Supply voltage range (VDDPLL)	–	1.08	1.2	1.32	V
f_{OSC}	Operating frequency range	Normal mode with crystal	3	16	20	MHz
Duty	Duty cycle	–	40	50	60	%
t_{ON}	Start-up time	3 MHz, C_{SHUNT} = 3pF 8 MHz, C_{SHUNT} = 7pF 16 MHz, C_{SHUNT} = 7pF with C_M = 8 fF 16 MHz, C_{SHUNT} = 7pF with C_M = 1.6 fF 20 MHz, C_{SHUNT} = 7pF	–	–	14.5 4 1.4 2.5 1	ms
I_{DD_ON}	Current consumption On VDDIO	3 MHz(1) 8 MHz(2) 16 MHz(3) 20 MHz(4)	–	230 300 390 450	350 400 470 560	µA
	On VDDPLL	3 MHz(1) 8 MHz(2) 16 MHz(3) 20 MHz(4)		6 12 20 24	7 14 23 30	
P_{ON}	Drive level	3 MHz 8 MHz 16 MHz, 20 MHz	–	–	15 30 50	µW
R_f	Internal resistor	Between XIN and XOUT	–	0.5	–	MΩ
$C_{CRYSTAL}$	Allowed crystal capacitive load	From crystal specification	12	–	18	pF
C_{LEXT}	External capacitor on XIN and XOUT	–	–	–	18	pF
C_{LINT}	Integrated load capacitance	Between XIN and XOUT	7.5	9.5	10.5	pF

Notes:
1. R_S = 100-200 Ohms; C_S = 2.0 - 2.5 pF; C_M = 2 – 1.5 fF(typ, worst case) using 1 kΩ serial resistor on XOUT.
2. R_S = 50-100 Ohms; C_S = 2.0 - 2.5 pF; C_M = 4 - 3 fF(typ, worst case).
3. R_S = 25-50 Ohms; C_S = 2.5 - 3.0 pF; C_M = 7 - 5 fF (typ, worst case).
4. R_S = 20-50 Ohms; C_S = 3.2 - 4.0 pF; C_M = 10 - 8 fF(typ, worst case).