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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4/M4F
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4cms16ca-au

Examples

```
SMUAD    R0, R4, R5  ; Multiplies bottom halfword of R4 with the bottom
                     ; halfword of R5, adds multiplication of top halfword
                     ; of R4 with top halfword of R5, writes to R0
SMUADX   R3, R7, R4  ; Multiplies bottom halfword of R7 with top halfword
                     ; of R4, adds multiplication of top halfword of R7
                     ; with bottom halfword of R4, writes to R3
SMUSD    R3, R6, R2  ; Multiplies bottom halfword of R4 with bottom halfword
                     ; of R6, subtracts multiplication of top halfword of R6
                     ; with top halfword of R3, writes to R3
SMUSDX   R4, R5, R3  ; Multiplies bottom halfword of R5 with top halfword of
                     ; R3, subtracts multiplication of top halfword of R5
                     ; with bottom halfword of R3, writes to R4.
```

12.6.6.10 SMUL and SMULW

Signed Multiply (halfwords) and Signed Multiply (word by halfword)

Syntax

op{*XY*}{*cond*} *Rd*,*Rn*, *Rm*
op{*Y*}{*cond*} *Rd*. *Rn*, *Rm*

For *SMULXY* only:

op is one of:

SMUL{*XY*} Signed Multiply (halfwords).

X and *Y* specify which halfword of the source registers *Rn* and *Rm* is used as the first and second multiply operand.
If *X* is B, then the bottom halfword, bits [15:0] of *Rn* is used.
If *X* is T, then the top halfword, bits [31:16] of *Rn* is used.If *Y* is B, then the bot tom halfword, bits [15:0], of *Rm* is used.
If *Y* is T, then the top halfword, bits [31:16], of *Rm* is used.

SMULW{Y} Signed Multiply (word by halfword).

Y specifies which halfword of the source register *Rm* is used as the second multiply operand.
If *Y* is B, then the bottom halfword (bits [15:0]) of *Rm* is used.
If *Y* is T, then the top halfword (bits [31:16]) of *Rm* is used.

cond is an optional condition code, see “Conditional Execution”.

Rd is the destination register.

Rn, Rm are registers holding the first and second operands.

Operation

The SMULBB, SMULTB, SMULBT and SMULTT instructions interprets the values from *Rn* and *Rm* as four signed 16-bit integers. These instructions:

- Multiplies the specified signed halfword, Top or Bottom, values from *Rn* and *Rm*.
- Writes the 32-bit result of the multiplication in *Rd.*

The SMULWT and SMULWB instructions interprets the values from *Rn* as a 32-bit signed integer and *Rm* as two halfword 16-bit signed integers. These instructions:

- Multiplies the first operand and the top, T suffix, or the bottom, B suffix, halfword of the second operand.
- Writes the signed most significant 32 bits of the 48-bit result in the destination register.

12.6.11.26 VSQRT

Floating-point Square Root.

Syntax

```
VSQRT{cond}.F32 Sd, Sm
```

where:

cond is an optional condition code, see “Conditional Execution”.

Sd is the destination floating-point value.

Sm is the operand floating-point value.

Operation

This instruction:

- Calculates the square root of the value in a floating-point register.
- Writes the result to another floating-point register.

Restrictions

There are no restrictions.

Condition Flags

These instructions do not change the flags.

It is not possible to switch directly between JTAG Boundary Scan and SWJ Debug Port operations. A chip reset must be performed after JTAGSEL is changed.

A Boundary-scan Descriptor Language (BSDL) file is provided on www.atmel.com to set up the test.

13.7.7.1 JTAG Boundary-scan Register

The Boundary-scan Register (BSR) contains a number of bits which correspond to active pins and the associated control signals.

Each SAM4 input/output pin corresponds to a 3-bit register in the BSR. The OUTPUT bit contains data that can be forced on the pad. The INPUT bit facilitates the observability of data applied to the pad. The CONTROL bit selects the direction of the pad.

For more information, refer to BDSL files available for the SAM4 Series.

17.6.11 RTC Interrupt Mask Register

Name: RTC_IMR

Address: 0x400E1488

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	TDERR	CAL	TIM	SEC	ALR	ACK

- **ACK: Acknowledge Update Interrupt Mask**

0: The acknowledge for update interrupt is disabled.

1: The acknowledge for update interrupt is enabled.

- **ALR: Alarm Interrupt Mask**

0: The alarm interrupt is disabled.

1: The alarm interrupt is enabled.

- **SEC: Second Event Interrupt Mask**

0: The second periodic interrupt is disabled.

1: The second periodic interrupt is enabled.

- **TIM: Time Event Interrupt Mask**

0: The selected time event interrupt is disabled.

1: The selected time event interrupt is enabled.

- **CAL: Calendar Event Interrupt Mask**

0: The selected calendar event interrupt is disabled.

1: The selected calendar event interrupt is enabled.

- **TDERR: Time and/or Date Error Mask**

0: The time and/or date error event is disabled.

1: The time and/or date error event is enabled.

25.5.4 IPC Interrupt Enable Command Register

Name: IPC_IECR

Address: 0x4004C00C (0), 0x4801400C (1)

Access: Write-only

31	30	29	28	27	26	25	24
IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24
23	22	21	20	19	18	17	16
IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16
15	14	13	12	11	10	9	8
IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8
7	6	5	4	3	2	1	0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0

- **IRQ0-IRQ31: Interrupt Enable**

0: No effect.

1: Enables the corresponding interrupt.

Table 26-5. List of Bus Matrix Slaves

Slave 0	Internal SRAM1
Slave 1	Internal SRAM2
Slave 2	External Bus Interface
Slave 3	Peripheral Bridge 1
Slave 4	Matrix0
Slave 5	CMCC1

26.2.2.3 Master to Slave Access (Matrix 1)

Table 26-6 gives valid paths for master to slave access on Matrix 1. The paths shown as "-" are forbidden or not wired, e.g. access from the Cortex-M4 S Bus to the Internal ROM.

Table 26-6. Matrix 1 Master to Slave Access

	Masters	0	1	2	3	4	5
Slaves		**Cortex-M4 I/D Bus**	**Cortex-M4 S Bus**	**PDC1**	**Matrix0**	**EBI Matrix 0**	**CMCC1**
0	Internal SRAM1	X	X	X	X	-	-
1	Internal SRAM2	-	X	X	X	-	-
2	External Bus Interface	X	X	X	-	X	X
3	Peripheral Bridge 1	-	X	X	X	-	-
4	Matrix0	X	X	-	-	-	X
5	CMCC1	X	-	-	-	-	-

26.2.2.4 Accesses through Matrix 1

- CM4P1 I/D Bus access to:
  - Flash (through 0x01000000 to 0x01FFFFFF)
  - EBI (through 0x03000000 to 0x06FFFFFF)
  - FLASH and EBI through Cache CMCC1
- CM4P1 S-Bus access to:
  - SRAM1, SRAM2, SRAM0 through Matrix0 (0x20000000),
  - EBI (0x60000000 to 0x63FFFFFF and 0xA0000000 to 0xA3FFFFFF),
  - HBRIDGE1, HBRIDGE0 through Matrix0 (0x40000000)
- PDC1 access to:
  - SRAM1, SRAM2
  - EBI (0x60000000 to 0x63FFFFFF),
  - HBRIDGE1
- Matrix0 access to:
  - SRAM1, SRAM2,
  - HBRIDGE1
- EBI from Matrix 0 access to:
  - EBI (through 0x030000000 to 0x06FFFFFFF, 0x60000000 to 0x63FFFFFF, 0xA0000000 to A3FFFFFF)

For read operations:

Null but positive setup and hold of address and NRD and/or NCS can not be guaranteed at the memory interface because of the propagation delay of theses signals through external logic and pads. If positive setup and hold values must be verified, then it is strictly recommended to program non-null values so as to cover possible skews between address, NCS and NRD signals.

For write operations:

If a null hold value is programmed on NWE, the SMC can guarantee a positive hold of address and NCS signal after the rising edge of NWE. This is true for WRITE_MODE = 1 only. See Section 27.11.2 ”Early Read Wait State”.

For read and write operations: a null value for pulse parameters is forbidden and may lead to unpredictable behavior.

In read and write cycles, the setup and hold time parameters are defined in reference to the address bus. For external devices that require setup and hold time between NCS and NRD signals (read), or between NCS and NWE signals (write), these setup and hold times must be converted into setup and hold times in reference to the address bus.

27.10 Scrambling/Unscrambling Function

The external data bus can be scrambled in order to prevent intellectual property data located in off-chip memories from being easily recovered by analyzing data at the package pin level of either microcontroller or memory device.

The scrambling and unscrambling are performed on-the-fly without additional wait states.

The scrambling/unscrambling function can be enabled or disabled by configuring the CSxSE bits in the SMC OCMS Mode Register (SMC_OCMS).

When multiple chip selects are handled, it is possible to configure the scrambling function per chip select using the CSxSE bits in the SMC_OCMS register.

The scrambling method depends on two user-configurable key registers, SMC_KEY1 and SMC_KEY2. These key registers are only accessible in Write mode.

The scrambling user key or the seed for key generation must be securely stored in a reliable non-volatile memory in order to recover data from the off-chip memory. Any data scrambled with a given key cannot be recovered if the key is lost.

27.11 Automatic Wait States

Under certain circumstances, the SMC automatically inserts idle cycles between accesses to avoid bus contention or operation conflict.

27.11.1 Chip Select Wait States

The SMC always inserts an idle cycle between two transfers on separate chip selects. This idle cycle ensures that there is no bus contention between the de-activation of one device and the activation of the next one.

During chip select wait state, all control lines are turned inactive: NWR, NCS[0..3], NRD lines are all set to 1.

Figure 27-15 illustrates a chip select wait state between access on Chip Select 0 and Chip Select 2.

- ENDTX flag is set when the PDC Transmit Counter Register (PERIPH_TCR) reaches zero.
- TXBUFE flag is set when both PERIPH_TCR and the PDC Transmit Next Counter Register (PERIPH_TNCR) reach zero.

These status flags are described in the Transfer Status Register (PERIPH_PTSR).

28.4.4 Data Transfers

The serial peripheral triggers its associated PDC channels' transfers using transmit enable (TXEN) and receive enable (RXEN) flags in the transfer control register integrated in the peripheral's user interface.

When the peripheral receives external data, it sends a Receive Ready signal to its PDC receive channel which then requests access to the Matrix. When access is granted, the PDC receive channel starts reading the peripheral Receive Holding register (RHR). The read data are stored in an internal buffer and then written to memory.

When the peripheral is about to send data, it sends a Transmit Ready to its PDC transmit channel which then requests access to the Matrix. When access is granted, the PDC transmit channel reads data from memory and transfers the data to the Transmit Holding register (THR) of its associated peripheral. The same peripheral sends data depending on its mechanism.

28.4.5 PDC Flags and Peripheral Status Register

Each peripheral connected to the PDC sends out receive ready and transmit ready flags and the PDC returns flags to the peripheral. All these flags are only visible in the peripheral's Status register.

Depending on whether the peripheral is half- or full-duplex, the flags belong to either one single channel or two different channels.

28.4.5.1 Receive Transfer End

The receive transfer end flag is set when PERIPH_RCR reaches zero and the last data has been transferred to memory.

This flag is reset by writing a non-zero value to PERIPH_RCR or PERIPH_RNCR.

28.4.5.2 Transmit Transfer End

The transmit transfer end flag is set when PERIPH_TCR reaches zero and the last data has been written to the peripheral THR.

This flag is reset by writing a non-zero value to PERIPH_TCR or PERIPH_TNCR.

28.4.5.3 Receive Buffer Full

The receive buffer full flag is set when PERIPH_RCR reaches zero, with PERIPH_RNCR also set to zero and the last data transferred to memory.

This flag is reset by writing a non-zero value to PERIPH_TCR or PERIPH_TNCR.

28.4.5.4 Transmit Buffer Empty

The transmit buffer empty flag is set when PERIPH_TCR reaches zero, with PERIPH_TNCR also set to zero and the last data written to peripheral THR.

This flag is reset by writing a non-zero value to PERIPH_TCR or PERIPH_TNCR.

Each wake-up input pin and alarm can be enabled to generate a fast startup event by setting the corresponding bit in PMC_FSMR.

The user interface does not provide any status for fast startup, but the user can easily recover this information by reading the PIO Controller and the status registers of the RTC and RTT.

30.11 Main Processor Startup from Embedded Flash

The inherent start-up time of the embedded Flash cannot provide a fast startup of the system.

If system fast start-up time is not required, the first instruction after a Wait mode exit can be located in the embedded Flash. Under these conditions, prior to entering Wait mode, the Flash controller must be programmed to perform access in 0 wait-state. Refer to Section 22. "Enhanced Embedded Flash Controller (EEFC)".

The procedure and conditions to enter Wait mode and the circuitry to exit Wait mode are strictly the same as fast startup (refer to Section 30.10 "Main Processor Fast Startup").

30.12 Coprocessor Sleep Mode

The coprocessor enters Sleep mode by executing the WaitForInterrupt (WFI) instruction of the coprocessor. Any enabled interrupt can wake the processor up.

30.13 Main Clock Failure Detector

The clock failure detector monitors the 3 to 20 MHz crystal oscillator or ceramic resonator-based oscillator to identify a failure of this oscillator when selected as main clock.

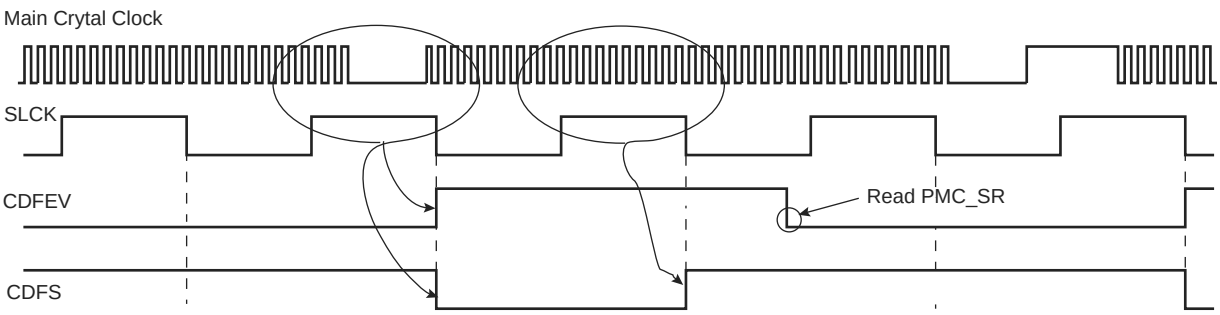
The clock failure detector can be enabled or disabled by bit CFDEN in CKGR_MOR. After a VDDCORE reset, the detector is disabled. However, if the oscillator is disabled (MOSCXTEN = 0), the detector is also disabled.

A failure is detected by means of a counter incrementing on the main clock and detection logic is triggered by the 32 kHz (typical) RC oscillator which is automatically enabled when CFDEN=1.

The counter is cleared when the 32 kHz (typical) RC oscillator clock signal is low and enabled when the signal is high. Thus, the failure detection time is one RC oscillator period. If, during the high level period of the 32 kHz (typical) RC oscillator clock signal, less than eight 3 to 20 MHz crystal oscillator clock periods have been counted, then a failure is reported.

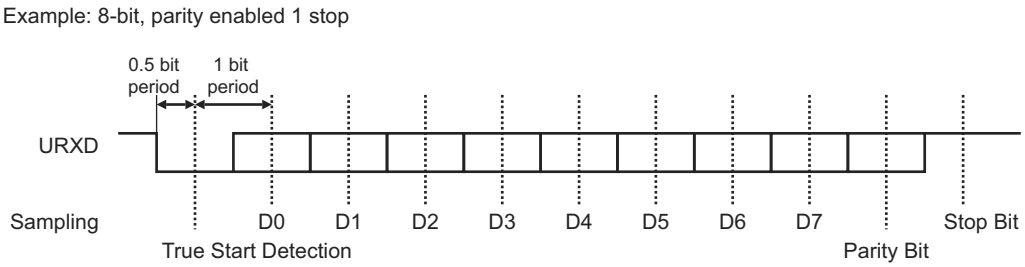
If a failure of the main clock is detected, bit CFDEV in PMC_SR indicates a failure event and generates an interrupt if the corresponding interrupt source is enabled. The interrupt remains active until a read occurs in PMC_SR. The user can know the status of the clock failure detection at any time by reading the CFDS bit in PMC_SR.

Figure 30-4. Clock Failure Detection (Example)



Note: ratio of clock periods is for illustration purposes only

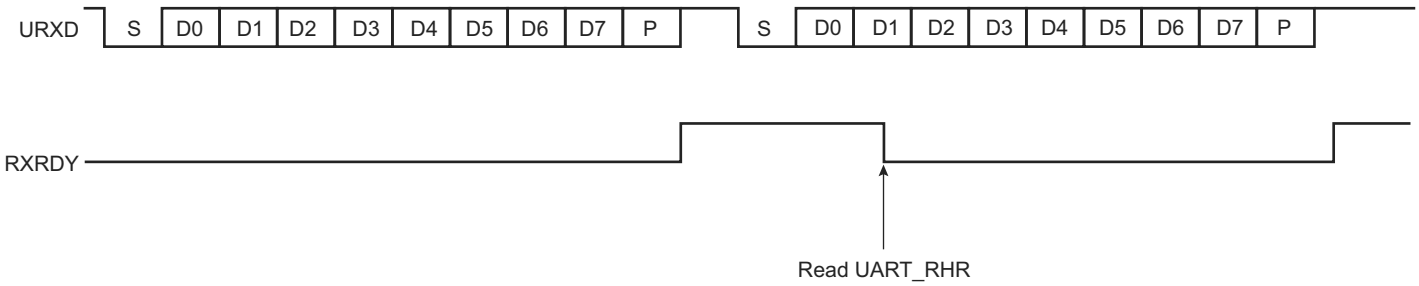
Figure 35-4. Character Reception



35.5.2.3 Receiver Ready

When a complete character is received, it is transferred to the Receive Holding Register (UART_RHR) and the RXRDY status bit in the Status Register (UART_SR) is set. The bit RXRDY is automatically cleared when UART_RHR is read.

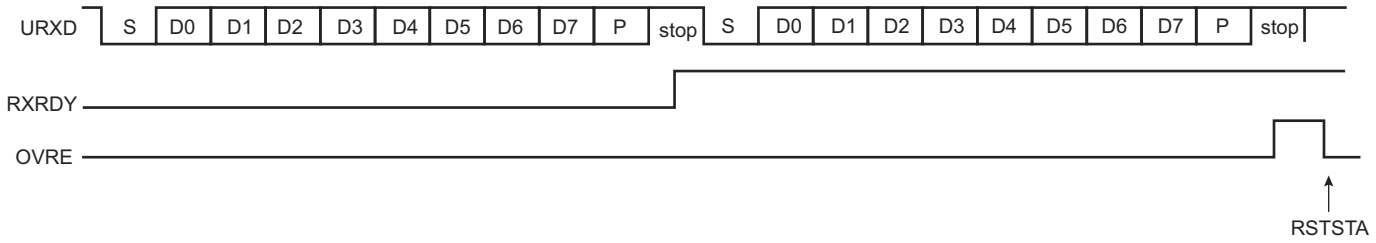
Figure 35-5. Receiver Ready



35.5.2.4 Receiver Overrun

The OVRE status bit in UART_SR is set if UART_RHR has not been read by the software (or the PDC) since the last transfer, the RXRDY bit is still set and a new character is received. OVRE is cleared when the software writes a 1 to the bit RSTSTA (Reset Status) in UART_CR.

Figure 35-6. Receiver Overrun



35.5.2.5 Parity Error

Each time a character is received, the receiver calculates the parity of the received data bits, in accordance with the field PAR in the Mode Register (UART_MR). It then compares the result with the received parity bit. If different, the parity error bit PARE in UART_SR is set at the same time RXRDY is set. The parity bit is cleared when UART_CR is written with the bit RSTSTA (Reset Status) at 1. If a new character is received before the reset status command is written, the PARE bit remains at 1.

36.7.10 USART Interrupt Mask Register (SPI_MODE)

Name: US_IMR (SPI_MODE)

Address: 0x40024010 (0), 0x40028010 (1), 0x4002C010 (2), 0x40030010 (3), 0x40034010 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	RXBUFF	TXBUFE	UNRE	TXEMPTY	–
7	6	5	4	3	2	1	0
–	–	OVRE	ENDTX	ENDRX	–	TXRDY	RXRDY

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

- **RXRDY: RXRDY Interrupt Mask**
- **TXRDY: TXRDY Interrupt Mask**
- **ENDRX: End of Receive Buffer Interrupt Mask**
- **ENDTX: End of Transmit Buffer Interrupt Mask**
- **OVRE: Overrun Error Interrupt Mask**
- **TXEMPTY: TXEMPTY Interrupt Mask**
- **UNRE: SPI Underrun Error Interrupt Mask**
- **TXBUFE: Transmit Buffer Empty Interrupt Mask**
- **RXBUFF: Receive Buffer Full Interrupt Mask**

40.7.18 ADC Analog Control Register

Name: ADC_ACR

Address: 0x40038094

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	ONREF	FORCEREF	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	IRVS				IRVCE	–	–

This register can only be written if the WPEN bit is cleared in “ADC Write Protection Mode Register”.

- **IRVCE: Internal Reference Voltage Change Enable**

0 (STUCK_AT_DEFAULT): The internal reference voltage is stuck at the default value (see Section 46. ”Electrical Characteristics” for further details).

1 (SELECTION): The internal reference voltage is defined by field IRVS.

- **IRVS: Internal Reference Voltage Selection**

See Table 46-44 “Programmable Voltage Reference Selection Values” for further details.

- **FORCEREF: Force Internal Reference Voltage**

0: The internal ADC voltage reference input is connected to the ADVREF line

1: The internal ADC voltage reference input is forced to VDDIO (ONREF must be cleared).

- **ONREF: Internal Voltage Reference ON**

0: The programmable voltage reference is OFF. The user can either force the internal ADC voltage reference input on the ADVREF pin or set the FORCEREF bit to connect VDDIO to the internal ADC voltage reference input.

1: The programmable voltage reference is ON and its output is connected both to the ADC voltage reference input and to the external ADVREF pin for decoupling (FORCEREF must be cleared).

40.7.20 ADC Write Protection Status Register

Name: ADC_WPSR

Address: 0x400380E8

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
WPVSRC							

15	14	13	12	11	10	9	8
WPVSRC							

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPVS

- **WPVS: Write Protection Violation Status**

0: No write protection violation has occurred since the last read of the ADC_WPSR register.

1: A write protection violation has occurred since the last read of the ADC_WPSR register. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

- **WPVSRC: Write Protection Violation Source**

When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

43.5.2.2 ICM Region Configuration Structure Member

Name: ICM_RCFG

Address: ICM_DSCR+0x004+RID*(0x10)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	MRPROT					
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	ALGO			–	PROCDLY	SUIEN	ECIEN
7	6	5	4	3	2	1	0
WCIEN	BEIEN	DMIEN	RHIEN	–	EOM	WRAP	CDWBN

- **CDWBN: Compare Digest or Write Back Digest**

0: The digest is written to the Hash area.

1: The digest value is compared to the digest stored in the Hash area.

- **WRAP: Wrap Command**

0: The next region descriptor address loaded is the current region identifier descriptor address incremented by 0x10.

1: The next region descriptor address loaded is ICM_DSCR.

- **EOM: End Of Monitoring**

0: The current descriptor does not terminate the monitoring.

1: The current descriptor terminates the Main List. WRAP bit value has no effect.

- **RHIEN: Region Hash Completed Interrupt Disable (Default Enabled)**

0: The ICM_ISR RHC[*i*] flag is set when the field NEXT = 0 in a descriptor of the main or second list.

1: The ICM_ISR RHC[*i*] flag remains cleared even if the setting condition is met.

- **DMIEN: Digest Mismatch Interrupt Disable (Default Enabled)**

0: The ICM_ISR RBE[*i*] flag is set when the hash value just calculated from the processed region differs from expected hash value.

1: The ICM_ISR RBE[*i*] flag remains cleared even if the setting condition is met.

- **BEIEN: Bus Error Interrupt Disable (Default Enabled)**

0: The flag is set when an error is reported on the system bus by the bus MATRIX.

1: The flag remains cleared even if the setting condition is met.

- **WCIEN: Wrap Condition Interrupt Disable (Default Enabled)**

0: The ICM_ISR RWC[*i*] flag is set when the WRAP bit is set in a descriptor of the main list.

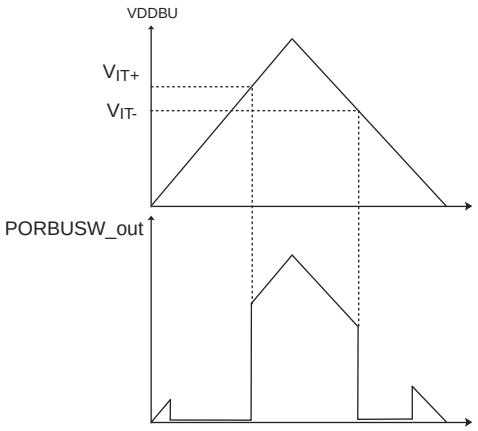
1: The ICM_ISR RWC[*i*] flag remains cleared even if the setting condition is met.

46.5.7 VDDBU Power-On-Reset

Table 46-25. Zero-Power-On POR (Backup POR) Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TH+}	Positive-going input threshold voltage (VDDBU)	At startup	1.45	1.53	1.59	V
V_{TH-}	Negative-going input threshold voltage (VDDBU)	–	1.35	1.45	1.55	V
I_{DDBU}	Current consumption	Enabled	–	300	700	nA
t_{res}	Reset time-out period	–	100	240	500	µs

Figure 46-15. Zero-Power-On Reset Characteristics



46.5.8 VDDIO Power-On-Reset

Table 46-26. Zero-Power-On POR (VDDIO POR) Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TH+}	Positive-going input threshold voltage (VDDIO)	At startup	1.45	1.53	1.59	V
V_{TH-}	Negative-going input threshold voltage (VDDIO)	–	1.35	1.45	1.55	V
I_{DDIO}	Current consumption	–	–	300	700	nA
t_{res}	Reset time-out period	–	100	240	500	µs

Table 46-40. ADC Analog Input Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FSR	Analog input full scale range(1)	–	0	–	V_{ADVREF}	V
C_{IN}	Input capacitance(2)	Accounts for I/O input capacitance + ADC sampling capacitor	–	–	10	pF

Notes: 1. If $V_{VDDIO} < V_{ADVREF}$, full scale range is limited to VDDIO.
2. Refer to Figure 46-18 “Simplified Acquisition Path”.

Table 46-41. Static Performance Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ADC}	Native ADC resolution	–	–	10	–	Bits
R_{ADC_AV}	Resolution with digital averaging	Refer to Section 40. “Analog-to-Digital Converter (ADC)”	10	–	12	Bits
INL	Integral non linearity	f_{CK_ADC} = 16 MHz	-2	–	+2	LSB
DNL	Differential non linearity		-1	–	+1	LSB
OE	Offset error	Errors with respect to the best fit line method	-5	–	5	LSB
GE	Gain error		-3	–	+3	LSB

Note: 1. In this table, values expressed in LSB refer to the Native ADC resolution (i.e., a 10-bit LSB).

Table 46-42. Dynamic Performance Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal to noise ratio	f_{CK_ADC} = 16 MHz, $V_{ADVREF} = V_{DDIN}$, f_{IN} = 50 kHz, $V_{INPP} = 0.95 \times V_{ADVREF}$	57	60	–	dB
THD	Total harmonic distortion		–	-68	-55	dB
SINAD	Signal to noise and distortion		52	59	–	dB
ENOB	Effective number of bits		8.3	9.6	–	Bits

46.6.2.1 SAM4CM4/8/16 Flash Wait States and Operating Frequency

The maximum operating frequency given in Table 46-52 below is limited by the Embedded Flash access time when the processor is fetching code out of it. The table gives the device maximum operating frequency depending on the FWS field of the EFC_FMR register. This field defines the number of wait states required to access the Embedded Flash Memory.

Table 46-52. SAM4CM4/8/16 Flash Wait State Versus Operating Frequency

FWS (Flash Wait State)	Maximum Operating Frequency (MHz) @ T_A = 85°C			
	VDDCORE = 1.08V VDDIO = 1.62V to 3.6V	VDDCORE = 1.2V VDDIO = 1.62V to 3.6V	VDDCORE = 1.08V VDDIO = 2.7V to 3.6V	VDDCORE = 1.2V VDDIO = 2.7V to 3.6V
0	16	17	20	21
1	33	35	40	42
2	51	52	61	63
3	67	70	81	85
4	85	87	98	106
5	100	105	–	120
6	–	121	–	–

46.6.2.2 SAM4CM32 Flash Wait States and Operating Frequency

The maximum operating frequency given in Table 46-53 below is limited by the Embedded Flash access time when the processor is fetching code out of it. The table gives the device maximum operating frequency depending on the FWS field of the EFC_FMR register. This field defines the number of wait states required to access the Embedded Flash Memory.

Table 46-53. SAM4CM32 Flash Wait State Versus Operating Frequency

FWS (Flash Wait State)	Maximum Operating Frequency (MHz) @ T_A = 85°C			
	VDDCORE = 1.08V VDDIO = 1.62V to 3.6V	VDDCORE = 1.2V VDDIO = 1.62V to 3.6V	VDDCORE = 1.08V VDDIO = 2.7V to 3.6V	VDDCORE = 1.2V VDDIO = 2.7V to 3.6V
0	16	17	20	21
1	33	34	40	42
2	50	52	60	63
3	67	69	80	83
4	84	86	91	104
5	91	104	–	118
6	–	114	–	–

Table 46-59. SAM4CM32 Typical Current Consumption in Wait Mode

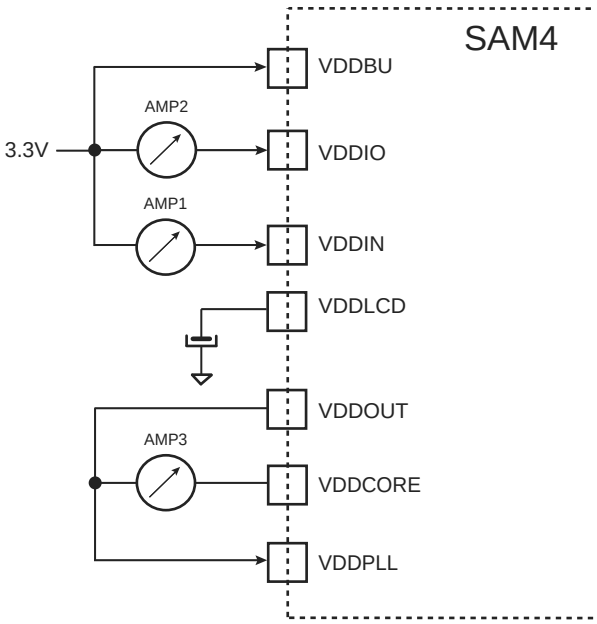
Conditions	IDD_BU - AMP1		IDD_IN/IO - AMP2		IDD_CORE - AMP3		Unit
	@25°C	@85°C	@25°C	@85°C	@25°C	@85°C	
Flash in Read-Idle mode	0.003	0.09	100	760	62	700	µA
Flash in Standby mode	0.003	0.09	100	760	62	700	
Flash in Deep Power-down mode	0.003	0.09	90	740	62	700	

46.7.3 Sleep Mode Current Consumption

Sleep mode configuration and measurements are defined in this section.

Reminder: The purpose of Sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clocks of CM4P0 and/or CM4P1 are stopped.

Figure 46-24. Measurement Setup for Sleep Mode



- VDDIO = VDDIN = 3.3V
- VDDCORE = 1.2V (Internal Voltage regulator used)
- T_A = 25°C
- Core 0 clock (HCLK) and Core 1 (CPHCLK) clock stopped
- Sub-system 0 Master Clock (MCK), Sub-system 1 Master Clock (CPBMCK) running at various frequencies (PLLB used for frequencies above 12 MHz, fast RC oscillator at 12 MHz for the 12 MHz point, and fast RC oscillator at 8 MHz divided by 1/2/4/8/16/32 for lower frequencies)
- All peripheral clocks deactivated
- No activity on I/O lines
- VDDPLL not taken into account. Refer to Section 46.5.14 “PLLA, PLLB Characteristics” for further details
- Current measurement as per Figure 46-24

50. SAM4CM16/8 Errata Revision A (MRL A) Parts

50.1 Device Identification

The following errata apply to the devices listed in Table 50-1.

Table 50-1. Device List

Device Marking	Chip ID
ATSAM4CMP16CA-AU	0xA64C_0CE0
ATSAM4CMP16CA-AUR	0xA64C_0CE0
ATSAM4CMP8CA-AU	0xA64C_0AE0
ATSAM4CMP8CA-AUR	0xA64C_0AE0
ATSAM4CMS16CA-AU	0xA64C_0CE0
ATSAM4CMS16CA-AUR	0xA64C_0CE0
ATSAM4CMS8CA-AU	0xA64C_0AE0
ATSAM4CMS8CA-AUR	0xA64C_0AE0

50.2 Flash Memory

50.2.1 Flash: Incorrect Flash Read May Occur Depending on VDDIO Voltage and Flash Wait State

Flash read issues leading to wrong instruction fetch or data read may occur under the following operating condition:

– VDDIO < 2.4V and Flash wait state(1) ≥ 1

If the core clock frequency does not require the use of the Flash wait state(2) (FWS = 0 in EEFC_FMR), there are no constraints on VDDIO voltage. The usable voltage range for VDDIO is defined in Table 46-2 “Recommended DC Operating Conditions on Power Supply Inputs”.

Notes: 1. FWS field in EEFC_FMR register.
2. Refer to Table 46-52 “SAM4CM4/8/16 Flash Wait State Versus Operating Frequency” and Table 46-53 “SAM4CM32 Flash Wait State Versus Operating Frequency” for maximum core clock frequency at zero (0) wait states.

Problem Fix/Workaround

None.

The issue is corrected in the device revision Marketing Revision Level B (MRL B). Please contact your local Sales Representative for further details.

50.3 Supply Controller (SUPC)

50.3.1 SUPC: Supply Monitor (SM) on VDDIO

The Supply Monitor (SM) Sampling mode reducing the average current consumption on VDDIO is not functional.

Problem Fix/Workaround

Use the Supply Monitor in Continuous mode only.

Table 55-3. SAM4CM Datasheet Rev. 11203C Revision History (Continued)

Doc. Rev. 11203C	Changes
06-Oct-14	Section 36. “Universal Synchronous Asynchronous Receiver Transmitter (USART)” ‘MCK’ replaced by ‘peripheral clock’ throughout. Section 36.2 “Embedded Characteristics”: Added ‘Digital Filter on Receive LIne’ bullet Updated Figure 36-1 “USART Block Diagram”. Removed table “SPI Operating Mode”. Section 36.6.1 “Baud Rate Generator”: updated 4th paragraph and figure. Updated information on RXIDLEV bit in Section 36.6.3.2 “Manchester Encoder” and Section 36.7.21 “USART Manchester Configuration Register”. Updated Figure 36-36 “Example of RTS Drive with Timeguard”. Table 36-7 “Possible Values for the Fi/Di Ratio”: in top row, replaced “774” with “744”. Section “Transmit Character Repetition”: updated 3rd paragraph. Section “Disable Successive Receive NACK”: updated last sentence. Section 36.6.7.5 “Character Transmission”: INACK replaced by WRDBT. Table 36-14 “Register Mapping”: US_MAN reset value corrected to 0x30011004. Section 36.7.3 “USART Mode Register”: Updated USART_MODE, USCLKS and PAR field descriptions. Added note on MAX_ITERATION field to DSNACK bit description. Section 36.7.4 “USART Mode Register (SPI_MODE)”: Deleted CHMODE filed description and added CLKO bit. Updated ENDRX, ENDTX, TXBUFE, and RXBUFF bit descriptions in Section 36.7.5 “USART Interrupt Enable Register”, Section 36.7.6 “USART Interrupt Enable Register (SPI_MODE)”, Section 36.7.7 “USART Interrupt Disable Register”, Section 36.7.9 “USART Interrupt Mask Register” and Section 36.7.11 “USART Channel Status Register”. Updated RXRDY, TXRDY, TXEMPTY, ITER and CTSIC bit descriptions in Section 36.7.11 “USART Channel Status Register”. Updated RXRDY, TXRDY, and TXEMPTY bit descriptions in Section 36.7.12 “USART Channel Status Register (SPI_MODE)” Section 36.7.18 “USART FI DI RATIO Register”: FI_DI_RATIO field now 11 bits wide and updated description.
	Section 37. “Timer Counter (TC)” ‘MCK’ replaced by ‘peripheral clock’ throughout. Added Section 37.6.14.6 “Missing Pulse Detection and Auto-correction”. Section 37.7.14 “TC Block Mode Register”: Removed FILTER bit (register bit 19 now reserved). Added AUTOC bit and MAXCMP field. Section 37.7.18 “TC QDEC Interrupt Status Register”: Added MPE bit.
	Section 39. “Segment Liquid Crystal Display Controller (SLCDC)” ‘SCLK’ replaced by ‘SLCK’ throughout. Updated Section 39.5.2 “Power Management”. In Section 39.5 “Product Dependencies”, removed section “Number of Segments and Commons”. Revised Section 39.6.7 “Disabling the SLCDC” (was “Disable Sequence”). Section 39.8.8 “SLCDC Interrupt Mask Register”: Modified access to Read-only. Updated DIS bit descriptions.