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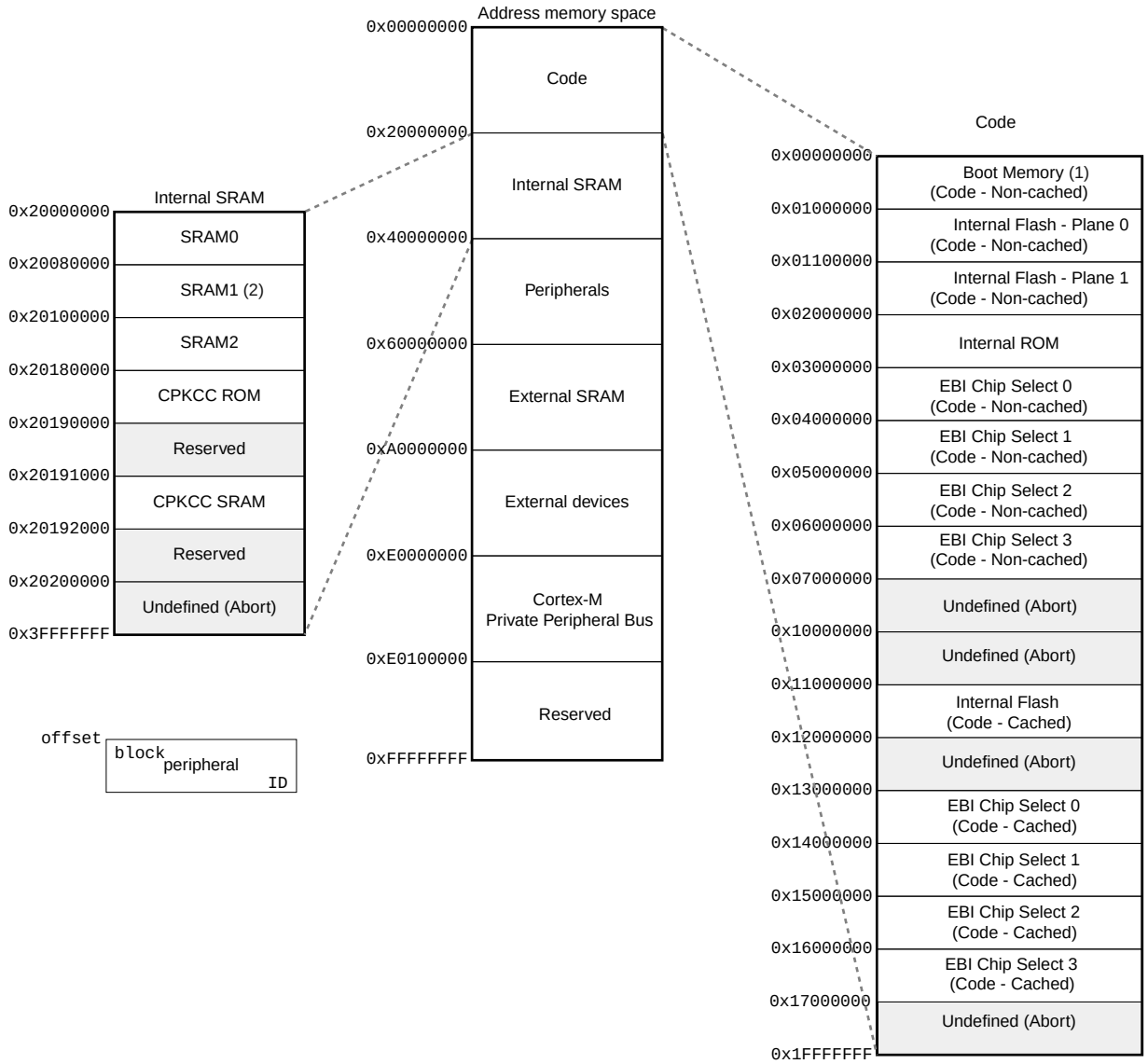
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4/M4F
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4cms8cb-au

Figure 7-3. SAM4CM32 Memory Mapping of CODE and SRAM Area



Notes: 1. Boot Memory for Core 0.
2. Boot Memory for Core 1 at 0x00000000.

11.3 APB/AHB Bridge

The SAM4CM embeds two peripheral bridges—one on each Matrix, with Matrix 0 for CM4P0 and Matrix 1 for CM4P1.

The peripherals of the bridge corresponding to CM4P0 (APB0) are clocked by MCK, and the peripherals of the bridge corresponding to CM4P1 (APB1) are clocked by CPBMCK.

11.4 Peripheral Signal Multiplexing on I/O Lines

The SAM4CM can multiplex the I/O lines of the peripheral set.

The SAM4CM PIO Controllers control up to 32 lines. Each line can be assigned to one of two peripheral functions: A or B. The multiplexing tables that follow define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only may be duplicated within the tables.

11.4.1 Pad Features

In Table 11-5 to Table 11-7, the column “Feature” indicates whether the corresponding I/O line has programmable Pull-up, Pull-down and/or Schmitt Trigger. Table 11-4 provides the key to the abbreviations used.

Table 11-4. I/O Line Features Abbreviations

Abbreviation	Definition
PUP(P)	Programmable Pull-up
PUP(NP)	Non-programmable Pull-up
PDN(P)	Programmable Pull-down
PDN(NP)	Non-programmable Pull-down
ST(P)	Programmable Schmitt Trigger
ST(NP)	Non-programmable Schmitt Trigger
LDRV(P)	Programmable Low Drive
LDRV(NRP)	Non-programmable Low Drive
HDRV(P)	Programmable High Drive
HDRV(NP)	Non-programmable High Drive
MaxDRV(NP)	Non-programmable Maximum Drive

11.4.2 Reset State

In Table 11-5 to Table 11-7, the column “Reset State” indicates the reset state of the line.

- PIO or signal name— Indicates whether the PIO line resets in I/O mode or in peripheral mode.
  If “PIO” is mentioned, the PIO line is in general-purpose I/O (GPIO). If a signal name is mentioned in the “Reset State” column, the PIO line is assigned to this function.
- I or O— Indicates whether the signal is input or output state.
- PU or PD— Indicates whether Pull-up, Pull-down or nothing is enabled.
- ST— Indicates that Schmitt Trigger is enabled.

Table 12-3. Ordering of the Memory Accesses Caused by Two Instructions

A2 / A1	Normal Access	Device Access		Strongly-ordered Access
		Non-shareable	Shareable	
Normal Access	–	–	–	–
Device access, non-shareable	–	<	–	<
Device access, shareable	–	–	<	<
Strongly-ordered access	–	<	<	<

Where:

– Means that the memory system does not guarantee the ordering of the accesses.

< Means that accesses are observed in program order, that is, A1 is always observed before A2.

12.4.2.3 Behavior of Memory Accesses

The following table describes the behavior of accesses to each region in the memory map.

Table 12-4. Memory Access Behavior

Address Range	Memory Region	Memory Type	XN	Description
0x00000000–0x1FFFFFFF	Code	Normal(1)	–	Executable region for program code. Data can also be put here.
0x20000000–0x3FFFFFFF	SRAM	Normal(1)	–	Executable region for data. Code can also be put here. This region includes bit band and bit band alias areas, see Table 12-6.
0x40000000–0x5FFFFFFF	Peripheral	Device(1)	XN	This region includes bit band and bit band alias areas, see Table 12-6.
0x60000000–0x9FFFFFFF	External RAM	Normal(1)	–	Executable region for data
0xA0000000–0xDFFFFFFF	External device	Device(1)	XN	External Device memory
0xE0000000–0xE00FFFFF	Private Peripheral Bus	Strongly-ordered(1)	XN	This region includes the NVIC, system timer, and system control block.
0xE0100000–0xFFFFFFFF	Reserved	Device(1)	XN	Reserved

Note: 1. See “Memory Regions, Types and Attributes” for more information.

The Code, SRAM, and external RAM regions can hold programs. However, ARM recommends that programs always use the Code region. This is because the processor has separate buses that enable instruction fetches and data accesses to occur simultaneously.

The MPU can override the default memory access behavior described in this section. For more information, see “Memory Protection Unit (MPU)”.

Additional Memory Access Constraints For Shared Memory

When a system includes shared memory, some memory regions have additional access constraints, and some regions are subdivided, as Table 12-5 shows.

Table 12-13. Cortex-M4 Instructions (Continued)

Mnemonic	Operands	Description	Flags
SMULBB, SMULBT SMULTB, SMULTT	{Rd,} Rn, Rm	Signed Multiply (halfwords)	–
SMULL	RdLo, RdHi, Rn, Rm	Signed Multiply (32 × 32), 64-bit result	–
SMULWB, SMULWT	{Rd,} Rn, Rm	Signed Multiply word by halfword	–
SMUSD, SMUSDX	{Rd,} Rn, Rm	Signed dual Multiply Subtract	–
SSAT	Rd, #n, Rm {,shift #s}	Signed Saturate	Q
SSAT16	Rd, #n, Rm	Signed Saturate 16	Q
SSAX	{Rd,} Rn, Rm	Signed Subtract and Add with Exchange	GE
SSUB16	{Rd,} Rn, Rm	Signed Subtract 16	–
SSUB8	{Rd,} Rn, Rm	Signed Subtract 8	–
STM	Rn{!}, reglist	Store Multiple registers, increment after	–
STMDB, STMEA	Rn{!}, reglist	Store Multiple registers, decrement before	–
STMFD, STMIA	Rn{!}, reglist	Store Multiple registers, increment after	–
STR	Rt, [Rn, #offset]	Store Register word	–
STRB, STRBT	Rt, [Rn, #offset]	Store Register byte	–
STRD	Rt, Rt2, [Rn, #offset]	Store Register two words	–
STREX	Rd, Rt, [Rn, #offset]	Store Register Exclusive	–
STREXB	Rd, Rt, [Rn]	Store Register Exclusive byte	–
STREXH	Rd, Rt, [Rn]	Store Register Exclusive halfword	–
STRH, STRHT	Rt, [Rn, #offset]	Store Register halfword	–
STRT	Rt, [Rn, #offset]	Store Register word	–
SUB, SUBS	{Rd,} Rn, Op2	Subtract	N,Z,C,V
SUB, SUBW	{Rd,} Rn, #imm12	Subtract	N,Z,C,V
SVC	#imm	Supervisor Call	–
SXTAB	{Rd,} Rn, Rm,{,ROR #}	Extend 8 bits to 32 and add	–
SXTAB16	{Rd,} Rn, Rm,{,ROR #}	Dual extend 8 bits to 16 and add	–
SXTAH	{Rd,} Rn, Rm,{,ROR #}	Extend 16 bits to 32 and add	–
SXTB16	{Rd,} Rm {,ROR #n}	Signed Extend Byte 16	–
SXTB	{Rd,} Rm {,ROR #n}	Sign extend a byte	–
SXTH	{Rd,} Rm {,ROR #n}	Sign extend a halfword	–
TBB	[Rn, Rm]	Table Branch Byte	–
TBH	[Rn, Rm, LSL #1]	Table Branch Halfword	–
TEQ	Rn, Op2	Test Equivalence	N,Z,C
TST	Rn, Op2	Test	N,Z,C
UADD16	{Rd,} Rn, Rm	Unsigned Add 16	GE
UADD8	{Rd,} Rn, Rm	Unsigned Add 8	GE
USAX	{Rd,} Rn, Rm	Unsigned Subtract and Add with Exchange	GE

12.8.3.1 Interrupt Set-enable Registers

Name: NVIC_ISERx [x=0..7]

Access: Read/Write

Reset: 0x000000000

31	30	29	28	27	26	25	24
SETENA							

23	22	21	20	19	18	17	16
SETENA							

15	14	13	12	11	10	9	8
SETENA							

7	6	5	4	3	2	1	0
SETENA							

These registers enable interrupts and show which interrupts are enabled.

- **SETENA: Interrupt Set-enable**

Write:

0: No effect.

1: Enables the interrupt.

Read:

0: Interrupt disabled.

1: Interrupt enabled.

Notes:
1. If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority.
2. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, the NVIC never activates the interrupt, regardless of its priority.

12.9.1.12 System Handler Control and State Register

Name: SCB_SHCSR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	USGFAULTENA	BUSFAULTENA	MEMFAULTENA

15	14	13	12	11	10	9	8
SVCALLPENDED	BUSFAULTPENDED	MEMFAULTPENDED	USGFAULTPENDED	SYSTICKACT	PENDSVACT	–	MONITORACT

7	6	5	4	3	2	1	0
SVCALLACT	–	–	–	USGFAULTACT	–	BUSFAULTACT	MEMFAULTACT

The SHCSR enables the system handlers, and indicates the pending status of the bus fault, memory management fault, and SVC exceptions; it also indicates the active status of the system handlers.

- **USGFAULTENA: Usage Fault Enable**

0: Disables the exception.

1: Enables the exception.

- **BUSFAULTENA: Bus Fault Enable**

0: Disables the exception.

1: Enables the exception.

- **MEMFAULTENA: Memory Management Fault Enable**

0: Disables the exception.

1: Enables the exception.

- **SVCALLPENDED: SVC Call Pending**

Read:

0: The exception is not pending.

1: The exception is pending.

Note: The user can write to these bits to change the pending status of the exceptions.

- **BUSFAULTPENDED: Bus Fault Exception Pending**

Read:

0: The exception is not pending.

1: The exception is pending.

Note: The user can write to these bits to change the pending status of the exceptions.

- **SIZE: Size of the MPU Protection Region**

The minimum permitted value is 3 (b00010).

The SIZE field defines the size of the MPU memory region specified by the MPU_RNR. as follows:

(Region size in bytes) = $2^{(SIZE+1)}$

The smallest permitted region size is 32B, corresponding to a SIZE value of 4. The table below gives an example of SIZE values, with the corresponding region size and value of N in the MPU_RBAR.

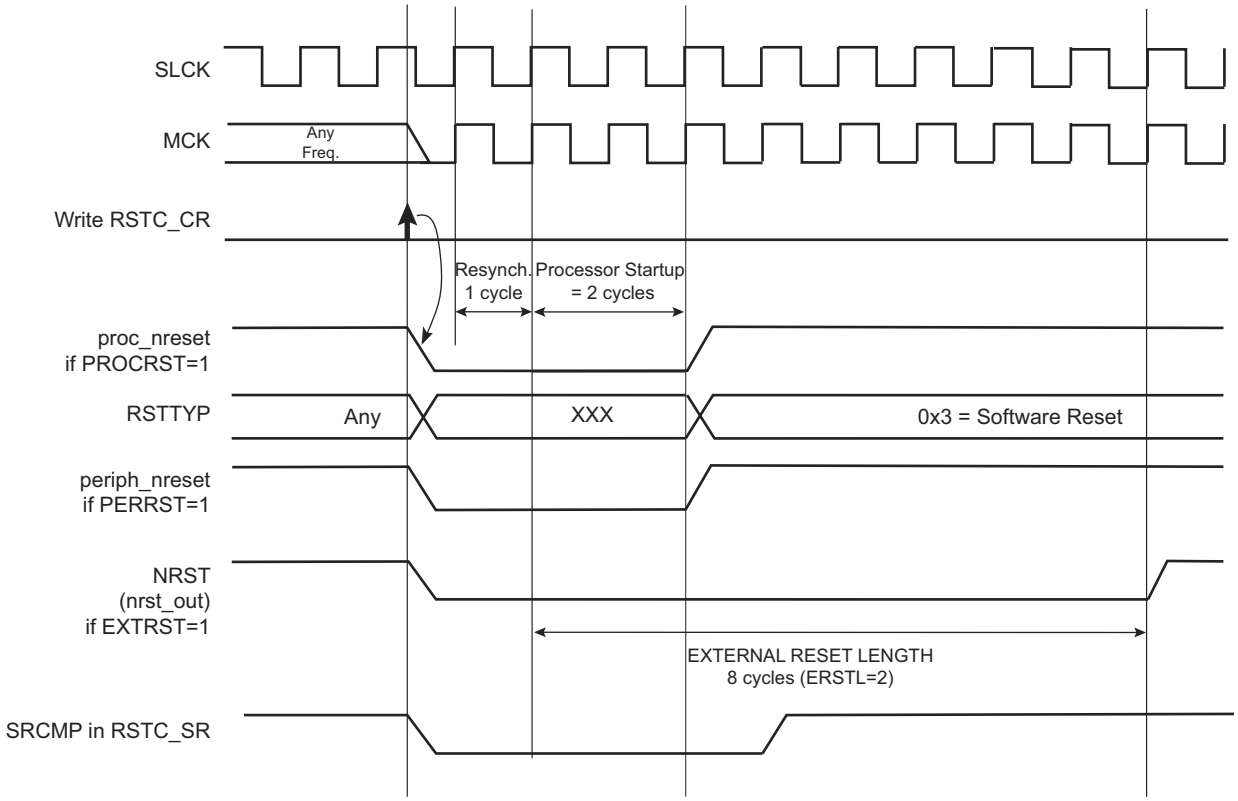
SIZE Value	Region Size	Value of N[1]	Note
b00100 (4)	32 B	5	Minimum permitted size
b01001 (9)	1 KB	10	–
b10011 (19)	1 MB	20	–
b11101 (29)	1 GB	30	–
b11111 (31)	4 GB	b01100	Maximum possible size

Note: 1. In the MPU_RBAR; see “MPU Region Base Address Register”

- **ENABLE: Region Enable**

Note: For information about access permission, see “MPU Access Permission Attributes”.

Figure 15-5. Software Reset



15.4.3.5 User Reset

The user reset is entered when a low level is detected on the NRST pin and bit URSTEN in the RSTC_MR is at 1. The NRST input signal is resynchronized with SLCK to ensure proper behavior of the system. Thus, the NRST pin must be asserted for at least 1 SLCK clock cycle to ensure execution of a user reset.

The user reset is entered 2 slow clock cycles (SLCK) after a low level is detected on NRST. The processor and coprocessor reset and the peripheral resets are asserted.

The user reset ends when NRST rises, after a two-cycle resynchronization time and a three-cycle processor startup. The processor clock is re-enabled as soon as NRST is confirmed high.

When the processor reset signal is released, field RSTC_SR.RSTTYP is loaded with the value 0x4, indicating a user reset.

The NRST manager guarantees that the NRST line is asserted for External Reset Length slow clock cycles, as programmed in field RSTC_MR.ERSTL. However, if NRST does not rise after External Reset Length because it is driven low externally, the internal reset lines remain asserted until NRST actually rises.

21.3.1 General Purpose Backup Register x

Name: SYS_GPBRx

Address: 0x400E1490

Access: Read/Write

31	30	29	28	27	26	25	24
GPBR_VALUE							

23	22	21	20	19	18	17	16
GPBR_VALUE							

15	14	13	12	11	10	9	8
GPBR_VALUE							

7	6	5	4	3	2	1	0
GPBR_VALUE							

These registers are reset at first power-up and on each loss of VDDBU_SW.

- **GPBR_VALUE: Value of GPBR x**

If a Tamper event has been detected, it is not possible to write GPBR_VALUE as long as the LPDBCS0 or LPDBCS3 flag has not been cleared in the Supply Controller Status Register (SUPC_SR).

32.6.5 PIO Output Disable Register

Name: PIO_ODR

Address: 0x400E0E14 (PIOA), 0x400E1014 (PIOB), 0x4800C014 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

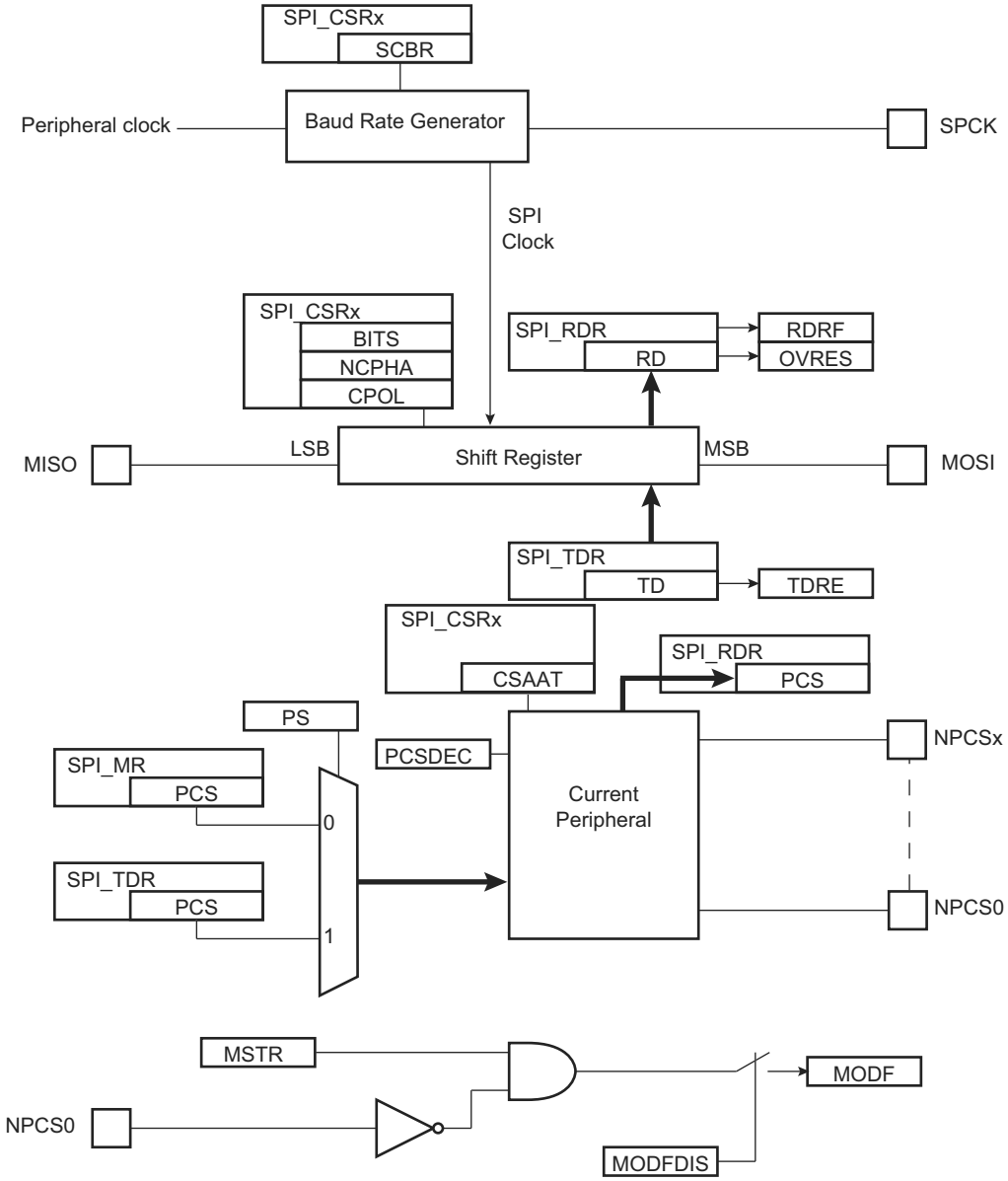
- **P0–P31: Output Disable**

0: No effect.

1: Disables the output on the I/O line.

33.7.3.1 Master Mode Block Diagram

Figure 33-6. Master Mode Block Diagram



- **DLYBCT: Delay Between Consecutive Transfers**

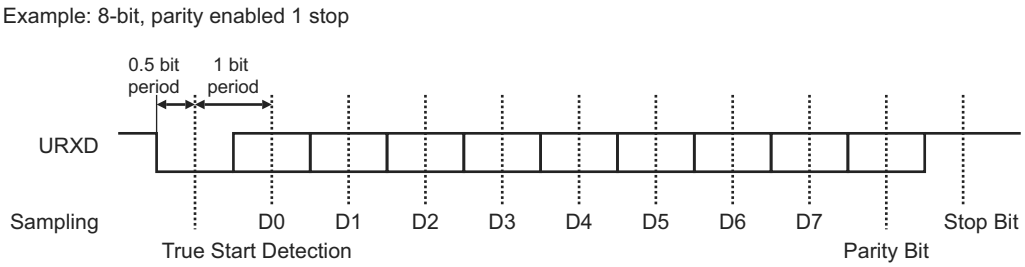
This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT = 0, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers.

Otherwise, the following equation determines the delay:

DLYBCT = Delay Between Consecutive Transfers × $f_{peripheral\ clock}$ / 32

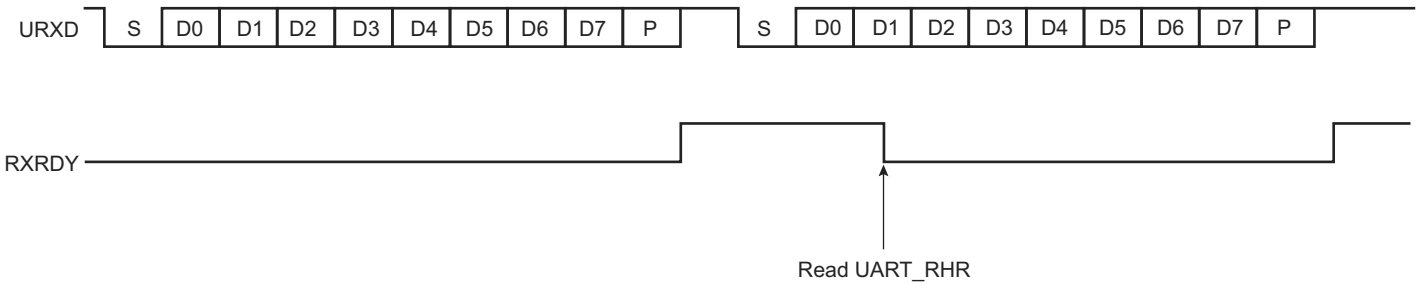
Figure 35-4. Character Reception



35.5.2.3 Receiver Ready

When a complete character is received, it is transferred to the Receive Holding Register (UART_RHR) and the RXRDY status bit in the Status Register (UART_SR) is set. The bit RXRDY is automatically cleared when UART_RHR is read.

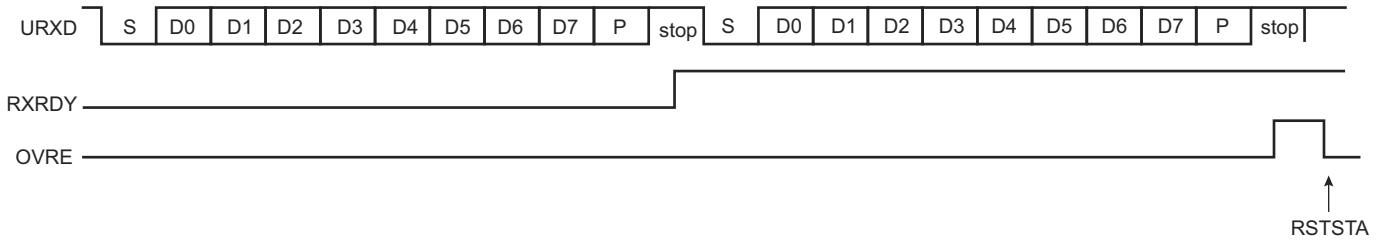
Figure 35-5. Receiver Ready



35.5.2.4 Receiver Overrun

The OVRE status bit in UART_SR is set if UART_RHR has not been read by the software (or the PDC) since the last transfer, the RXRDY bit is still set and a new character is received. OVRE is cleared when the software writes a 1 to the bit RSTSTA (Reset Status) in UART_CR.

Figure 35-6. Receiver Overrun



35.5.2.5 Parity Error

Each time a character is received, the receiver calculates the parity of the received data bits, in accordance with the field PAR in the Mode Register (UART_MR). It then compares the result with the received parity bit. If different, the parity error bit PARE in UART_SR is set at the same time RXRDY is set. The parity bit is cleared when UART_CR is written with the bit RSTSTA (Reset Status) at 1. If a new character is received before the reset status command is written, the PARE bit remains at 1.

- **CHMODE: Channel Mode**

Value	Name	Description
0	NORMAL	Normal mode
1	AUTOMATIC	Automatic echo
2	LOCAL_LOOPBACK	Local loopback
3	REMOTE_LOOPBACK	Remote loopback

- **OPT_CLKDIV: Optical Link Clock Divider**

0 to 31: The optical modulation clock frequency is defined by PLLACK / (8 * (OPT_CLKDIV + 8)).

- **OPT_DUTY: Optical Link Modulation Clock Duty Cycle**

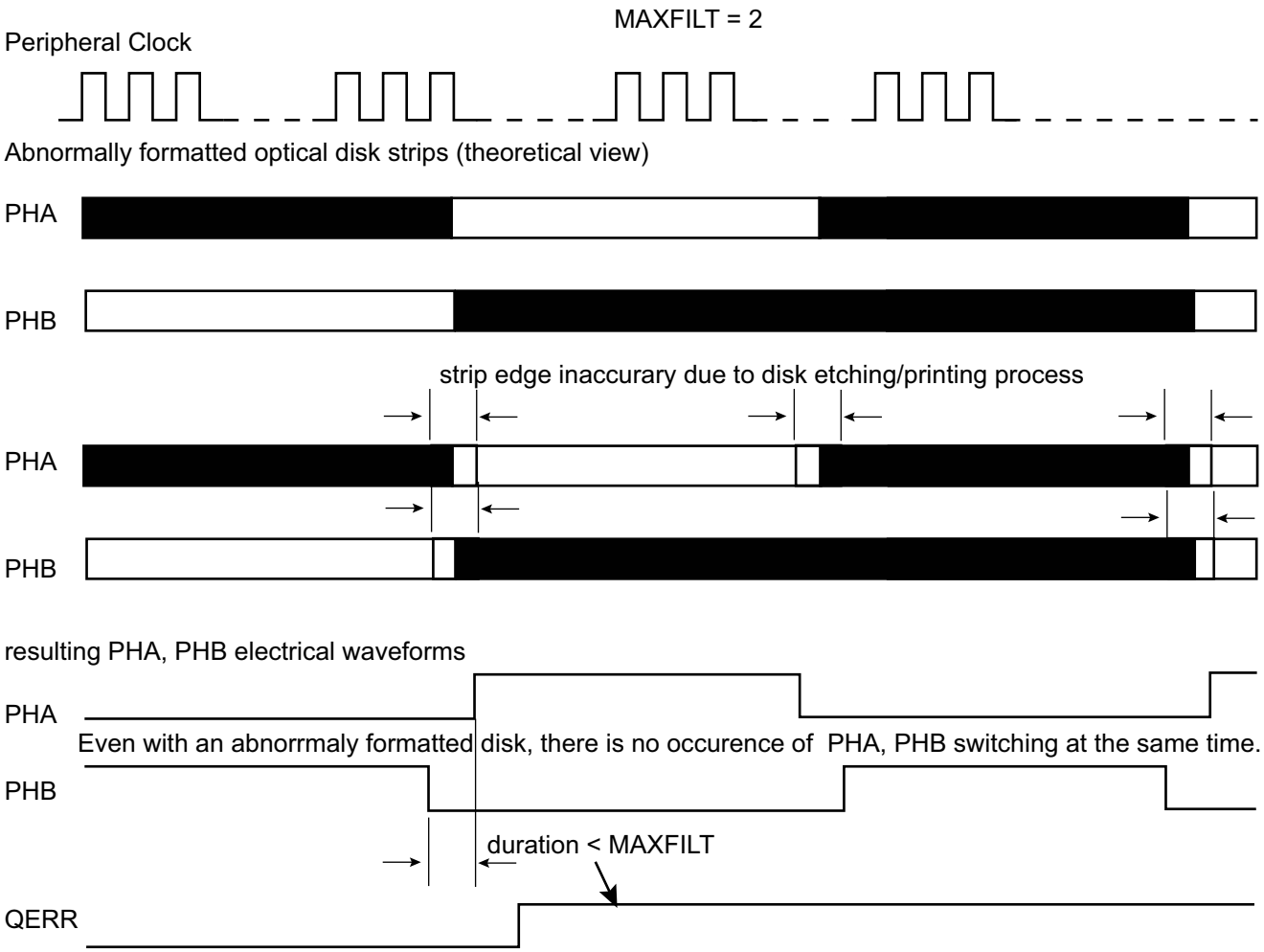
Value	Name	Description
0	DUTY_50	Modulation clock duty cycle Is 50%.
1	DUTY_43P75	Modulation clock duty cycle Is 43.75%.
2	DUTY_37P5	Modulation clock duty cycle Is 37.5%.
3	DUTY_31P25	Modulation clock duty cycle Is 31.75%.
4	DUTY_25	Modulation clock duty cycle Is 25%.
5	DUTY_18P75	Modulation clock duty cycle Is 18.75%.
6	DUTY_12P5	Modulation clock duty cycle Is 12.5%.
7	DUTY_6P25	Modulation clock duty cycle Is 6.25%.

- **OPT_CMPTH: Receive Path Comparator Threshold**

Value	Name	Description
0	VDDIO_DIV2	Comparator threshold is VDDIO/2 volts.
1	VDDIO_DIV2P5	Comparator threshold is VDDIO/2.5 volts.
2	VDDIO_DIV3P3	Comparator threshold is VDDIO/3.3 volts.
3	VDDIO_DIV5	Comparator threshold is VDDIO/5 volts.
4	VDDIO_DIV10	Comparator threshold is VDDIO/10 volts.

configurable and corresponds to (MAXFILT + 1) × $t_{peripheral\ clock}$ ns. After being filtered there is no reason to have two edges closer than (MAXFILT + 1) × $t_{peripheral\ clock}$ ns under normal mode of operation.

Figure 37-19. Quadrature Error Detection



MAXFILT must be tuned according to several factors such as the peripheral clock frequency, type of rotary sensor and rotation speed to be achieved.

37.6.14.4 Position and Rotation Measurement

When the POSEN bit is set in the TC_BMR, the motor axis position is processed on channel 0 (by means of the PHA, PHB edge detections) and the number of motor revolutions are recorded on channel 1 if the IDX signal is provided on the TIOB1 input. The position measurement can be read in the TC_CV0 register and the rotation measurement can be read in the TC_CV1 register.

Channel 0 and 1 must be configured in Capture mode (TC_CMR0.WAVE = 0). ‘Rising edge’ must be selected as the External Trigger Edge (TC_CMR.ETRGEDG = 0x01) and ‘TIOA’ must be selected as the External Trigger (TC_CMR.ABETRG = 0x1).

In parallel, the number of edges are accumulated on timer/counter channel 0 and can be read on the TC_CV0 register.

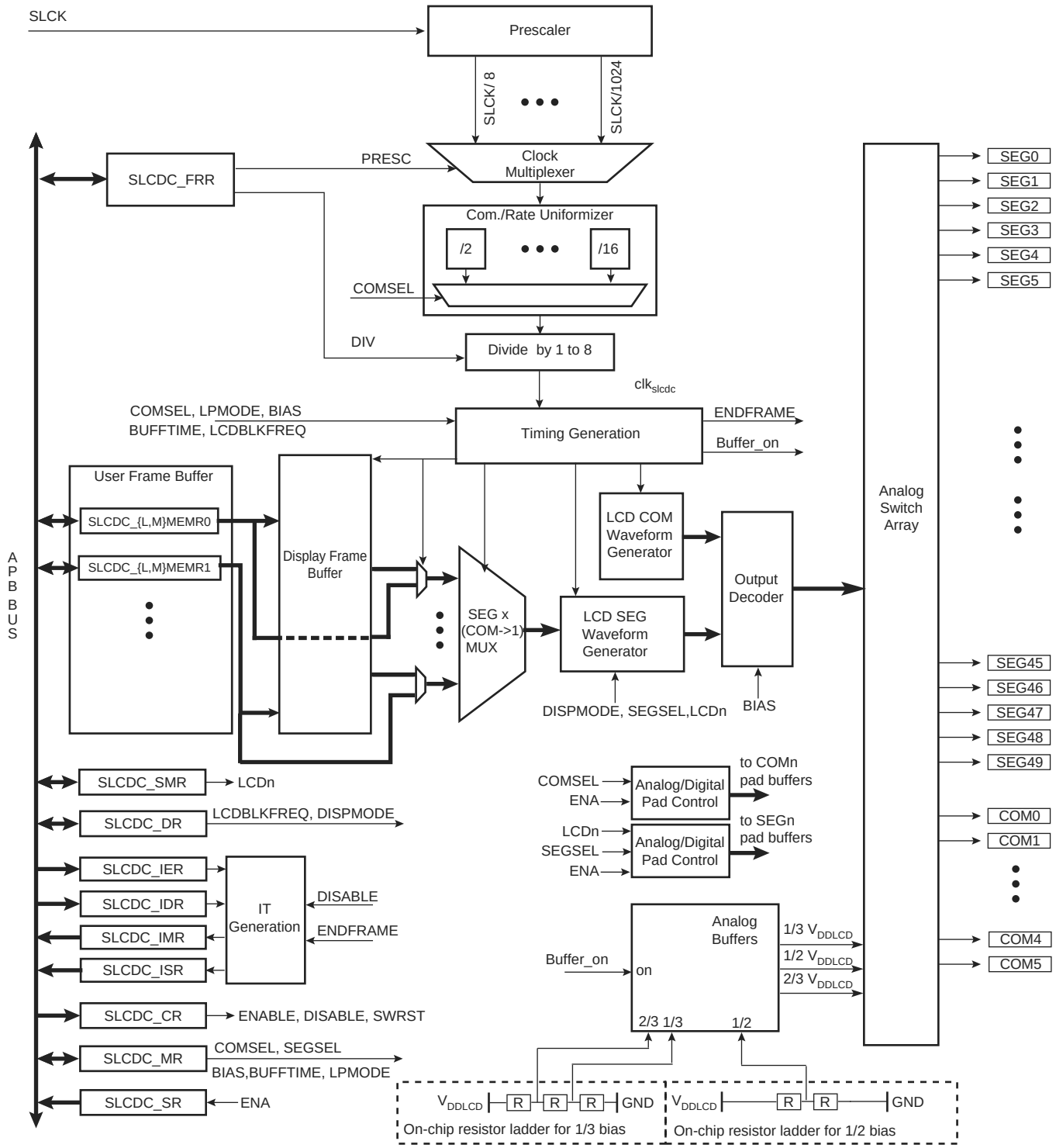
Therefore, the accurate position can be read on both TC_CV registers and concatenated to form a 32-bit word.

The timer/counter channel 0 is cleared for each increment of IDX count value.

- Segments Layout can be Fully Defined by User to Optimize Usage of Multiplexed Digital Functions
- Latching of Display Data Gives Full Freedom in Register Updates
- Power Saving Modes for Extremely Low Power Consumption

39.3 Block Diagram

Figure 39-1. SLCDC Block Diagram



8. When software reads one of the AES_ODATARx, the DATRDY bit is automatically cleared.

Table 42-2. Authorized Input Data Registers

Operation Mode	Input Data Registers to Write
ECB	All
CBC	All
OFB	All
128-bit CFB	All
64-bit CFB	AES_IDATAR0 and AES_IDATAR1
32-bit CFB	AES_IDATAR0
16-bit CFB	AES_IDATAR0
8-bit CFB	AES_IDATAR0
CTR	All
GCM	All

Notes: 1. In 64-bit CFB mode, writing to AES_IDATAR2 and AES_IDATAR3 is not allowed and may lead to errors in processing.
2. In 32, 16, and 8-bit CFB modes, writing to AES_IDATAR1, AES_IDATAR2 and AES_IDATAR3 is not allowed and may lead to errors in processing.

42.4.4.2 Auto Mode

The Auto Mode is similar to the manual one, except that in this mode, as soon as the correct number of AES_IDATARx is written, processing is automatically started without any action in the AES_CR.

42.4.4.3 PDC Mode

The Peripheral DMA Controller (PDC) can be used in association with the AES to perform an encryption/decryption of a buffer without any action by software during processing.

The field SMOD in the AES_MR must be configured to 0x2.

The sequence order is as follows:

1. Write the AES_MR with all required fields, including but not limited to SMOD and OPMOD.
2. Write the key in the AES_KEYWRx.
3. Write the initialization vector (or counter) in the AES_IVRx.

Note: The AES_IVRx concern all modes except ECB.

4. Set the Transmit Pointer Register (AES_TPR) to the address where the data buffer to encrypt/decrypt is stored and the Receive Pointer Register (AES_RPR) where it must be encrypted/decrypted.

Note: Transmit and receive buffers can be identical.

5. Set the Transmit and the Receive Counter Registers (AES_TCR and AES_RCR) to the same value. This value must be a multiple of the data transfer type size (see Table 42-3).

Note: The same requirements are necessary for the Next Pointer(s) and Counter(s) of the PDC (AES_TNPR, AES_RNPR, AES_TNCR, AES_RNCR).

6. If not already done, set the bit ENDRX (or RXBUFF if the next pointers and counters are used) in the AES_IER, depending on whether an interrupt is required or not at the end of processing.
7. Enable the PDC in transmission and reception to start the processing (AES_PTCR).

When the processing completes, the ENDRX (or RXBUFF) flag in the AES_ISR is raised. If an interrupt has been enabled by setting the corresponding bit in the AES_IER, the interrupt line of the AES is activated.

42.5.1 AES Control Register

Name: AES_CR

Address: 0x40000000

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	SWRST
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	START

- **START: Start Processing**

0: No effect.

1: Starts manual encryption/decryption process.

- **SWRST: Software Reset**

0: No effect.

1: Resets the AES. A software-triggered hardware reset of the AES interface is performed.

from noisy switching signals (clock, data, PWM, etc.). A good practice is to shield them with a quiet ground net to avoid coupling to neighboring signals.

46.5.14 PLLA, PLLB Characteristics

Table 46-33. PLLA Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDPLL}	Supply voltage range (VDDPLL)	–	1.08	1.2	1.32	V
f_{IN}	Input frequency range	–	30	32.768	34	kHz
f_{OUT}	Output frequency range	–	7.5	8.192	8.5	MHz
N_{RATIO}	Frequency multiplying ratio (MULA +1)	–	–	250	–	–
J_P	Period jitter	Peak value	–	4	–	ns
t_{ON}	Start-up time	From OFF to output oscillations (Output frequency within 10% of target frequency)	–	–	250	µs
t_{LOCK}	Lock time	From OFF to PLL locked	–	–	2.5	ms
I_{PLLON}	Active mode current consumption (VDDPLL)	f_{OUT} = 8.192 MHz	–	50	–	µA
I_{PLLOFF}	OFF mode current consumption (VDDPLL)	@25°C Over the temperature range	–	0.05 0.05	0.30 5	µA

Table 46-34. PLLB Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDPLL}	Supply voltage range (VDDPLL)	–	1.08	1.2	1.32	V
f_{IN}	Input frequency range	–	3	–	32	MHz
f_{OUT}	Output frequency range	–	80	–	240	MHz
N_{RATIO}	Frequency multiplying ratio (MULB +1)	–	3	–	62	–
Q_{RATIO}	Frequency dividing ratio (DIVB)	–	2	–	24	–
t_{ON}	Start-up time	–	–	60	150	µs
IDD_{PLL}	Current consumption on VDDPLL	Active mode @ 80 MHz @1.2V Active mode @ 96 MHz @1.2V Active mode @ 160 MHz @1.2V Active mode @ 240 MHz @1.2V	–	0.94 1.2 2.1 3.34	1.2 1.5 2.5 4	mA

Table 46-56. SAM4CM4/8/16 Typical Current Consumption Values for Backup Mode Configurations C and D

Conditions	Configuration C		Configuration D		Unit
	IDD_BU - AMP1	IDD_IN/IO - AMP2	IDD_BU - AMP1	IDD_IN/IO - AMP2	
VDDIO = 3.6V @25°C	0.05	3.6	0.05	10.5	µA
VDDIO = 3.3V @25°C		3.3		9.9	
VDDIO = 3.0V @25°C		2.9		9.3	
VDDIO = 2.5V @25°C		2.4		8.3	
VDDIO = 3.6V @85°C	0.09	7.8	0.10	15.9	
VDDIO = 3.3V @85°C		7.2		15.0	
VDDIO = 3.0V @85°C		6.7		14.4	
VDDIO = 2.5V @85°C		5.7		13.2	

Table 46-57. SAM4CM32 Typical Current Consumption Values for Backup Mode Configurations C and D

Conditions	Configuration C		Configuration D		Unit
	IDD_BU - AMP1	IDD_IN/IO - AMP2	IDD_BU - AMP1	IDD_IN/IO - AMP2	
VDDIO = 3.6V @25°C	0.05	4.5	0.05	10.7	µA
VDDIO = 3.3V @25°C		4.0		9.9	
VDDIO = 3.0V @25°C		3.6		9.1	
VDDIO = 2.5V @25°C		3.1		8.3	
VDDIO = 3.6V @85°C	0.09	10.7	0.10	18.2	
VDDIO = 3.3V @85°C		9.8		16.9	
VDDIO = 3.0V @85°C		9.0		15.9	
VDDIO = 2.5V @85°C		7.9		14.3	

Figure 46-22. Typical Current Consumption in Backup Mode for Configurations C and D

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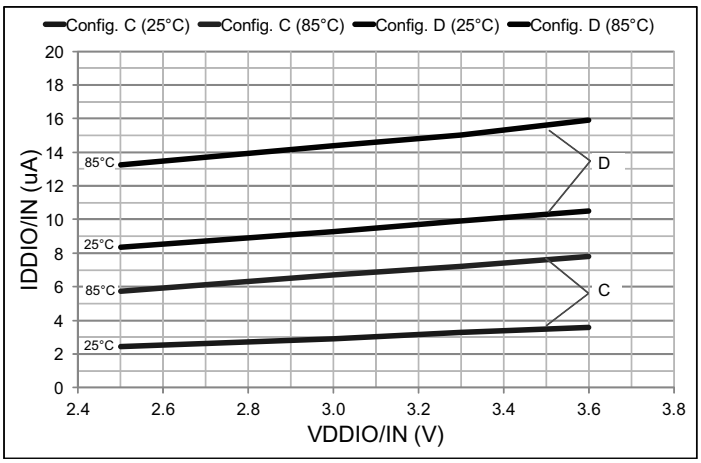

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