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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4/M4F
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4cms8cb-aur

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

8.1.4.10 GPNVM Bits

The SAM4CM features two (SAM4CM16/SAM4CM8/SAM4CM4) or three (SAM4CM32) GPNVM bits. These bits can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface (refer to Section 22. “Enhanced Embedded Flash Controller (EEFC)”).

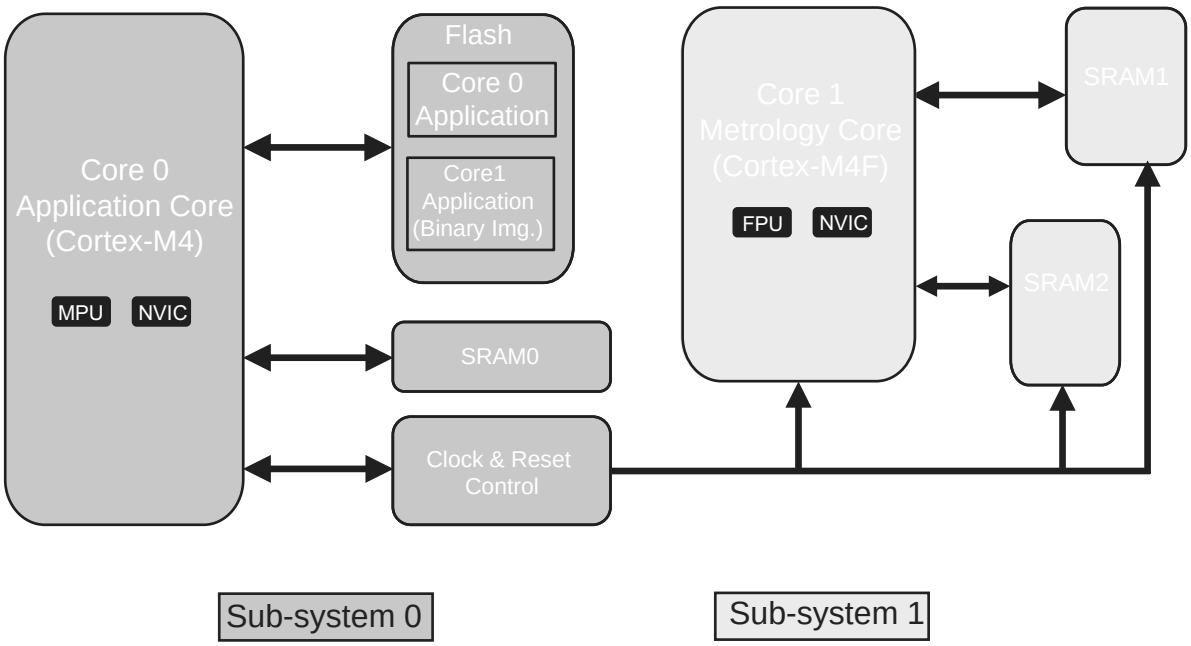
Table 8-3. General-purpose Nonvolatile Memory Bits

GPNVM Bit	Function
0	Security bit
1	Boot mode selection
2	Memory Plane Boot Selection (Plane 0 or Plane 1) (SAM4CM32 only)

8.1.5 Boot Strategy

Figure 8-5 below shows a load view of the memory at boot time.

Figure 8-5. Simplified Load View at Boot Time



Note: Matrices, AHB and APB Bridges are not represented.

8.1.5.1 Application Core (Core 0) Boot Process

The application processor (CM4P0) always boots at the address 0x0. To ensure maximum boot possibilities, the memory layout can be changed using a General-purpose NVM (GPNVM) bit. A GPNVM bit is used to boot either on the ROM (default) or from the Flash. The GPNVM bit can be cleared or set through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface. Setting GPNVM Bit 1 selects the boot from Flash whereas clearing this bit selects the boot from ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

12.4.1.15 Base Priority Mask Register

Name: BASEPRI

Access: Read/Write

Reset: 0x000000000

31	30	29	28	27	26	25	24
–							

23	22	21	20	19	18	17	16
–							

15	14	13	12	11	10	9	8
–							

7	6	5	4	3	2	1	0
BASEPRI							

The BASEPRI register defines the minimum priority for exception processing. When BASEPRI is set to a nonzero value, it prevents the activation of all exceptions with same or lower priority level as the BASEPRI value.

- **BASEPRI**

Priority mask bits:

0x0000: No effect

Nonzero: Defines the base priority for exception processing

The processor does not process any exception with a priority value greater than or equal to BASEPRI.

This field is similar to the priority fields in the interrupt priority registers. The processor implements only bits[7:4] of this field, bits[3:0] read as zero and ignore writes. See “Interrupt Priority Registers” for more information. Remember that higher priority field values correspond to lower exception priorities.

For more information about hard faults, memory management faults, bus faults, and usage faults, see “Fault Handling”.

12.4.3.3 Exception Handlers

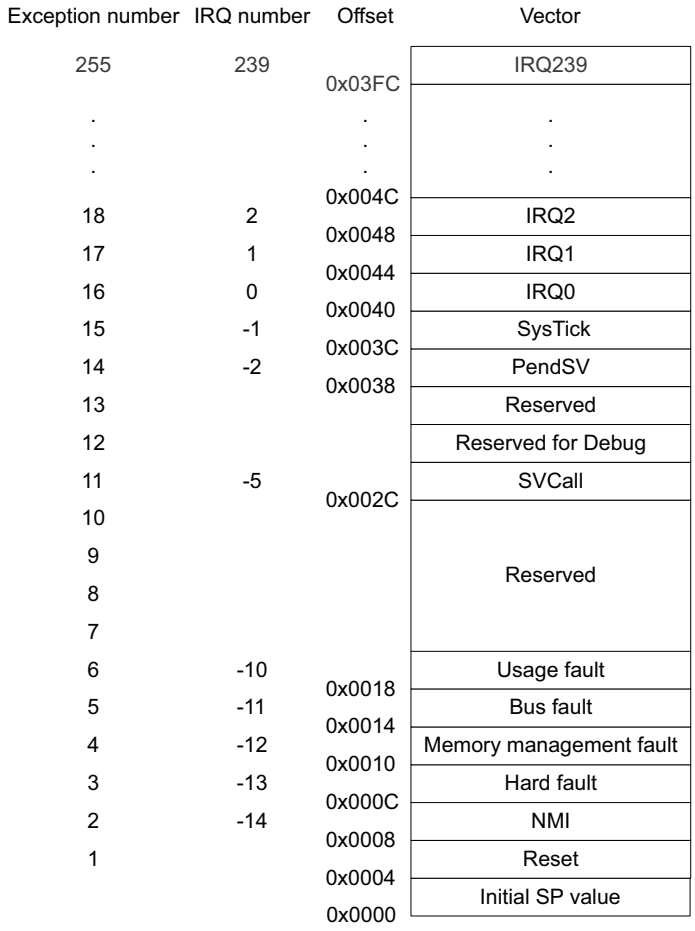
The processor handles exceptions using:

- Interrupt Service Routines (ISRs)
  Interrupts IRQ0 to IRQ40 are the exceptions handled by ISRs.
- Fault Handlers
  Hard fault, memory management fault, usage fault, bus fault are fault exceptions handled by the fault handlers.
- System Handlers
  NMI, PendSV, SVCall SysTick, and the fault exceptions are all system exceptions that are handled by system handlers.

12.4.3.4 Vector Table

The vector table contains the reset value of the stack pointer, and the start addresses, also called exception vectors, for all exception handlers. Figure 12-6 shows the order of the exception vectors in the vector table. The least-significant bit of each vector must be 1, indicating that the exception handler is Thumb code.

Figure 12-6. Vector Table



On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the SCB_VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80, see “Vector Table Offset Register”.

Table 12-13. Cortex-M4 Instructions (Continued)

Mnemonic	Operands	Description	Flags
SMULBB, SMULBT SMULTB, SMULTT	{Rd,} Rn, Rm	Signed Multiply (halfwords)	–
SMULL	RdLo, RdHi, Rn, Rm	Signed Multiply (32 × 32), 64-bit result	–
SMULWB, SMULWT	{Rd,} Rn, Rm	Signed Multiply word by halfword	–
SMUSD, SMUSDX	{Rd,} Rn, Rm	Signed dual Multiply Subtract	–
SSAT	Rd, #n, Rm {,shift #s}	Signed Saturate	Q
SSAT16	Rd, #n, Rm	Signed Saturate 16	Q
SSAX	{Rd,} Rn, Rm	Signed Subtract and Add with Exchange	GE
SSUB16	{Rd,} Rn, Rm	Signed Subtract 16	–
SSUB8	{Rd,} Rn, Rm	Signed Subtract 8	–
STM	Rn{!}, reglist	Store Multiple registers, increment after	–
STMDB, STMEA	Rn{!}, reglist	Store Multiple registers, decrement before	–
STMFD, STMIA	Rn{!}, reglist	Store Multiple registers, increment after	–
STR	Rt, [Rn, #offset]	Store Register word	–
STRB, STRBT	Rt, [Rn, #offset]	Store Register byte	–
STRD	Rt, Rt2, [Rn, #offset]	Store Register two words	–
STREX	Rd, Rt, [Rn, #offset]	Store Register Exclusive	–
STREXB	Rd, Rt, [Rn]	Store Register Exclusive byte	–
STREXH	Rd, Rt, [Rn]	Store Register Exclusive halfword	–
STRH, STRHT	Rt, [Rn, #offset]	Store Register halfword	–
STRT	Rt, [Rn, #offset]	Store Register word	–
SUB, SUBS	{Rd,} Rn, Op2	Subtract	N,Z,C,V
SUB, SUBW	{Rd,} Rn, #imm12	Subtract	N,Z,C,V
SVC	#imm	Supervisor Call	–
SXTAB	{Rd,} Rn, Rm,{,ROR #}	Extend 8 bits to 32 and add	–
SXTAB16	{Rd,} Rn, Rm,{,ROR #}	Dual extend 8 bits to 16 and add	–
SXTAH	{Rd,} Rn, Rm,{,ROR #}	Extend 16 bits to 32 and add	–
SXTB16	{Rd,} Rm {,ROR #n}	Signed Extend Byte 16	–
SXTB	{Rd,} Rm {,ROR #n}	Sign extend a byte	–
SXTH	{Rd,} Rm {,ROR #n}	Sign extend a halfword	–
TBB	[Rn, Rm]	Table Branch Byte	–
TBH	[Rn, Rm, LSL #1]	Table Branch Halfword	–
TEQ	Rn, Op2	Test Equivalence	N,Z,C
TST	Rn, Op2	Test	N,Z,C
UADD16	{Rd,} Rn, Rm	Unsigned Add 16	GE
UADD8	{Rd,} Rn, Rm	Unsigned Add 8	GE
USAX	{Rd,} Rn, Rm	Unsigned Subtract and Add with Exchange	GE

12.9.1.17 Bus Fault Address Register

Name: SCB_BFAR

Access: Read/Write

31	30	29	28	27	26	25	24
ADDRESS							

23	22	21	20	19	18	17	16
ADDRESS							

15	14	13	12	11	10	9	8
ADDRESS							

7	6	5	4	3	2	1	0
ADDRESS							

The SCB_BFAR contains the address of the location that generated a bus fault.

- **ADDRESS: Bus Fault Generation Location Address**

When the BFARVALID bit of the BFSR subregister is set to 1, this field holds the address of the location that generated the bus fault.

Notes:
1. When an unaligned access faults, the address in the SCB_BFAR is the one requested by the instruction, even if it is not the address of the fault.
2. Flags in the BFSR indicate the cause of the fault, and whether the value in the SCB_BFAR is valid. See “BFSR: Bus Fault Status Subregister”.

12.11.2.3 MPU Region Number Register

Name: MPU_RNR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
REGION							

The MPU_RNR selects which memory region is referenced by the MPU_RBAR and MPU_RASRs.

- **REGION: MPU Region Referenced by the MPU_RBAR and MPU_RASRs**

Indicates the MPU region referenced by the MPU_RBAR and MPU_RASRs.

The MPU supports 8 memory regions, so the permitted values of this field are 0–7.

Normally, the required region number is written to this register before accessing the MPU_RBAR or MPU_RASR. However, the region number can be changed by writing to the MPU_RBAR with the VALID bit set to 1; see “MPU Region Base Address Register”. This write updates the value of the REGION field.

12.12.2.1 Coprocessor Access Control Register

Name: CPACR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
CP11		CP10		–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

The CPACR specifies the access privileges for coprocessors.

- **CP10: Access Privileges for Coprocessor 10**

The possible values of each field are:

0: Access denied. Any attempted access generates a NOCP UsageFault.

1: Privileged access only. An unprivileged access generates a NOCP fault.

2: Reserved. The result of any access is unpredictable.

3: Full access.

- **CP11: Access Privileges for Coprocessor 11**

The possible values of each field are:

0: Access denied. Any attempted access generates a NOCP UsageFault.

1: Privileged access only. An unprivileged access generates a NOCP fault.

2: Reserved. The result of any access is unpredictable.

3: Full access.

20.4.5 Using Backup Battery/Automatic Power Switch

The power switch automatically selects either VDDBU or VDDIO as a power source.

As soon as VDDIO is present (higher than 1.9V), it supplies the backup area of the device (VDDBU_SW = VDDIO) even if the voltage of VDDBU is higher than VDDIO. If not, the backup area is supplied by the VDDBU voltage source (VDDBU_SW = VDDBU). For more information on power supply schematics, refer to the section “Power Supplies”.

20.4.6 Supply Monitor

The SUPC embeds a supply monitor located in the VDDBU_SW power domain and which monitors VDDIO power supply.

The supply monitor can be used to prevent the processor from falling into an unpredictable state if the main power supply drops below a certain level.

The threshold of the supply monitor is programmable. It can be selected from 1.9V to 3.4V by steps of 100 mV. This threshold is configured in the SMTH field of the Supply Controller Supply Monitor Mode register (SUPC_SMMR).

The supply monitor can also be enabled during one slow clock period on every one of either 32, 256 or 2048 slow clock periods, depending on the user selection. This is configured in the SMSMPL field in SUPC_SMMR.

Enabling the supply monitor for such reduced times divides the typical supply monitor power consumption by factors of 2, 16 or 128, respectively, if continuous monitoring of the VDDIO power supply is not required.

A supply monitor detection can either generate a system reset (vddcore_nreset signal is asserted) or a system wakeup. Generating a system reset when a supply monitor detection occurs is enabled by setting the SMRSTEN bit in SUPC_SMMR.

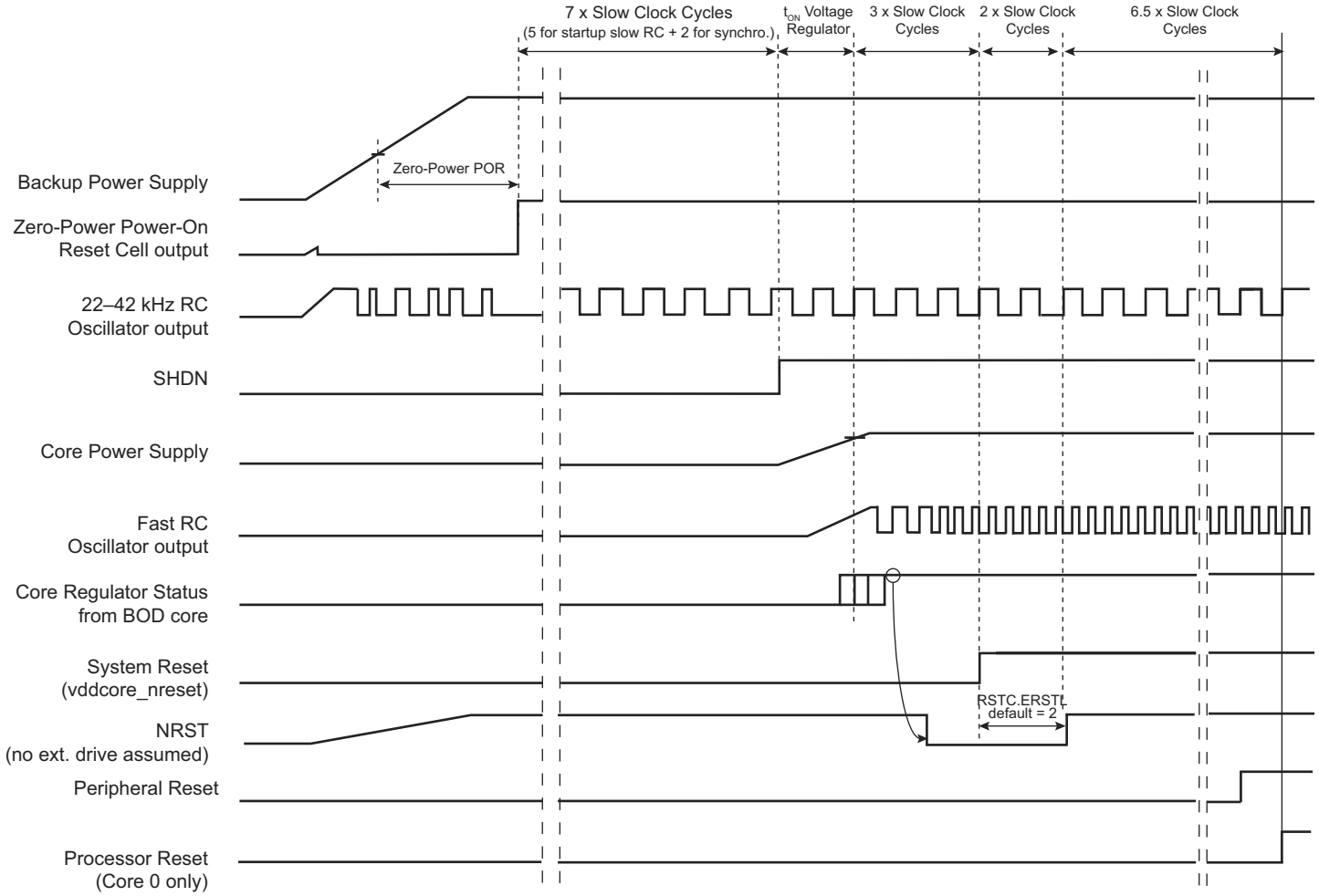
Waking up the system when a supply monitor detection occurs is enabled by setting the SMEN bit in the Supply Controller Wakeup Mode register (SUPC_WUMR).

The SUPC provides two status bits for the supply monitor in the SUPC_SR. These bits determine whether the last wakeup was due to the supply monitor:

- The SMOS bit provides real-time information, updated at each measurement cycle or updated at each Slow Clock cycle, if the measurement is continuous.
- The SMS bit provides saved information and shows a supply monitor detection has occurred since the last read of SUPC_SR.

The SMS bit generates an interrupt if the SMIEN bit is set in SUPC_SMMR.

Figure 20-3. Raising the VDDBU_SW Power Supply



Note: After processor reset rising, the core starts fetching instructions from Flash at 4 MHz.

20.4.7.2 SHDN Output Pin

The SHDN pin is designed to drive the enable pin of an external voltage regulator. This pin is controlled by the VROFF bit in SUPC_CR. When the device goes into Backup mode (bit VROFF set), the SHDN pin is asserted low. Upon a wakeup event, the SHDN pin is released (VDDBU level).

20.4.8 System Reset

The SUPC manages the system reset signal (vddcore_nreset) to the Reset Controller, as described in Section 20.4.7 ”Backup Power Supply Reset”. The system reset signal is normally asserted before shutting down the core power supply and released as soon as the core power supply is correctly regulated.

There are two additional sources which can be programmed to activate the system reset signal:

- a supply monitor detection
- a brownout detection

20.4.8.1 Supply Monitor Reset

The supply monitor can generate a reset of the system. This can be enabled by setting the SMRSTEN bit in SUPC_SMMR.

The output of the supply monitor is synchronized on SLCK. If SMRSTEN is set and if a supply monitor detection occurs, the system reset is asserted one or two slow clock cycles after the detection.

Figure 23-2. Parallel Programming Timing, Write Sequence

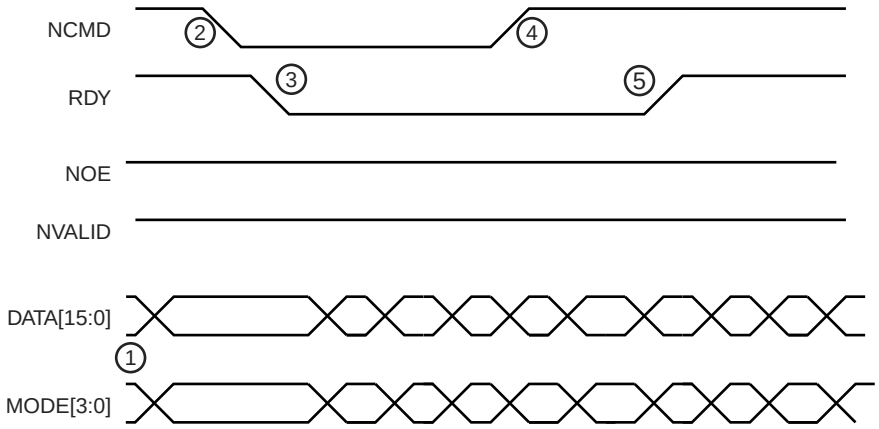


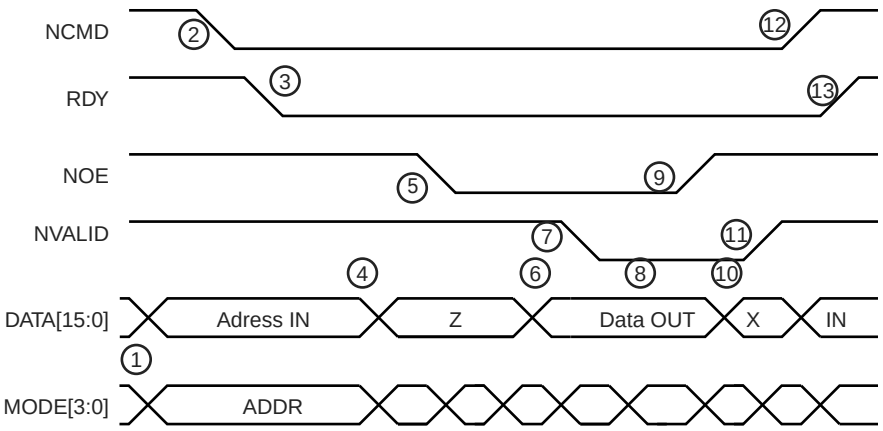
Table 23-4. Write Handshake

Step	Programmer Action	Device Action	Data I/O
1	Sets MODE and DATA signals	Waits for NCMD low	Input
2	Clears NCMD signal	Latches MODE and DATA	Input
3	Waits for RDY low	Clears RDY signal	Input
4	Releases MODE and DATA signals	Executes command and polls NCMD high	Input
5	Sets NCMD signal	Executes command and polls NCMD high	Input
6	Waits for RDY high	Sets RDY	Input

23.3.4.2 Read Handshaking

For details on the read handshaking sequence, refer to Figure 23-3 and Table 23-5.

Figure 23-3. Parallel Programming Timing, Read Sequence



These additional modes are:

- Rising edge detection
- Falling edge detection
- Low-level detection
- High-level detection

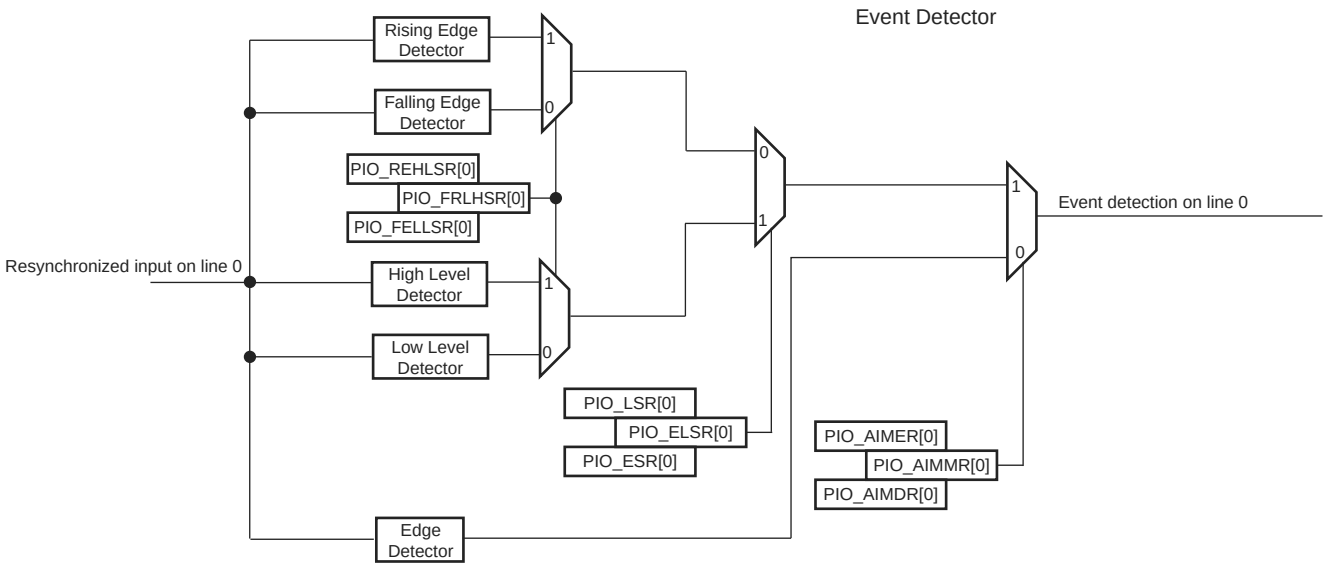
In order to select an additional interrupt mode:

- The type of event detection (edge or level) must be selected by writing in the Edge Select Register (PIO_ESR) and Level Select Register (PIO_LSR) which select, respectively, the edge and level detection. The current status of this selection is accessible through the Edge/Level Status Register (PIO_ELSR).
- The polarity of the event detection (rising/falling edge or high/low-level) must be selected by writing in the Falling Edge/Low-Level Select Register (PIO_FELLSR) and Rising Edge/High-Level Select Register (PIO_REHLSR) which allow to select falling or rising edge (if edge is selected in PIO_ELSR) edge or high- or low-level detection (if level is selected in PIO_ELSR). The current status of this selection is accessible through the Fall/Rise - Low/High Status Register (PIO_FRLHSR).

When an input edge or level is detected on an I/O line, the corresponding bit in the Interrupt Status Register (PIO_ISR) is set. If the corresponding bit in PIO_IMR is set, the PIO Controller interrupt line is asserted.The interrupt signals of the 32 channels are ORed-wired together to generate a single interrupt signal to the interrupt controller.

When the software reads PIO_ISR, all the interrupts are automatically cleared. This signifies that all the interrupts that are pending when PIO_ISR is read must be handled. When an Interrupt is enabled on a “level”, the interrupt is generated as long as the interrupt source is not cleared, even if some read accesses in PIO_ISR are performed.

Figure 32-6. Event Detector on Input Lines (Figure Represents Line 0)



Example of interrupt generation on following lines:

- Rising edge on PIO line 0
- Falling edge on PIO line 1
- Rising edge on PIO line 2
- Low-level on PIO line 3
- High-level on PIO line 4
- High-level on PIO line 5

Figure 34-8. Master Read with One Data Byte

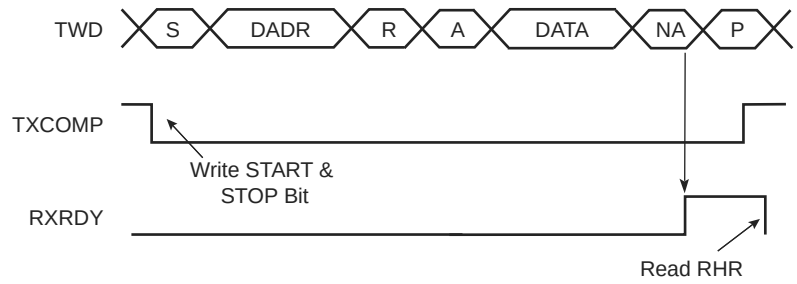


Figure 34-9. Master Read with Multiple Data Bytes

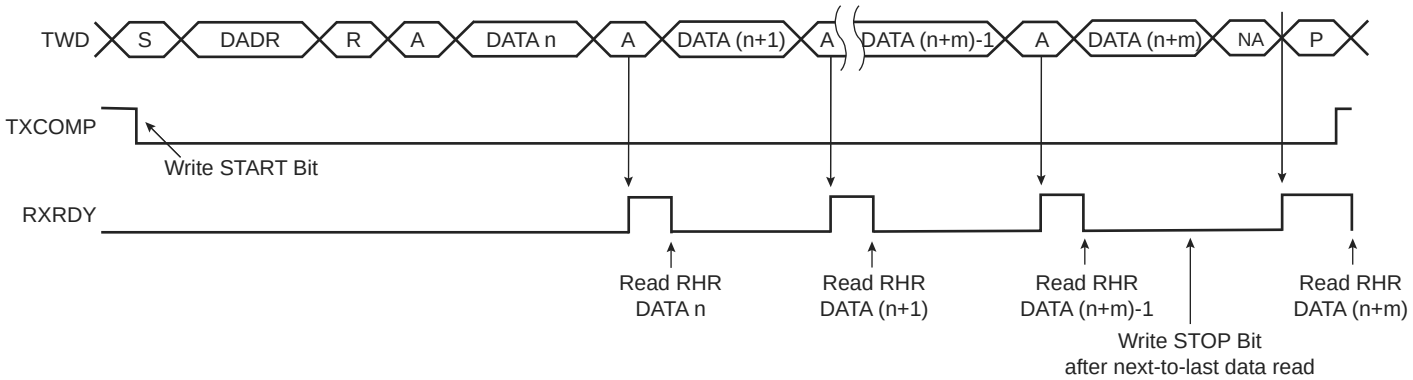
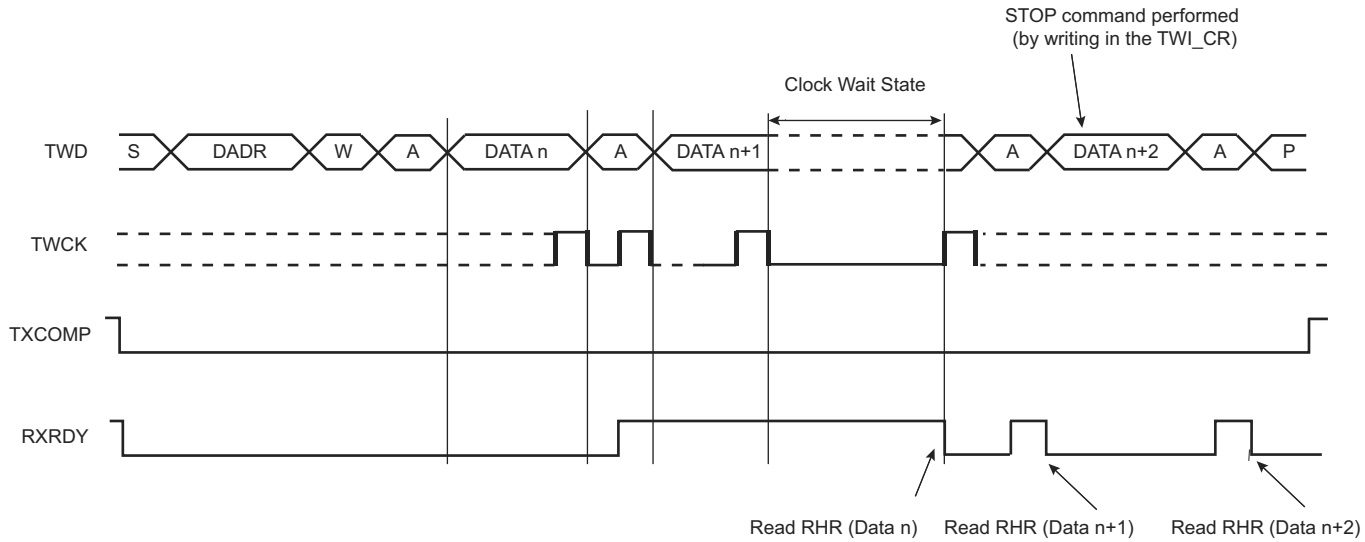


Figure 34-10. Master Read Wait State with Multiple Data Bytes



34.7.3.6 Internal Address

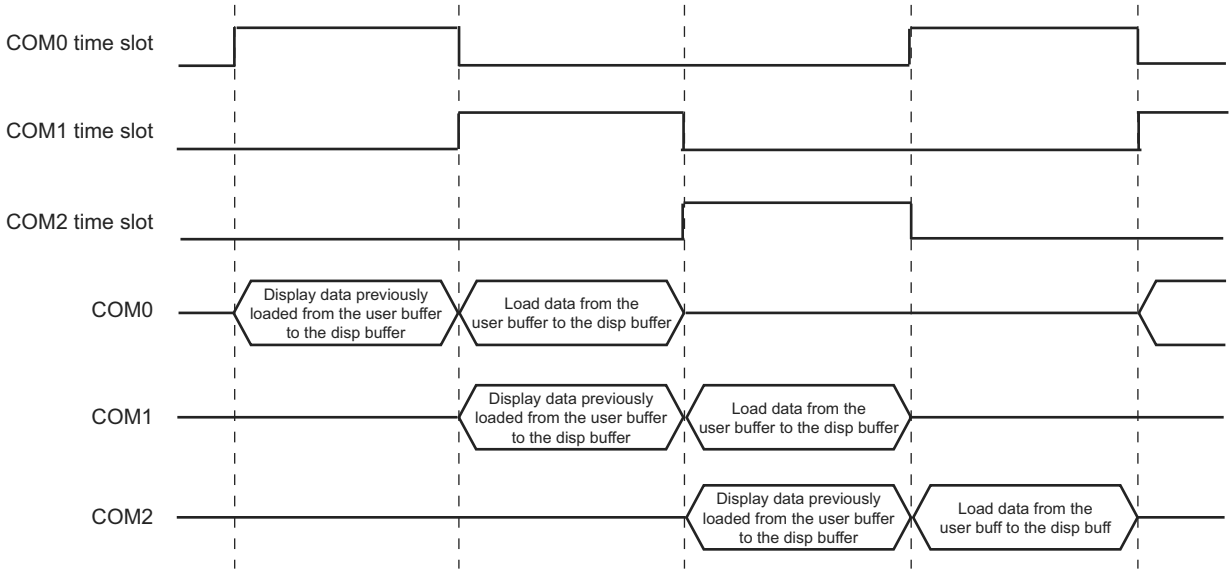
The TWI can perform transfers with 7-bit slave address devices and 10-bit slave address devices.

7-bit Slave Addressing

When addressing 7-bit slave devices, the internal address bytes are used to perform random address (read or write) accesses to reach one or more data bytes, e.g. within a memory page location in a serial memory. When performing read operations with an internal address, the TWI performs a write operation to set the internal address into the slave device, and then switch to Master receiver mode. Note that the second START condition (after

39.6.4 SLCDC memory

Figure 39-9. Memory Management



When a bit in the display memory (SLCDC_LMEMRx and SLCDC_MMEMRx registers) is written to one, the corresponding segment is energized (on), and non-energized when a bit in the display memory is written to zero.

At the beginning of each common, the display buffer is updated. The value of the previous common is latched in the display memory (its value is transferred from the user buffer to the frame buffer).

The advantages of this solution are:

- Ability to access the user buffer at any time in the frame, in any display mode and even in low power waveform
- Ability to change only one pixel without reloading the picture

39.6.5 Display Features

In order to improve the flexibility of SLCDC the following set of display modes are embedded:

- Force mode off: all pixels are turned off and the memory content is kept.
- Force mode on: all pixels are turned on and the memory content is kept.
- Inverted Mode: all pixels are set in the inverted state as defined in SLCDC memory and the memory content is kept.
- Two blinking modes:
  - Standard Blinking mode: all pixels are alternately turned off to the predefined state in SLCDC memory at LCDBLKFREQ frequency.
  - Inverted Blinking mode: all pixels are alternately turned off to the predefined opposite state in SLCDC memory at LCDBLKFREQ frequency.
- Buffer Swap mode: all pixels are alternatively assigned to the state defined in the user buffer then to the state defined in the display buffer.

39.8.8 SLCDC Interrupt Mask Register

Name: SLCDC_IMR

Address: 0x4003C028

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	DIS	–	ENDFRAME

- **ENDFRAME: End of Frame Interrupt Mask**

0: The corresponding interrupt is not enabled.

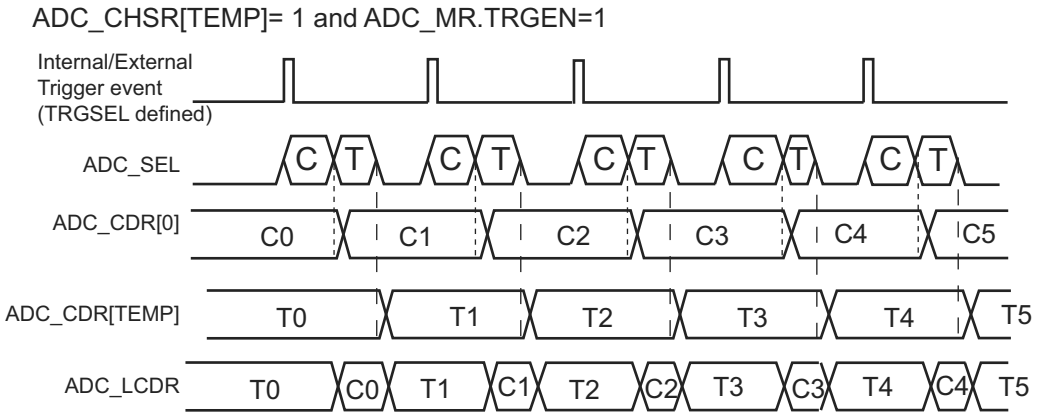
1: The corresponding interrupt is enabled.

- **DIS: SLCDC Disable Completion Interrupt Mask**

0: The corresponding interrupt is not enabled.

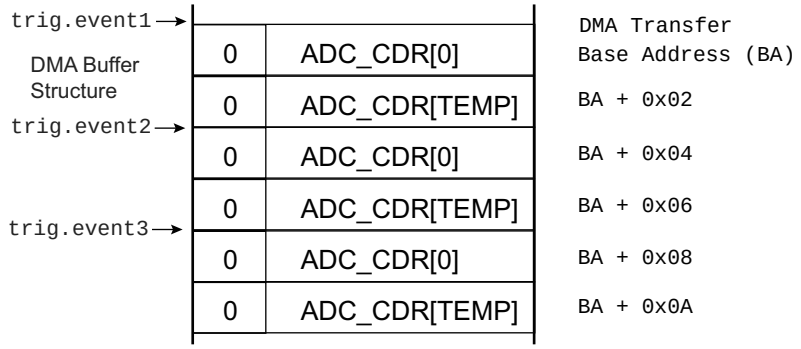
1: The corresponding interrupt is enabled.

Figure 40-6. Non-optimized Temperature Conversion



Notes: ADC_SEL: Command to the ADC cell
C: Classic ADC Conversion Sequence
T: Temperature Sensor Channel

Assuming ADC_CHSR[0] = 1 and ADC_CHSR[TEMP] = 1
where TEMP is the index of the temperature sensor channel



The temperature factor has a slow variation rate and is potentially different from other conversion channels. As a result, the ADC Controller triggers the measurement differently when TEMPON is set in ADC_TEMPMR but CH7 is not set in the ADC_CHSR.

Under these conditions, the measurement is triggered every second by means of an internal trigger generated by the RTC, always enabled and totally independent of the internal/external triggers. The RTC event will be processed on the next internal/external trigger event as described in Figure 40-7, "Optimized Temperature Conversion Combined With Classical Conversions". The internal/external trigger is selected through the TRGSEL field of ADC_MR.

In this mode of operation, the temperature sensor is only powered for a period of time covering the startup time and conversion time (refer to Figure 40-8, "Temperature Conversion Only").

Every second, a conversion is scheduled for channel 7 but the result of the conversion is only uploaded in ADC_CDR7 and not in ADC_LCDR. Therefore there is no change in the structure of the Peripheral DMA Controller buffer due to the conversion of the temperature channel; only the enabled channels are kept in the buffer. The end of conversion of the temperature channel is reported by means of EOC7 flag in ADC_ISR.

43.6.6 ICM Interrupt Mask Register

Name: ICM_IMR

Address: 0x40044018

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	URAD

23	22	21	20	19	18	17	16
RSU				REC			

15	14	13	12	11	10	9	8
RWC				RBE			

7	6	5	4	3	2	1	0
RDM				RHC			

- **RHC: Region Hash Completed Interrupt Mask**

0: When RHC[*i*] is set to zero, the interrupt is disabled for region i.

1: When RHC[*i*] is set to one, the interrupt is enabled for region i.

- **RDM: Region Digest Mismatch Interrupt Mask**

0: When RDM[*i*] is set to zero, the interrupt is disabled for region i.

1: When RDM[*i*] is set to one, the interrupt is enabled for region i.

- **RBE: Region Bus Error Interrupt Mask**

0: When RBE[*i*] is set to zero, the interrupt is disabled for region i.

1: When RBE[*i*] is set to one, the interrupt is enabled for region i.

- **RWC: Region Wrap Condition Detected Interrupt Mask**

0: When RWC[*i*] is set to zero, the interrupt is disabled for region i.

1: When RWC[*i*] is set to one, the interrupt is enabled for region i.

- **REC: Region End bit Condition Detected Interrupt Mask**

0: When REC[*i*] is set to zero, the interrupt is disabled for region i.

1: When REC[*i*] is set to one, the interrupt is enabled for region i.

- **RSU: Region Status Updated Interrupt Mask**

0: When RSU[*i*] is set to zero, the interrupt is disabled for region i.

1: When RSU[*i*] is set to one, the interrupt is enabled for region i.

- **URAD: Undefined Register Access Detection Interrupt Mask**

0: Interrupt is disabled

1: Interrupt is enabled.

43.6.7 ICM Interrupt Status Register

Name: ICM_ISR

Address: 0x4004401C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	URAD

23	22	21	20	19	18	17	16
RSU				REC			

15	14	13	12	11	10	9	8
RWC				RBE			

7	6	5	4	3	2	1	0
RDM				RHC			

- **RHC: Region Hash Completed**

When RHC[*i*] is set, it indicates that the ICM has completed the region with identifier *i*.

- **RDM: Region Digest Mismatch**

When RDM[*i*] is set, it indicates that there is a digest comparison mismatch between the hash value of the region with identifier *i* and the reference value located in the Hash Area.

- **RBE: Region Bus Error**

When RBE[*i*] is set, it indicates that a bus error has been detected while hashing memory region *i*.

- **RWC: Region Wrap Condition Detected**

When RWC[*i*] is set, it indicates that a wrap condition has been detected.

- **REC: Region End bit Condition Detected**

When REC[*i*] is set, it indicates that an end bit condition has been detected.

- **RSU: Region Status Updated Detected**

When RSU[*i*] is set, it indicates that a region status updated condition has been detected.

- **URAD: Undefined Register Access Detection Status**

0: No undefined register access has been detected since the last SWRST.

1: At least one undefined register access has been detected since the last SWRST.

The URAD bit is only reset by the SWRST bit in the ICM_CTRL register.

The URAT field in the ICM_UASR indicates the unspecified access type.

Master Read Mode

$$f_{SPCK}Max = \frac{1}{SPI_0(orSPI_3) + t_{valid}}$$

t_{valid} is the slave time response to output data after detecting an SPCK edge.

For a non-volatile memory with t_{valid} (or t_v) = 5 ns, f_{SPCK}max = 40 MHz at V_{DDIO} = 3.3 V.

Slave Read Mode

In Slave mode, SPCK is the input clock for the SPI. The max SPCK frequency is given by setup and hold timings SPI_7/SPI_8(or SPI_{10}/SPI_{11}). Since this gives a frequency well above the pad limit, the limit in Slave Read mode is given by the SPCK pad.

Slave Write Mode

$$f_{SPCK}Max = \frac{1}{2x(SPI_{6max}(orSPI_{9max}) + t_{setup})}$$

t_{setup} is the setup time from the master before sampling data.

Notes: 1. Current consumption per measurement channel.
2. V_{IND} may be limited by the recommended input voltage on analog input pins (+/-0.25V, refer to Table 46-5 “Recommended Operating Conditions on Input Pins”).
3. Corresponds to the maximum signal on the voltage channel(s).
4. Includes the input impedance drift with temperature.

Table 46-48. EMAFE Precision Voltage Reference and Die Temperature Sensor Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Unit
V_{VDDA}	Operating supply voltage	–	2.7	2.8	2.9	V
I_{VDDA}	Supply current	OFF	–	–	0.1	µA
		ON	–	70	100	
V_{REF_AFE0}	Output voltage initial accuracy	At T_{J0} = 23°C	1.142	1.144	1.146	V
TC_{VREF_U}	V_{REF} drift with temperature(1)	Uncompensated (SAM4CMS4 devices)	–	50	–	ppm /°C
TC_{VREF_C}		Using factory-programmed calibration registers	–	10	30	
R_{OUT}	V_{REF_AFE} output resistance	–	200	500	800	kΩ
D_{TEMP_Lin}	Die temperature sensor, digital reading linearity	–	–	±2	–	°C
I_{VREF_OFF}	Current in VREF pin when internal voltage reference is OFF	–	-100	–	100	nA

Note: 1. TC is defined using the box method: TC = ($V_{REF\_AFE\_MAX}$ - $V_{REF\_AFE\_MIN}$) / (V_{REF_AFE0} x (T_{MAX} - T_{MIN})).

Table 46-49. EMAFE VDDA LDO Regulator

Symbol	Parameter	Comments	Min	Typ	Max	Unit
V_{VDDIN}	Operating supply voltage	–	3.0	3.3	3.6	V
I_{VDDIN}	Supply current	OFF	–	–	0.1	µA
		ON	–	–	250	
I_O	Output current	–	–	–	15	mA
V_O	DC output voltage	I_O= 0 mA.	2.75	2.8V	2.85	V
$\Delta V_O / \Delta I_O$	Static load regulation	I_O: 0 to I_{OMAX}	-5	–	–	mV/mA
$\Delta V_O / \Delta V_{DDIN}$	Static line regulation	V_{DDIN}: 3.0 to 3.6V	-5	–	5	mV/V
PSRR	Power supply rejection ratio	f = DC to 2000 Hz	–	40	–	dB
		f = 1 MHz	–	40	–	
t_{ON}	Start-up time	V_O from 0 to 95% of final value. I_O= 0 mA.	–	–	1	ms
C_O	Stable output capacitor range	Capacitive	0.5	1	4.7	µF
		Resistive	5	10	300	mΩ

49. Ordering Information

Table 49-1. Ordering Codes for SAM4CM Devices

Ordering Code	MRL	Flash (Kbytes)	Package	Conditioning	Temperature Operating Range
ATSAM4CMP32CB-AU	B	2 x 1024	LQFP100	Tray	Industrial (-40°C to +85°C)
ATSAM4CMP32CB-AUR				Reel	
ATSAM4CMP32CA-AU	A			Tray	
ATSAM4CMP32CA-AUR				Reel	
ATSAM4CMP16CC-AU	C	1024		Tray	
ATSAM4CMP16CC-AUR				Reel	
ATSAM4CMP16CB-AU	B			Tray	
ATSAM4CMP16CB-AUR				Reel	
ATSAM4CMP16CA-AU	A			Tray	
ATSAM4CMP16CA-AUR				Reel	
ATSAM4CMP8CC-AU	C	512		Tray	
ATSAM4CMP8CC-AUR				Reel	
ATSAM4CMP8CB-AU	B			Tray	
ATSAM4CMP8CB-AUR				Reel	
ATSAM4CMP8CA-AU	A			Tray	
ATSAM4CMP8CA-AUR				Reel	
ATSAM4CMS32CB-AU	B	2 x 1024		Tray	
ATSAM4CMS32CB-AUR				Reel	
ATSAM4CMS32CA-AU	A			Tray	
ATSAM4CMS32CA-AUR				Reel	
ATSAM4CMS16CC-AU	C	1024		Tray	
ATSAM4CMS16CC-AUR				Reel	
ATSAM4CMS16CB-AU	B			Tray	
ATSAM4CMS16CB-AUR				Reel	
ATSAM4CMS16CA-AU	A			Tray	
ATSAM4CMS16CA-AUR				Reel	
ATSAM4CMS8CC-AU	C	512		Tray	
ATSAM4CMS8CC-AUR				Reel	
ATSAM4CMS8CB-AU	B			Tray	
ATSAM4CMS8CB-AUR				Reel	
ATSAM4CMS8CA-AU	A			Tray	
ATSAM4CMS8CA-AUR				Reel	