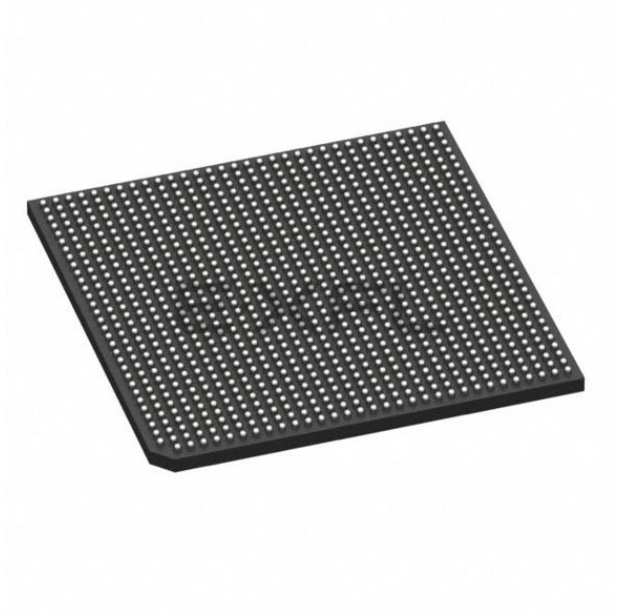

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8567evtaqgg

1 MPC8568E Overview

This section provides a high-level overview of MPC8568E features. Figure 1 shows the major functional units within the MPC8568E.

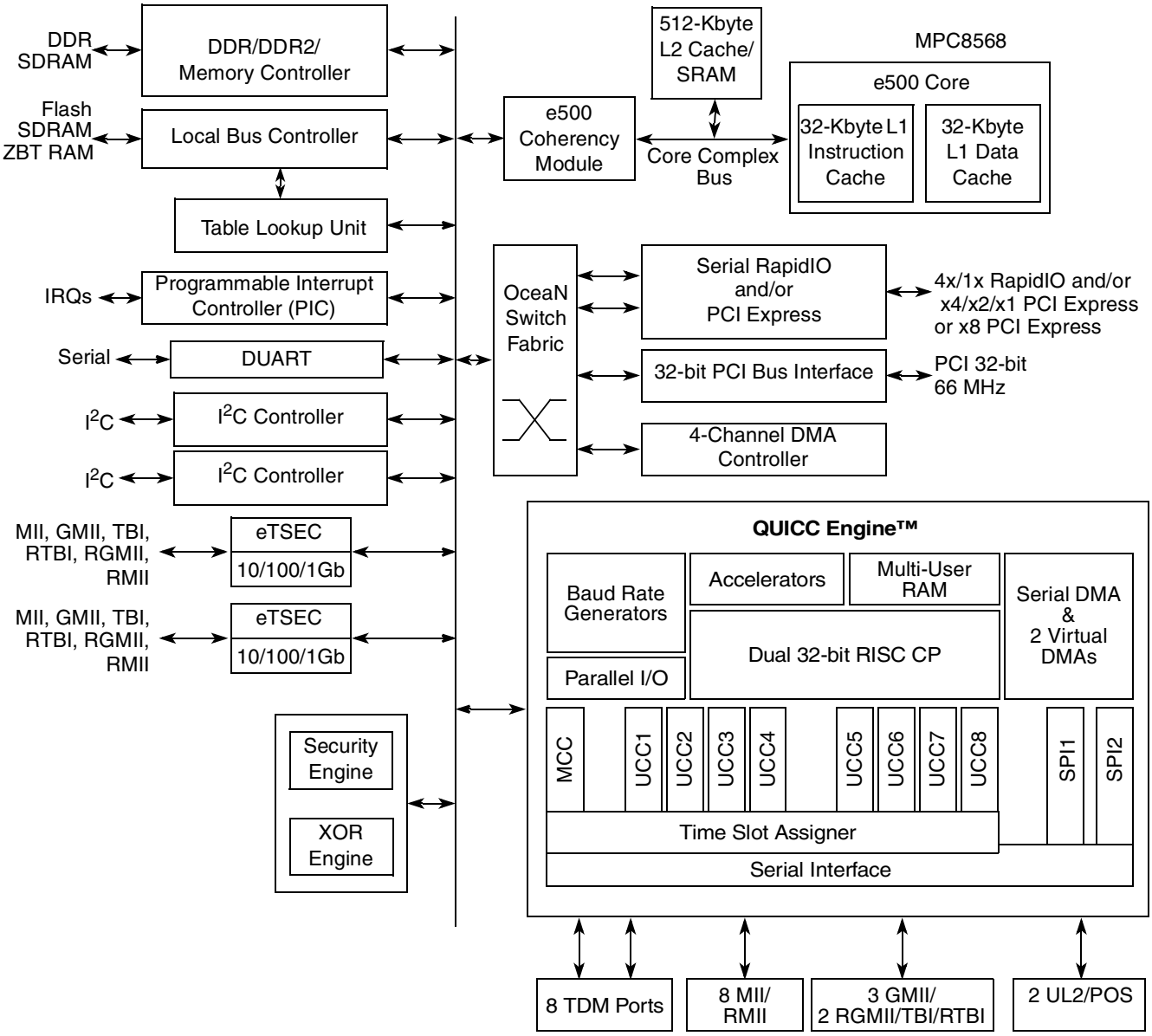

Figure 1. MPC8568E Block Diagram

Table 1. Supported eTSEC1 and eTSEC2 Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

1.2.6 DDR SDRAM Controller

The MPC8568E supports DDR SDRAM and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbits, 2 Gbits and 4 Gbits. Four chip select signals support

Table 2. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	4, 5
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)		—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	•C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	1.1 V ± 55 mV	V	—
Core power supply for SerDes transceiver	SCOREVDD	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceiver	XV_{DD}	1.1 V ± 55 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—

4.4 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8568E.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	 — —	 — —	 0.75 1.0	ns	—
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TVDD = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

4.5 FIFO Clock Speed Restrictions

Note the following FIFO maximum speed restrictions based on the platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 167 MHz

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	–0.3	MV_{REF}– 0.15	V	—
Output leakage current	I_{OZ}	–10	10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 15 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

Table 20. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8568E Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz

Figure 5 shows the DDR SDRAM output timing diagram.

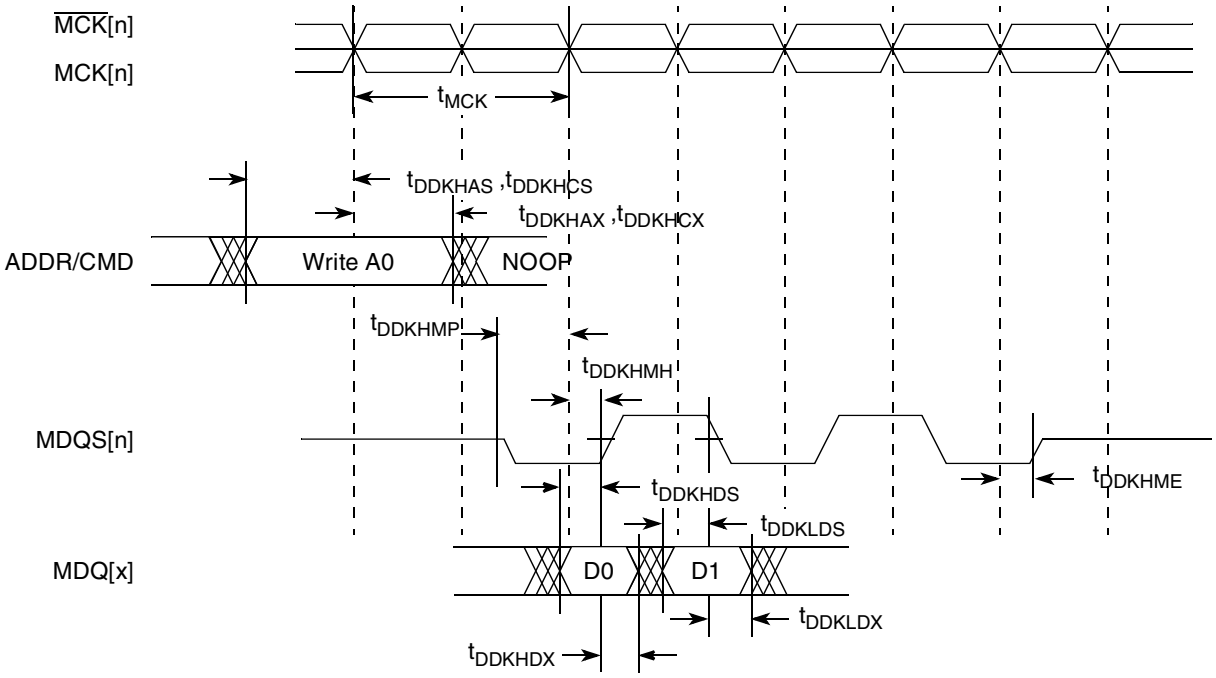

Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

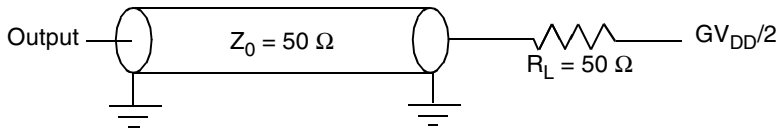

Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8568E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V

Timing diagrams for FIFO appear in Figure 7 and Figure 8.

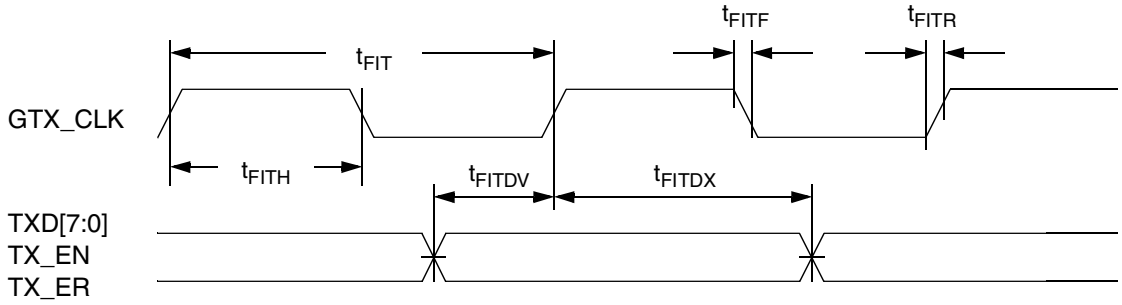

Figure 7. FIFO Transmit AC Timing Diagram

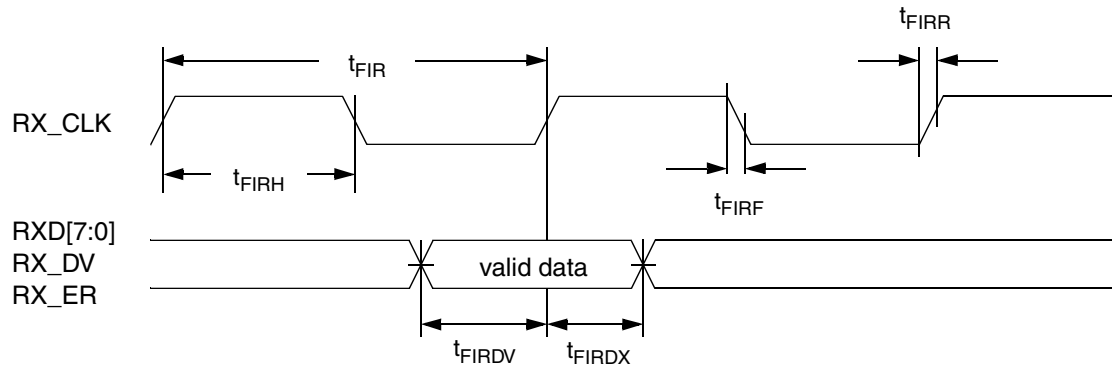

Figure 8. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	45	—	55	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}^2	—	1.0	2.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}^2	—	1.0	2.0	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	1.0	2.0	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	1.0	2.0	ns

Table 28. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	1.0	2.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 10 provides the AC test load for eTSEC.

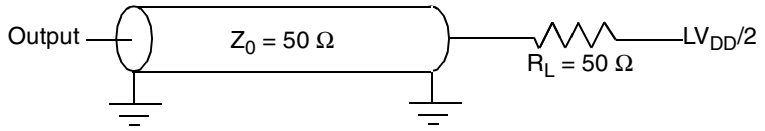

Figure 10. eTSEC AC Test Load

Figure 11 shows the GMII receive AC timing diagram.

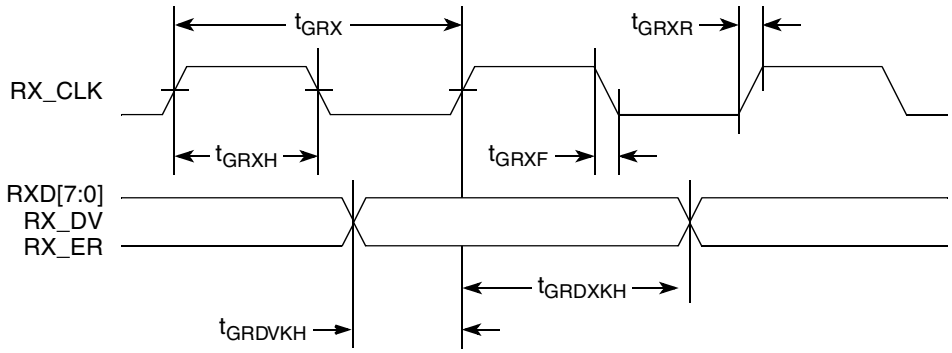

Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

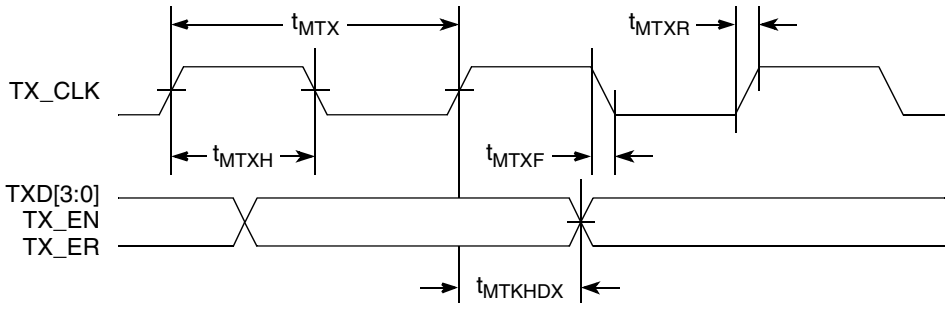

Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%

9.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 23.1, "Clock Ranges."

Table 41. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.

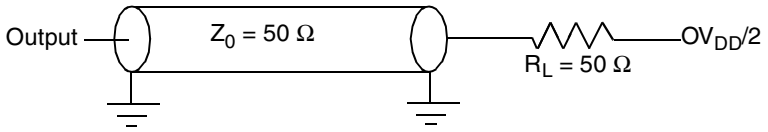

Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.

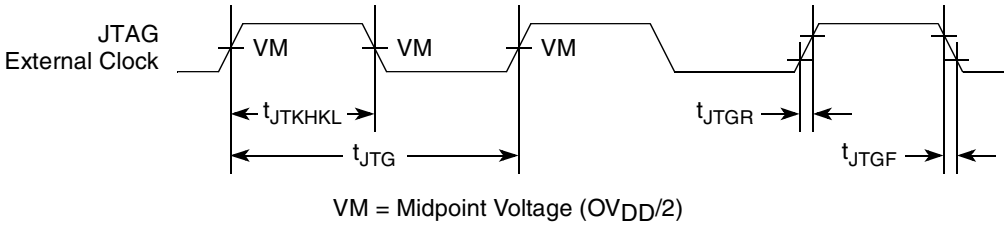

Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the $\overline{\text{TRST}}$ timing diagram.

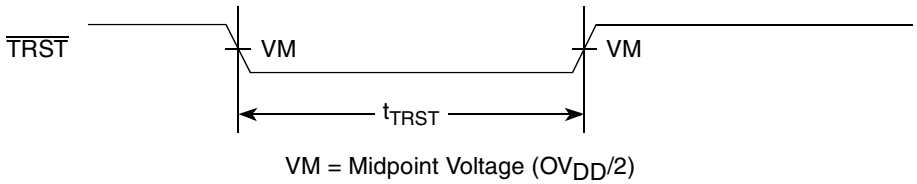

Figure 32. $\overline{\text{TRST}}$ Timing Diagram

Table 71. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

19.2 TDM/SI AC Timing Specifications

Table 72 provides the TDM/SI input and output AC timing specifications.

Table 72. TDM/SI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 60 provides the AC test load for the TDM/SI.

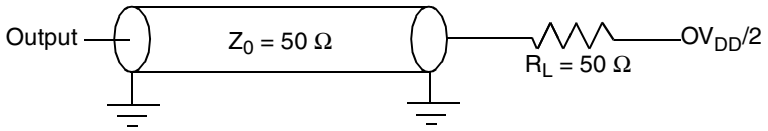

Figure 60. TDM/SI AC Test Load

Figure 61 represents the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—
PE[20]	AH6	I/O	OV_{DD}	—
PE[21:23]	AM1, AE10, AG5	I/O	OV_{DD}	5
PE[24]	AJ1	I/O	OV_{DD}	5
PE[25:31]	AH2, AM2, AE9, AH5, AL1, AD9, AL4	I/O	OV_{DD}	—
PF[7]	AG9	I/O	TV_{DD}	—
PF[8:10]	AF10, AK7, AJ6	I/O	TV_{DD}	5
PF[11:19]	AH7, AF9, AJ7, AJ5, AF7, AG8, AG7, AM5, AK5	I/O	TV_{DD}	—
PF[20]	AK1	I/O	OV_{DD}	—
PF[21:22]	AH3, AL3	I/O	OV_{DD}	5,33
PF[23:31]	AB11, AE7, AJ3, AC11, AG6, AG3, AH4, AM3, AD11	I/O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AL21	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AL23	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AK18	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AL17	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AM17	O	OV_{DD}	2,4

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 23.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor. These two pins are not ESD protected.
17. . The value of PA[0:4] during reset set the QE clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.4, "QE/SYSCLK PLL Ratio."
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx Flow Control.
24. Do not connect.
25. These are test signals for factory use only and must be pulled up (100 - 1 K) to OVDD for normal machine operation.
26. Independent supplies derived from board VDD.
27. Recommend a pull-up resistor (~1 K.) be placed on this pin to OV_{DD}.
29. The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP, PA[5]

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_REQ[4:1]	AG29, AJ27, AH29, AB17	I	OV_{DD}	—
PCI_REQ[0]	AC17	I/O	OV_{DD}	—
PCI_CLK	AM26	I	OV_{DD}	39
PCI_DEVSEL	AK23	I/O	OV_{DD}	2
PCI_FRAME	AE21	I/O	OV_{DD}	2
PCI_IDSEL	AB19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	B22, C22, E20, A19, C23, A22, A20, C20, G22, E22, E16, F16, E23, F23, F17, H17, A18, A17, B16, C16, B19, C19, E17, A16, A13, A14, A12, C12, A15, B15, B13, C13, G12, G11, H8, F8, D13, F12, E9, F9, A7, B7, C5, E5, C8, E8, D6, A5, E6, G6, E1, F1, G7, E7, E2, D1, C4, A3, B1, C1, A4, B4, C2, D2	I/O	GV_{DD}	—
MECC[0:7]	C11, E11, D9, A8, D12, A11, A9, C9	I/O	GV_{DD}	—
MDM[0:8]	A21, E21, D18, B14, F11, A6, G5, A2, A10	O	GV_{DD}	—
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
MDQS[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
MWE	K3	O	GV_{DD}	—
MCAS	L3	O	GV_{DD}	—
MRAS	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
MCS[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
MCK[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AJ20	I	OV_{DD}	25
L2_TSTCLK	AJ19	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH31	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AJ31	I	OV_{DD}	25
Thermal Management				
THERM0	AB30	—	—	14
THERM1	AB31	—	—	14
Power Management				
ASLEEP	AK21	O	OV_{DD}	9,19,29
Power and Ground Signals				
GND	A23, A26, A32, B3, B6, B9, B12, B18, B21, B23, B24, B25, B26, B27, C15, C24, D5, D8, D11, D17, D20, D23, D24, D28, E13, E14, E24, E31, F3, F7, F15, F18, F22, F24, F27, G8, G16, G19, G23, H5, H12, H13, H15, H16, H18, H19, H21, H22, J2, J7, J10, J14, J15, J16, J17, J18, J19, J20, J21, J22, J29, J31, J32, K14, K15, K16, K17, K18, K19, K20, K21, K22, K24, L1, L4, L9, L12, L15, L16, L17, L18, L19, L20, L21, L22, L23, M12, M13, M18, M20, M21, M23, N4, N8, N11, N13, N15, N17, N19, N21, N23, P2, P6, P12, P14, P16, P18, P20, P22, P23, R10, R13, R15, R17, R19, R21, R23, T12, T14, T16, T18, T20, T22, T23, U4, U8, U13, U15, U17, U19, U21, U23, V2, V6, V12, V14, V16, V18, V20, V22, V23, W10, W13, W15, W17, W19, W21, W23, Y12, Y14, Y16, Y18, Y20, Y22, Y23, AA4, AA8, AA12, AA13, AA15, AA17, AA19, AA21, AA22, AA23, AB2, AB6, AB12, AB23, AB29, AB32, AC10, AC23, AC24, AC25, AC28, AC29, AC30, AC31, AC32, AD16, AD17, AD19, AD21, AD25, AD26, AD27, AD31, AE8, AE12, AF2, AF4, AF6, AF16, AF21, AF25, AG10, AG14, AG18, AG24, AG28, AH23, AJ4, AJ8, AJ12, AJ21, AJ30, AJ32, AK2, AK10, AK16, AK32, AL6, AL14, AL18, AL19, AL20, AL22, AL24, AL25, AL26, AL31, AL32, AM19, AM21, AM23, AM25, AM30, AM31, AM32	—	—	—
SCOREGND	K28, K29, K30, L28, L31, M28, M30, N32, P28, P30, R28, T29, U32, V30, W28, W31, Y28, Y29, AA29, AA30, AA32, AB28	Ground for SerDes receiver	—	—
XGND	N24, N26, P25, R27, T24, U26, V25, W27, Y24, AA26, AB25, AC27	Ground for SerDes transmitter	—	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AV_{DD_CORE}	AM24	Power for e500 PLL (1.1V)	—	26
AV_{DD_PLAT}	AM20	Power for CCB PLL (1.1V)	—	26
AV_{DD_SRDS}	R29	Power for SRDSPLL (1.1V)	—	26
AGND_SRDS	R31	Ground for SRDSPLL	—	
SENSEVDD	M17	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A24	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	K32	I	200Ω to GND	—
SD_IMP_CAL_TX	AA28	I	100Ω to GND	—
SD_PLL_TPA	R30	O	—	24
Reserved Pins				
Reserved	AE17, AH12, AL13, AL11, AK13, AH13, AG11, AD13, AM13, AG12, AC13, AL12, AJ16, AM15, AK15	N/A	N/A	42
Reserved	AF17, AM14, AE14, AM11, AK11, AF11, AJ14, AJ13, AD12, AE13, AG13, AB13, AE11, AH11, AM12, AJ11, AB15, AB16, AE16, AG15, AF15, AH14	N/A	N/A	45

- $\overline{\text{SD\_TX}}$[7:0]

25.9.2 Unused input

25.9.2.1 SerDes block power not supplied

If the high speed interface is not used at all, then SCOREVDD/XVDD/AV_{DD_SRDS} can be tied to GND, all receiver inputs should be tied to the GND as well. This includes:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$
- $\overline{\text{SD\_RX\_CLK}}$
- $\overline{\text{SD\_RX\_FRM\_CTL}}$

25.9.2.2 SerDes Interface Partly used

If the high-speed SerDes interface is partly unused, any of the unused receiver pins should be terminated as follows:

- SD_RX[7:0] = tied to SCOREGND
- $\overline{\text{SD\_RX}}$[7:0] = tied to SCOREGND
- SD_REF_CLK = tied to SCOREGND
- $\overline{\text{SD\_REF\_CLK}}$ = tied to SCOREGND

NOTE

Power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

During HRESET/POR, the high-speed interface must be in Serial RapidIO mode and/or PCI Express mode according to the state of the PE[8:10]. Software must disable this mode through DEVDISR[SRIO] or DEVDISR[PCIE] accordingly during software initialization.

26 Ordering Information

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