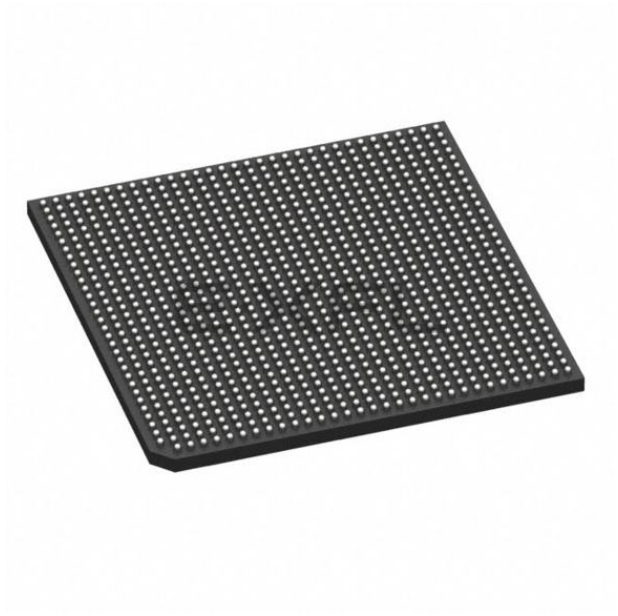

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8567evtaujj

1 MPC8568E Overview

This section provides a high-level overview of MPC8568E features. Figure 1 shows the major functional units within the MPC8568E.

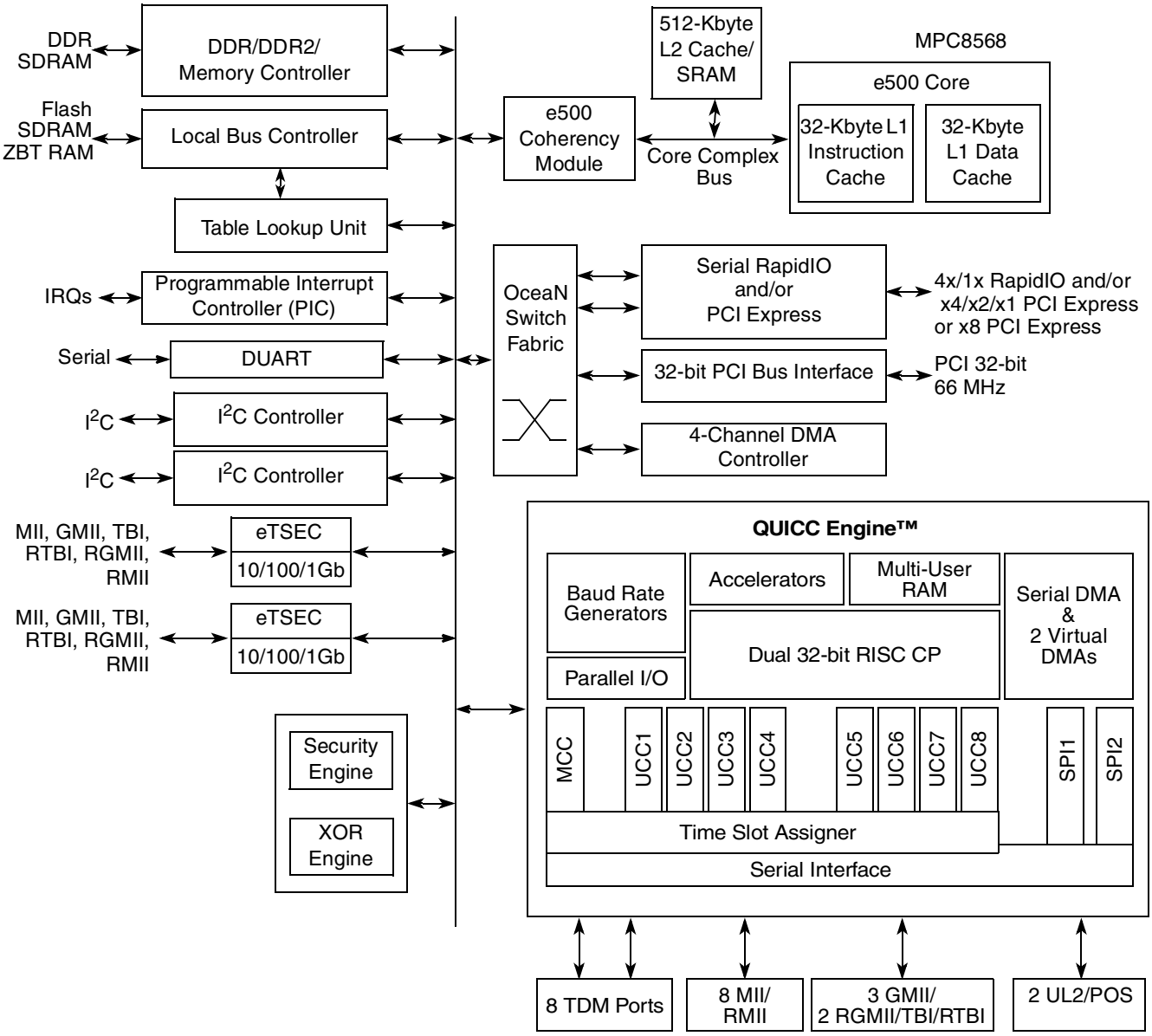


Figure 1. MPC8568E Block Diagram

Table 1. Supported eTSEC1 and eTSEC2 Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

1.2.6 DDR SDRAM Controller

The MPC8568E supports DDR SDRAM and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbits, 2 Gbits and 4 Gbits. Four chip select signals support

1.2.15 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8568E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	SCOREVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
eTSEC1, eTSEC2 I/O Voltage	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
QE UCC1/UCC2 Ethernet Interface I/O Voltage	TV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	3
Local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3

Table 6. Typical MPC8568E I/O Power Dissipation (continued)

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
eTSEC Ethernet	MII						0.01					W	Multiply with number of the interfaces
	GMII/TBI						0.07					W	
	RGMII/RTBI							0.04				W	
eTSEC FIFO I/O	16b, 200 MHz						0.20					W	Multiply with number of the interfaces
	16b, 155 MHz						0.16					W	
	8b, 200 MHz						0.11					W	
	8b, 155 MHz						0.08					W	
QE UCC	MII/RMII								0.01			W	Multiply with number of the interfaces If UCC is programmed for other protocols, scale Ethernet power dissipation to the number of signals and the clock rate
	GMII/TBI								0.07			W	
	RGMII/RTBI									0.04		W	

Note: This is the power for each individual interface. The power must be calculated for each interface being utilized.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8568E.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3

Table 7. SYSCLK AC Timing Specifications (continued)

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.2 PCI Clock Timing

Table 8 provides the PCI clock (PCI_CLK) AC timing specifications for the MPC8568E.

Table 8. PCI_CLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI_CLK frequency	f_{PCI_CLK}	—	—	66.7	MHz	—
PCI_CLK cycle time	t_{PCI_CLK}	15	—	—	ns	—
PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	1
PCI_CLK duty cycle	t_{KHK}/t_{PCI_CLK}	40	—	60	%	2
PCI_CLK jitter	—	—	—	+/– 150	ps	3,4

Notes:
1. Rise and fall times for PCI_CLK are measured at 0.4 V and 2.7 V.
2. Timing is guaranteed by design and characterization.
3. This represents the total input jitter—short term and long term—and is guaranteed by design.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the Time Base unit of the e500. There is no need for jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency. RTC may be grounded if not needed.

Table 28. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	1.0	2.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 10 provides the AC test load for eTSEC.

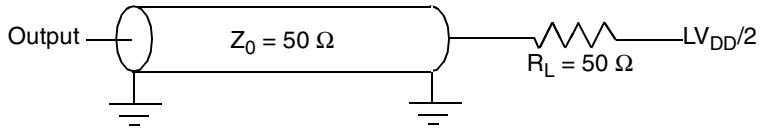


Figure 10. eTSEC AC Test Load

Figure 11 shows the GMII receive AC timing diagram.

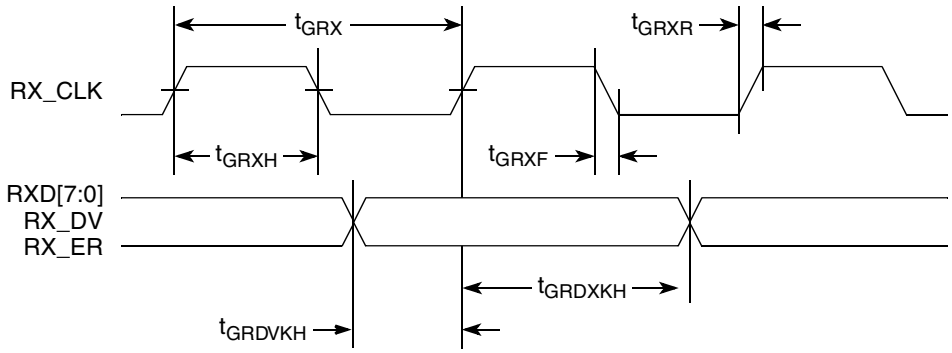


Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR} [2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF} [2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.

Figure 16 shows the TBI receive AC timing diagram.

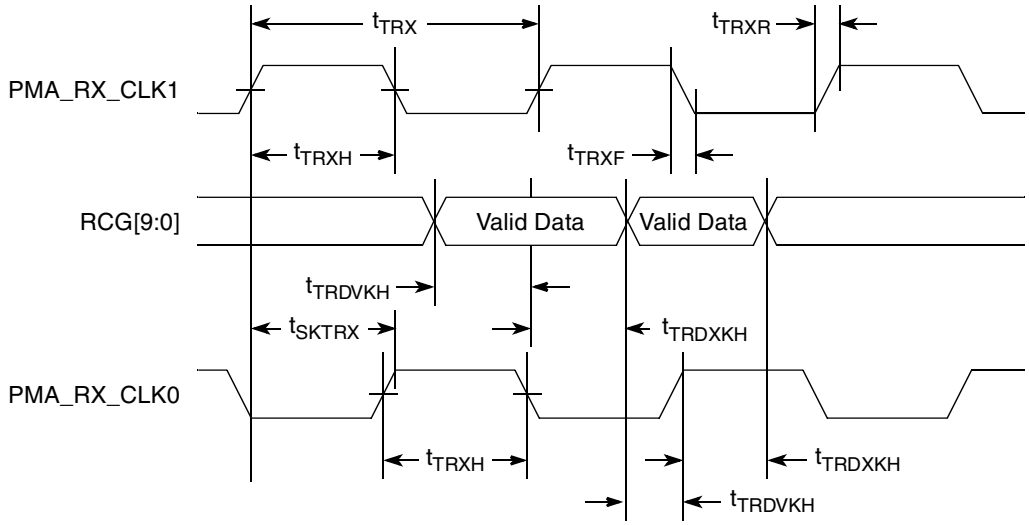


Figure 16. TBI Receive AC Timing Diagram

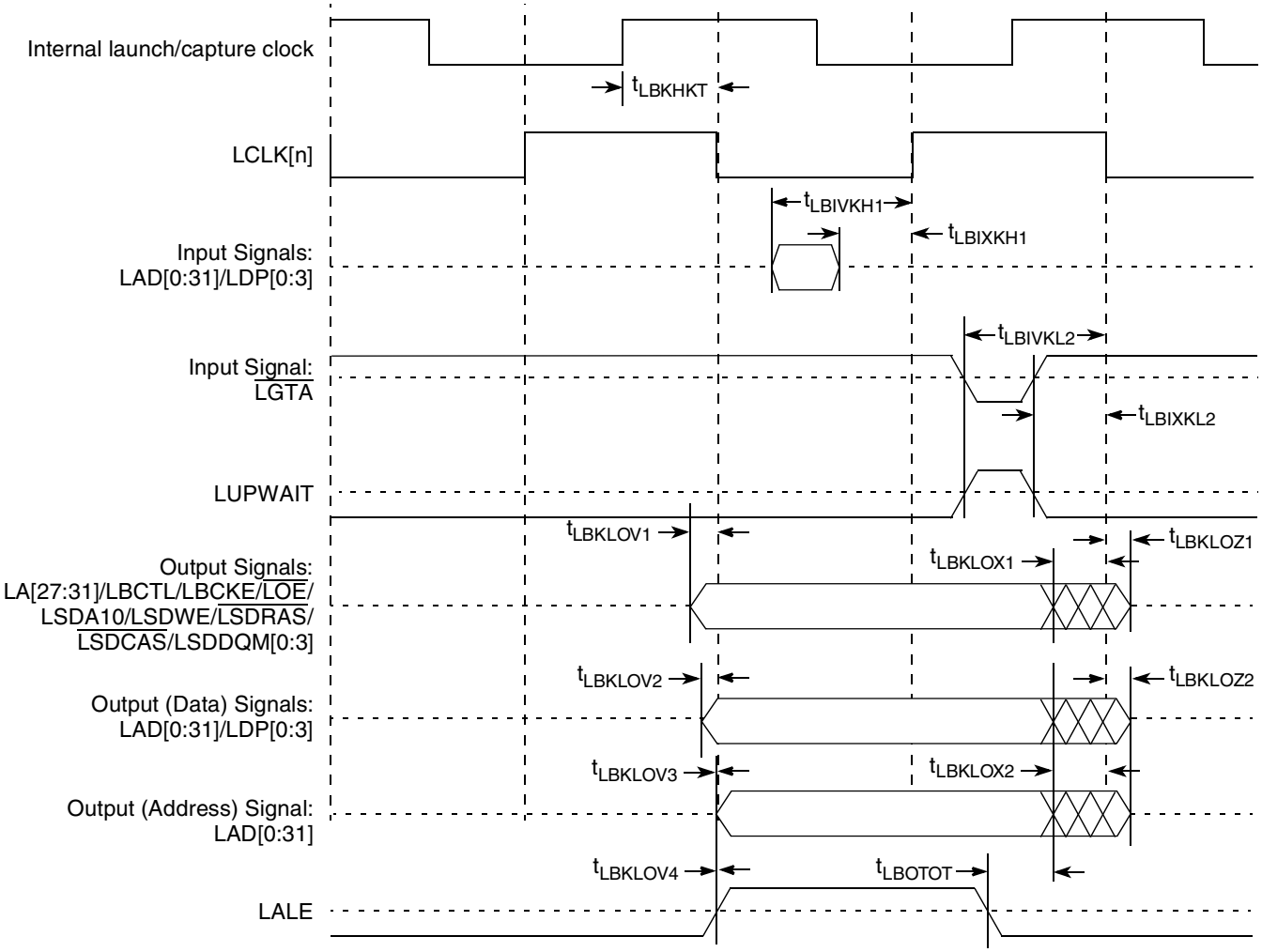


Figure 25. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

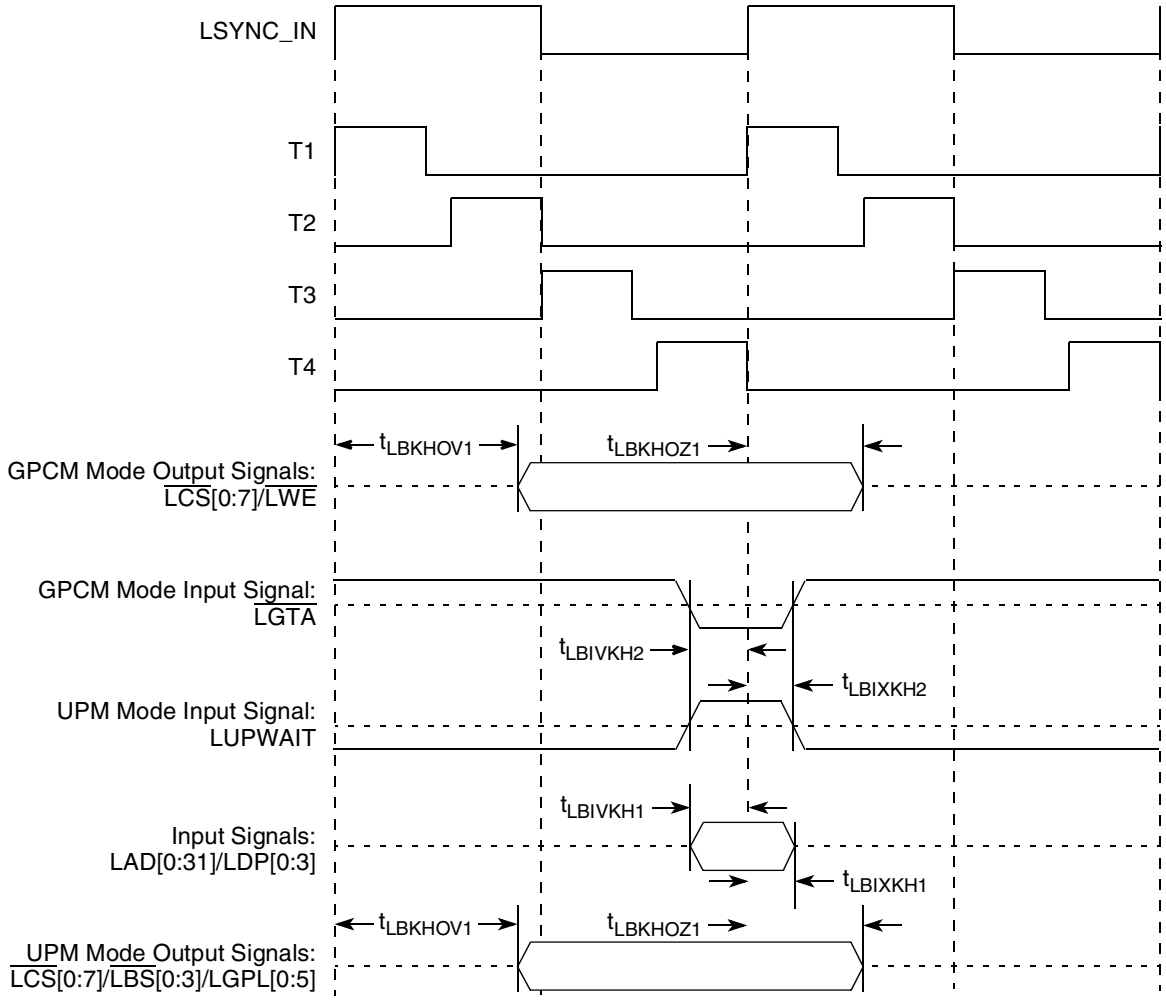


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface of the MPC8568E.

10.1 JTAG DC Electrical Characteristics

Table provides the DC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8568E.

Table 44. JTAG DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = -6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 < V_{IN} < OV_{DD}$	—	±10	uA

10.2 JTAG AC Electrical Characteristics

Table 45 provides the JTAG AC timing specifications as defined in Figure 31 through Figure 33.

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Table 47. I²C AC Electrical Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol [1]	Min	Max	Unit
Capacitive load for each bus line	C_b	—	400	pF

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8568 provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8568 acts as the I²C bus master while transmitting, the MPC8568 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8568 would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8568 as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*

Figure 30 provides the AC test load for the I²C.

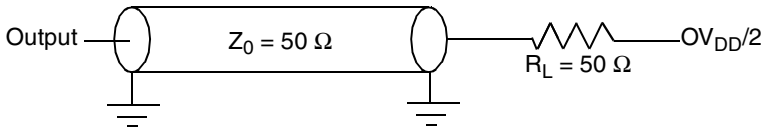


Figure 34. I²C AC Test Load

Figure 35 shows the AC timing diagram for the I²C bus.

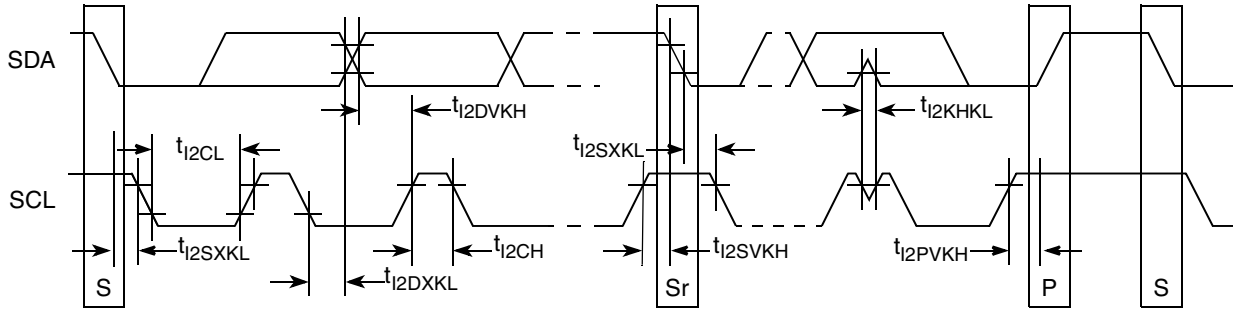


Figure 35. I²C Bus AC Timing Diagram

Figure 38 shows the PCI output AC timing conditions.

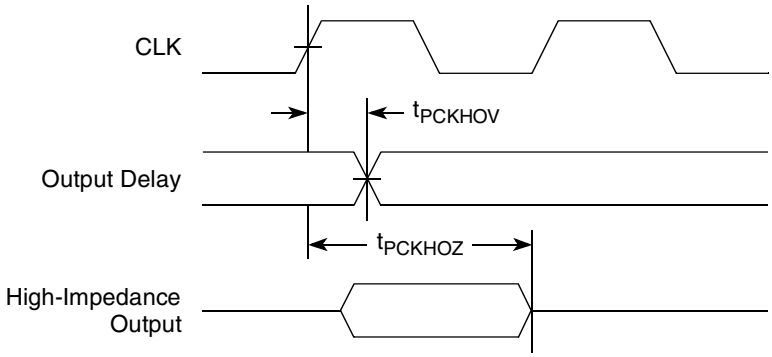


Figure 38. PCI Output AC Timing Measurement Condition

13 High-Speed Serial Interfaces (HSSI)

The MPC8568E features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. It can be used for PCI Express and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 39 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

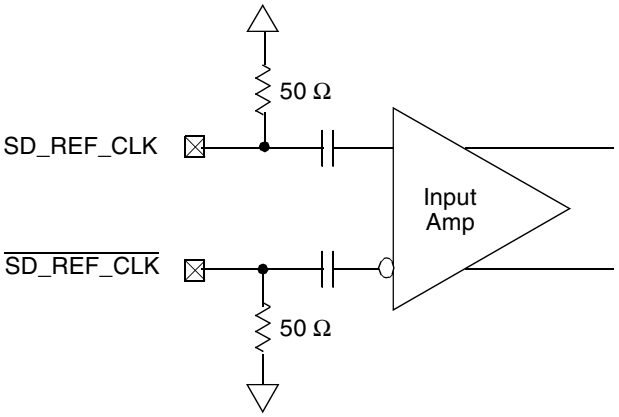


Figure 40. Receiver of SerDes Reference Clocks

13.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8568E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in section 13.2.1, the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 41 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SCOREGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SCOREGND). Figure 42 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 43 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC

or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

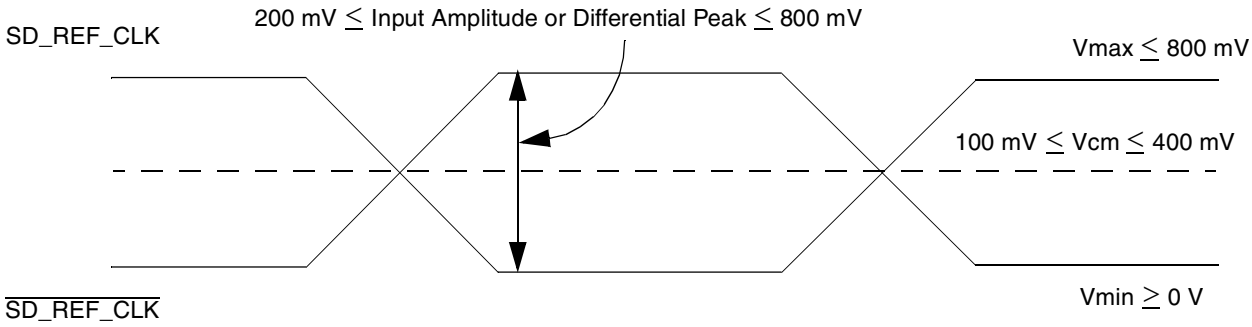


Figure 41. Differential Reference Clock Input DC Requirements (External DC-Coupled)

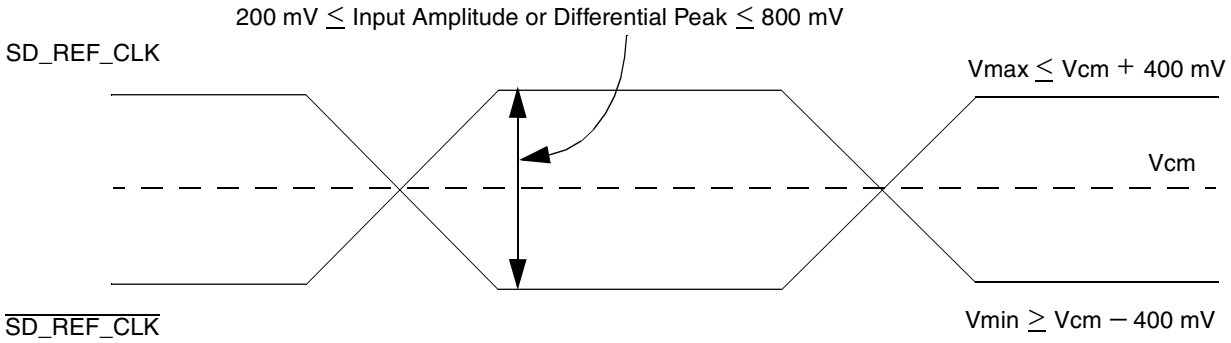


Figure 42. Differential Reference Clock Input DC Requirements (External AC-Coupled)

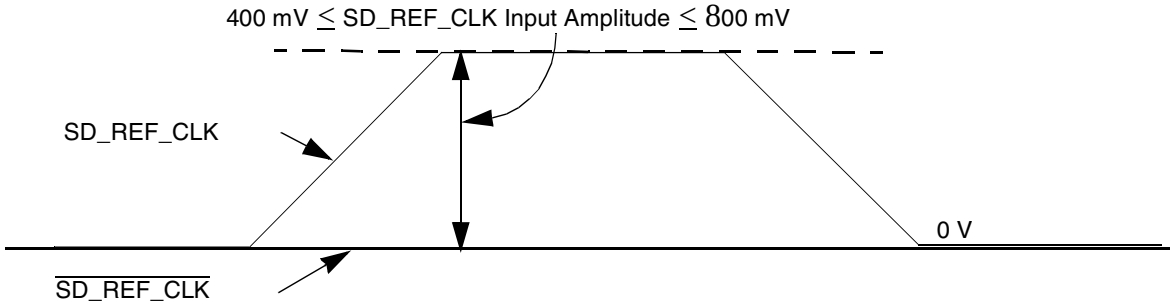


Figure 43. Single-Ended Reference Clock Input DC Requirements

17 PIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8568E.

17.1 PIC DC Electrical Characteristics

Table 67 provides the DC electrical characteristics for the external interrupt pins of the MPC8568E.

Table 67. PIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—		±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

17.2 PIC AC Timing Specifications

Table 68 provides the PIC input and output AC timing specifications.

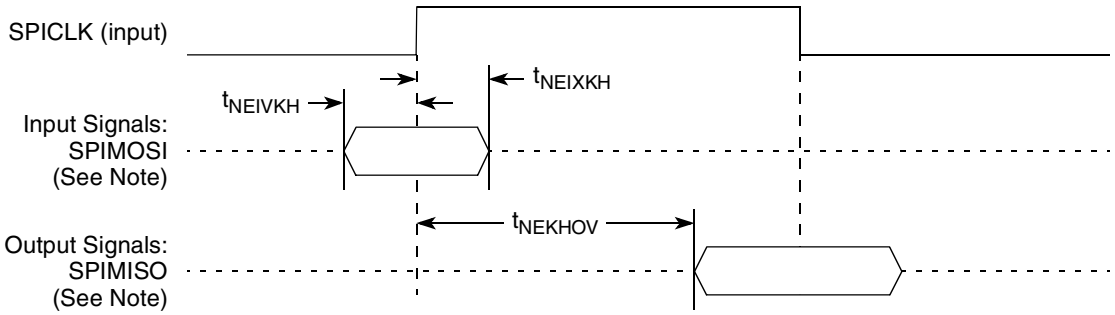
Table 68. PIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

Figure 58 through Figure 59 represent the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

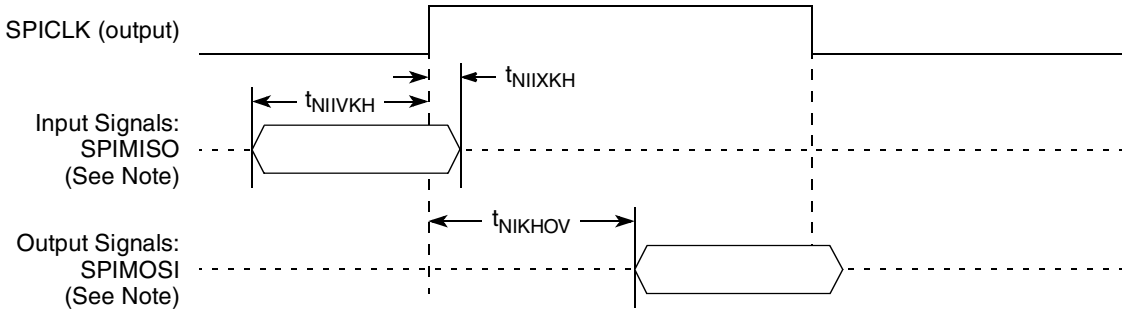
Figure 58 shows the SPI timing in Slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 58. SPI AC Timing in Slave mode (External Clock) Diagram

Figure 59 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 59. SPI AC Timing in Master mode (Internal Clock) Diagram

19 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8568E.

19.1 TDM/SI DC Electrical Characteristics

Table 71 provides the DC electrical characteristics for the MPC8568E TDM/SI.

Table 71. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V

Table 71. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

19.2 TDM/SI AC Timing Specifications

Table 72 provides the TDM/SI input and output AC timing specifications.

Table 72. TDM/SI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 60 provides the AC test load for the TDM/SI.

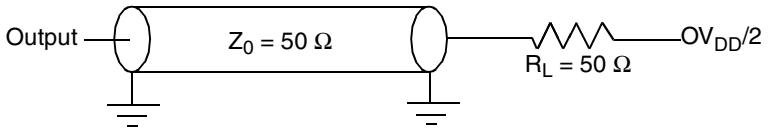


Figure 60. TDM/SI AC Test Load

Figure 61 represents the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TX_CLK	AJ11	I	LV_{DD}	—
TSEC1_TX_EN	AC13	O	LV_{DD}	30
TSEC1_TX_ER	AL12	O	LV_{DD}	5,9
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	AC14, AD15, AB14, AH15, AD14, AH17, AE15, AC15	I	LV_{DD}	—
TSEC2_TXD[7]	AM16	O	LV_{DD}	5, 9
TSEC2_TXD[6:1]	AJ15, AJ17, AF13, AK17, AH16, AG17	O	LV_{DD}	—
TSEC2_TXD[0]	AL15	O	LV_{DD}	5, 9
TSEC2_COL	AB15	I	LV_{DD}	—
TSEC2_CRS	AB16	I/O	LV_{DD}	20
TSEC2_GTX_CLK	AJ16	O	LV_{DD}	—
TSEC2_RX_CLK	AE16	I	LV_{DD}	—
TSEC2_RX_DV	AG15	I	LV_{DD}	—
TSEC2_RX_ER	AF15	I	LV_{DD}	—
TSEC2_TX_CLK	AH14	I	LV_{DD}	—
TSEC2_TX_EN	AM15	O	LV_{DD}	30
TSEC2_TX_ER	AK15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:7]	AM16, AJ15, AJ17, AF13, AK17, AH16, AG17, AL15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PE[20]	AH6	I/O	OV_{DD}	—
PE[21:23]	AM1, AE10, AG5	I/O	OV_{DD}	5
PE[24]	AJ1	I/O	OV_{DD}	5
PE[25:31]	AH2, AM2, AE9, AH5, AL1, AD9, AL4	I/O	OV_{DD}	—
PF[7]	AG9	I/O	TV_{DD}	—
PF[8:10]	AF10, AK7, AJ6	I/O	TV_{DD}	5
PF[11:19]	AH7, AF9, AJ7, AJ5, AF7, AG8, AG7, AM5, AK5	I/O	TV_{DD}	—
PF[20]	AK1	I/O	OV_{DD}	—
PF[21:22]	AH3, AL3	I/O	OV_{DD}	5,33
PF[23:31]	AB11, AE7, AJ3, AC11, AG6, AG3, AH4, AM3, AD11	I/O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AL21	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AL23	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AK18	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AL17	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AM17	O	OV_{DD}	2,4
Debug				
TRIG_IN	AL29	I	OV_{DD}	—
TRIG_OUT	AM29	O	OV_{DD}	6,9,19, 29
MSRCID[0:1]	AK29, AJ29	O	OV_{DD}	5,6,9
MSRCID[2:4]	AM28, AL28, AK27	O	OV_{DD}	6,19,29
MDVAL	AJ28	O	OV_{DD}	6
CLK_OUT	AF18	O	OV_{DD}	11
Clock				
RTC	AH20	I	OV_{DD}	—
SYSCLK	AK22	I	OV_{DD}	—
JTAG				
TCK	AH18	I	OV_{DD}	—
TDI	AH19	I	OV_{DD}	12
TDO	AJ18	O	OV_{DD}	11
TMS	AK19	I	OV_{DD}	12
$\overline{\text{TRST}}$	AK20	I	OV_{DD}	12