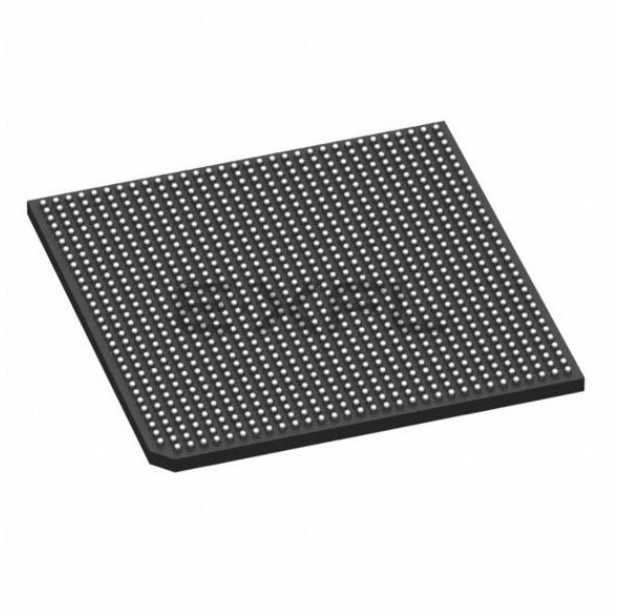


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8568ecvtaqgg

up to four banks of memory. The MPC8568E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes (MDM[0:8]) are used to provide byte selection for memory bank writes.

The MPC8568E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8568E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8568E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

1.2.7 Table Lookup Unit (TLU)

The table lookup unit (TLU) provides access to application-defined routing topology and control tables in external memory. It accesses an external memory array attached to the local bus controller (LBC). Communication between the CPU and the TLU occurs via messages passed through the TLU's memory-mapped configuration and status registers.

The TLU provides resources for efficient generation of table entry addresses in memory, hash generation of addresses, and binary table searching algorithms for both exact-match and longest-prefix-match strategies.It supports the following TLU complex table types:

- Hash-Trie-Key table for hash-based exact-match algorithms
- Chained-Hash table for partially indexed and hashed exact-match algorithms
- Longest-prefix-match algorithm
- Flat-Data table for retrieving search results and simple indexed algorithms

1.2.8 PCI Controller

The MPC8568E supports one 32-bit PCI controller, which supports speeds of up to 66 MHz. Other features include:

- Compatible with the *PCI Local Bus Specification, Revision 2.2*, supporting 32- and 64-bit addressing
- Can function as host or agent bridge interface
- As a master, supports read and write operations to PCI memory space, PCI I/O space, and PCI configuration space
- Can generate PCI special-cycle and interrupt-acknowledge commands. As a target, it supports read and write operations to system memory as well as configuration accesses.
- Supports PCI-to-memory and memory-to-PCI streaming, memory prefetching of PCI read accesses, and posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible with selectable hardware-enforced coherency

Table 6. Typical MPC8568E I/O Power Dissipation (continued)

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
eTSEC Ethernet	MII						0.01					W	Multiply with number of the interfaces
	GMII/TBI						0.07					W	
	RGMII/RTBI							0.04				W	
eTSEC FIFO I/O	16b, 200 MHz						0.20					W	Multiply with number of the interfaces
	16b, 155 MHz						0.16					W	
	8b, 200 MHz						0.11					W	
	8b, 155 MHz						0.08					W	
QE UCC	MII/RMII								0.01			W	Multiply with number of the interfaces If UCC is programmed for other protocols, scale Ethernet power dissipation to the number of signals and the clock rate
	GMII/TBI								0.07			W	
	RGMII/RTBI									0.04		W	

Note: This is the power for each individual interface. The power must be calculated for each interface being utilized.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8568E.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

Table 24. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

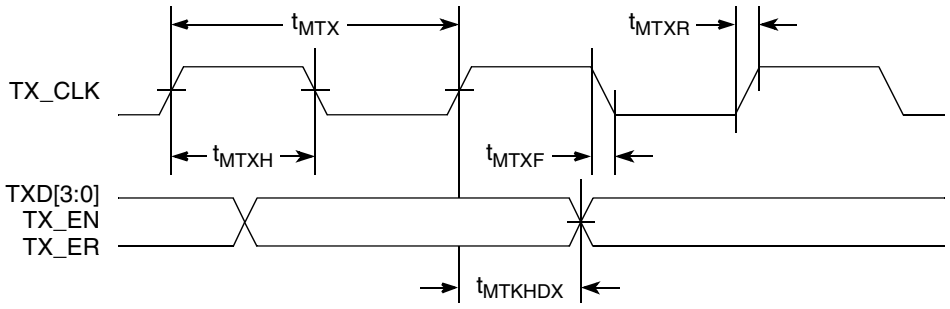


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n* TSECn_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	1.0	2.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	1.0	2.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

A timing diagram for TBI receive appears in Figure 17.

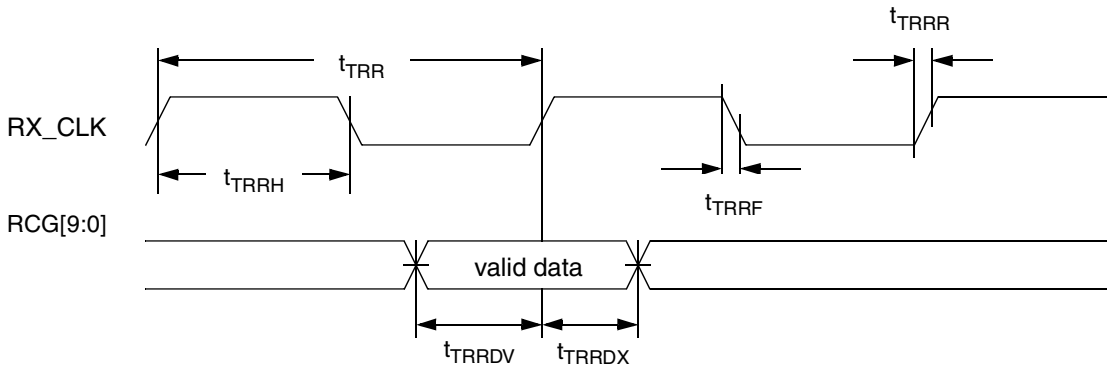


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}[5]	7.2	8.0	8.8	ns

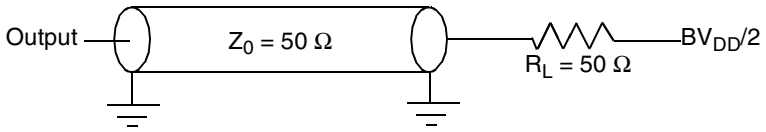


Figure 23. Local Bus AC Test Load

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 24 to Figure 29 show the local bus signals.

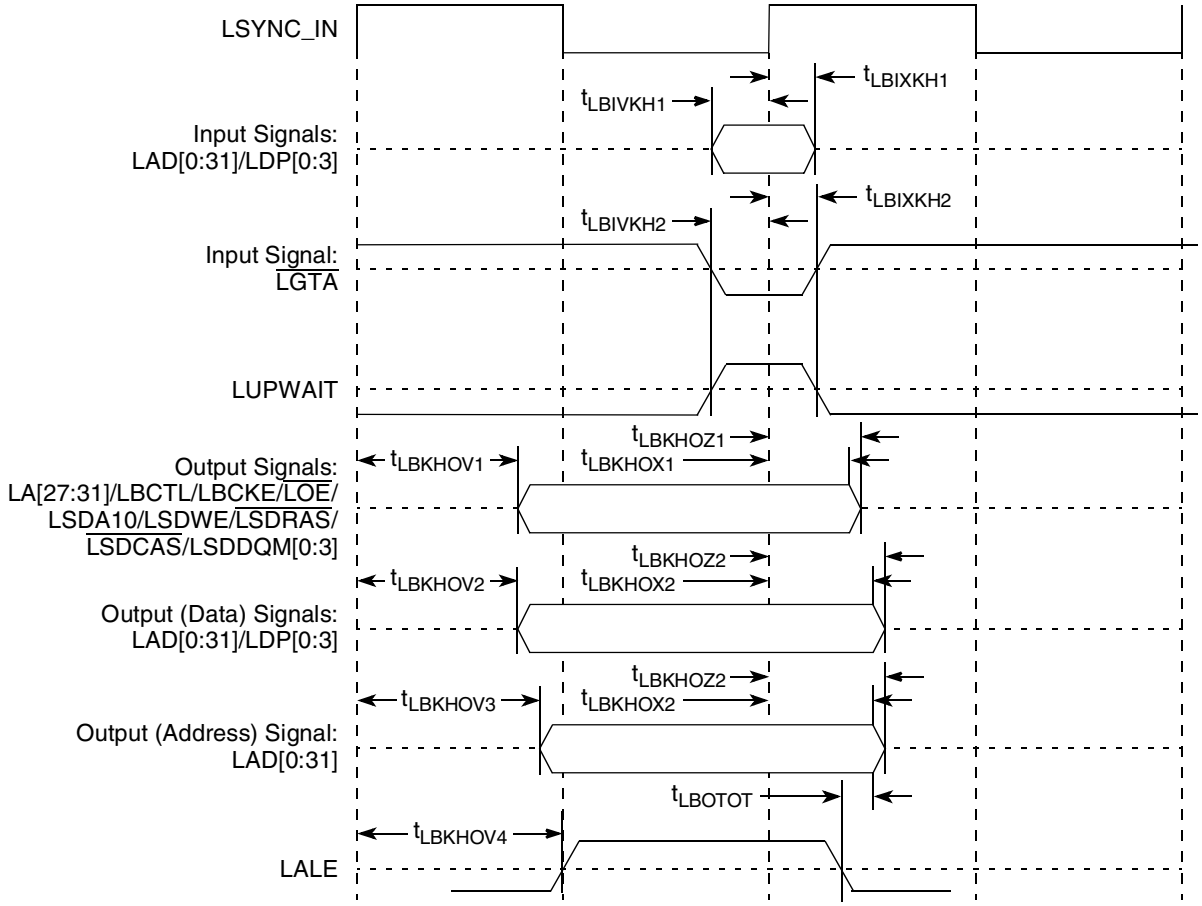


Figure 24. Local Bus Signals (PLL Enabled)

Table 43 describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V with PLL disabled.

Table 43. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—

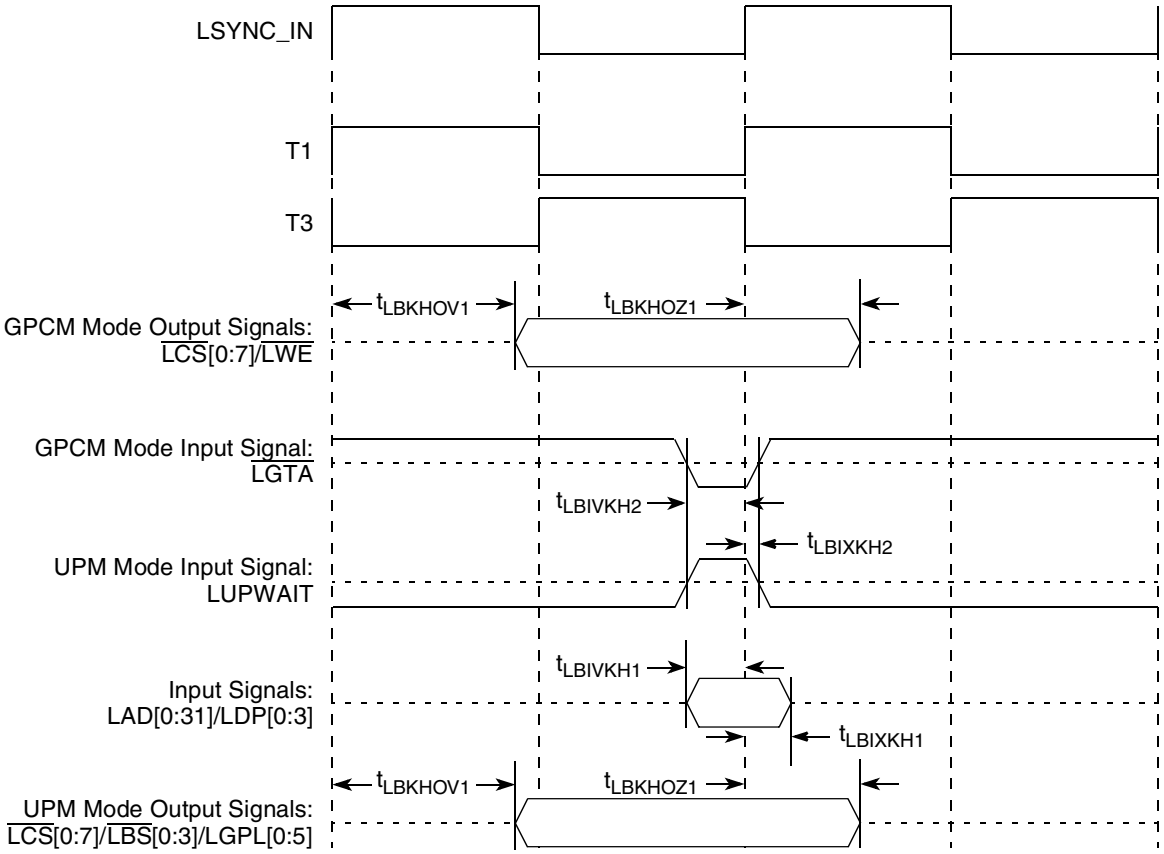


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

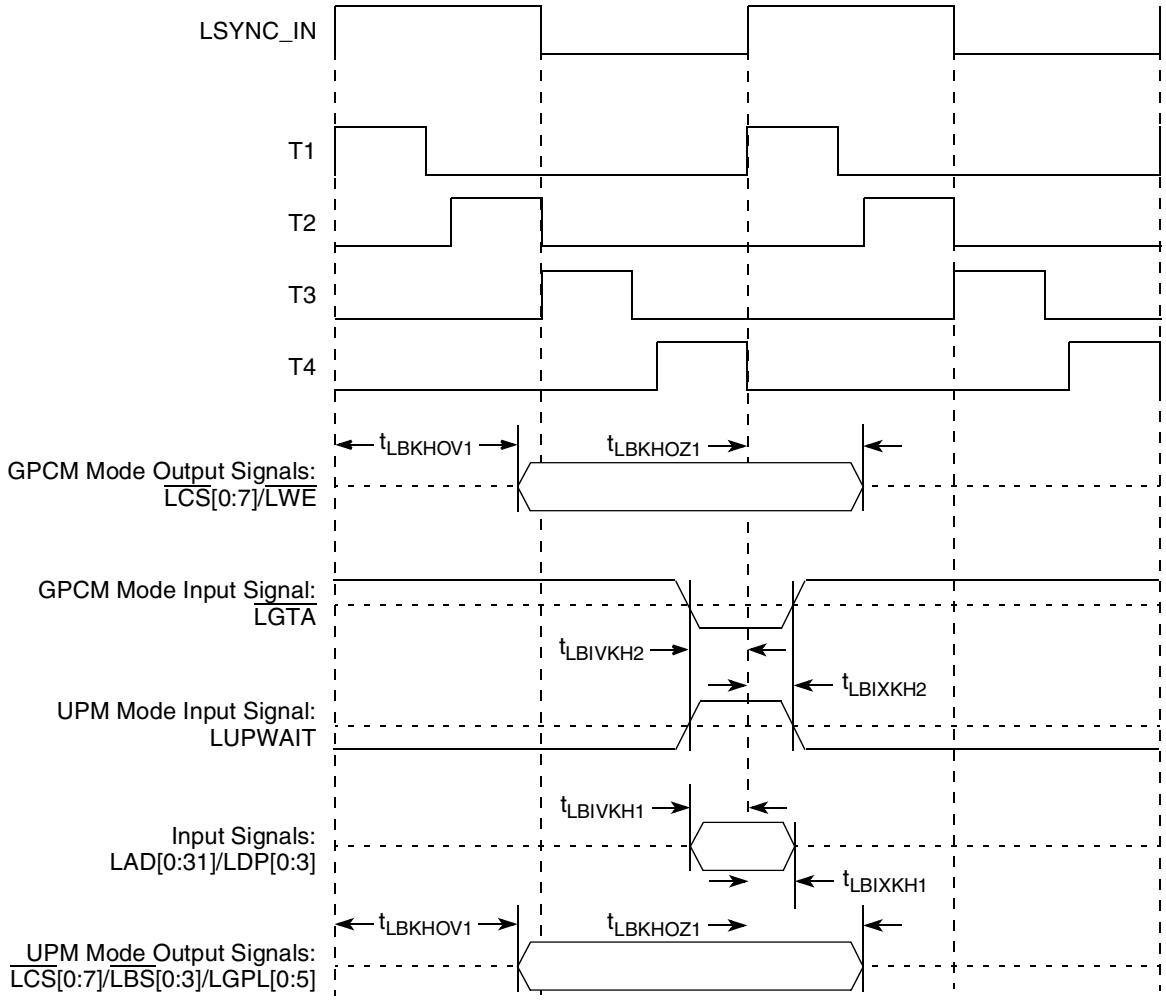


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 62. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 63. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

17 PIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8568E.

17.1 PIC DC Electrical Characteristics

Table 67 provides the DC electrical characteristics for the external interrupt pins of the MPC8568E.

Table 67. PIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—		±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

17.2 PIC AC Timing Specifications

Table 68 provides the PIC input and output AC timing specifications.

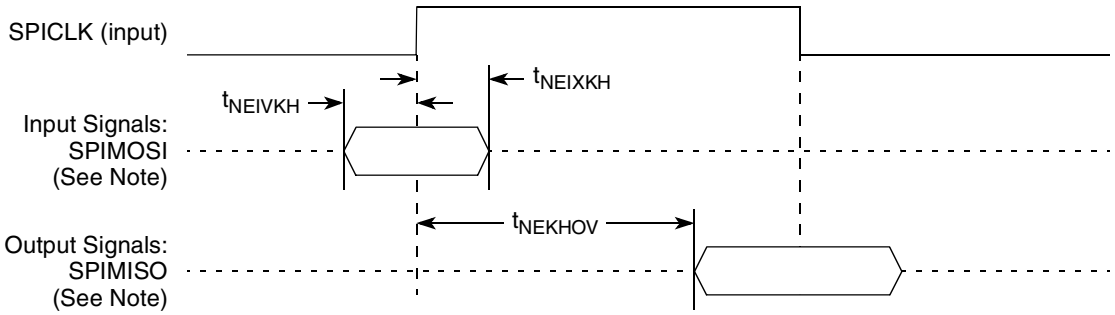
Table 68. PIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

Figure 58 through Figure 59 represent the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

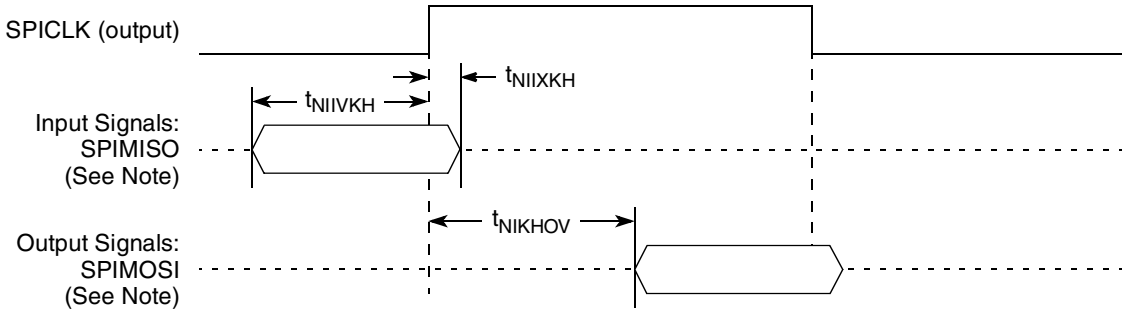
Figure 58 shows the SPI timing in Slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 58. SPI AC Timing in Slave mode (External Clock) Diagram

Figure 59 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 59. SPI AC Timing in Master mode (Internal Clock) Diagram

19 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8568E.

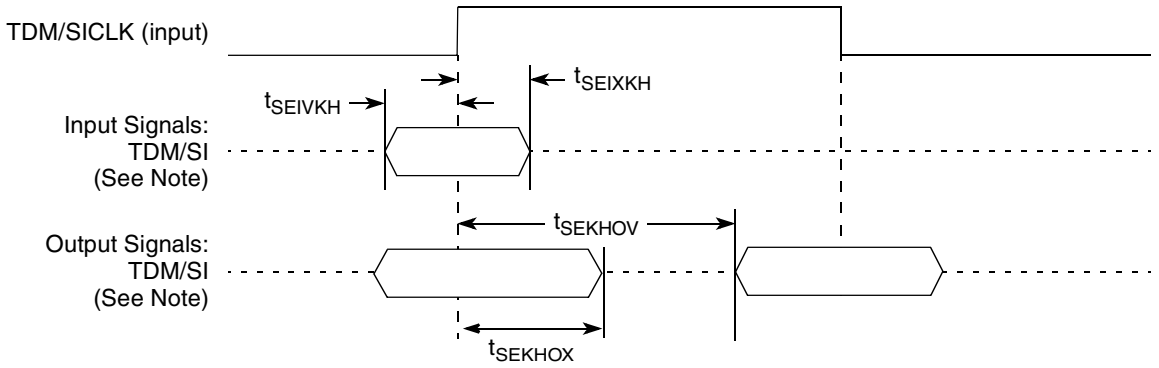
19.1 TDM/SI DC Electrical Characteristics

Table 71 provides the DC electrical characteristics for the MPC8568E TDM/SI.

Table 71. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V

Figure 61 shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI

Figure 61. TDM/SI AC Timing (External Clock) Diagram

20 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA-packet over sonnet of the MPC8568E.

20.1 UTOPIA/POS DC Electrical Characteristics

Table 73 provides the DC electrical characteristics for the MPC8568E UTOPIA.

Table 73. Utopia DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	μA

20.2 Utopia/POS AC Timing Specifications

Table 74 provides the UTOPIA input and output AC timing specifications.

Table 74. Utopia AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
Utopia outputs—Internal clock delay	t_{UIKHOV}	0	8.0	ns
Utopia outputs—External clock delay	t_{UEKHOV}	1	10.0	ns
Utopia outputs—Internal clock High Impedance	t_{UIKHOX}	0	8.0	ns
Utopia outputs—External clock High Impedance	t_{UEKHOX}	1	10.0	ns

Table 76. HDLC, BiSync, Transparent AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 77. Synchronous UART AC Timing Specifications

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns
Outputs—External clock delay	t_{HEKHOV}	1	14	ns
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	11	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 65 provides the AC test load.

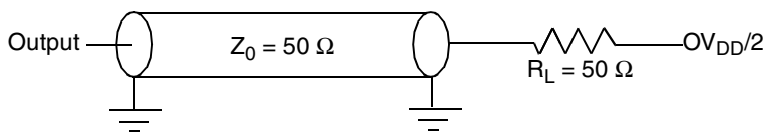


Figure 65. AC Test Load

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

Table 79 provides the pin-out listing for the MPC8567E 1023 FC-PBGA package.

Table 79. MPC8567E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	—
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALE	G31	O	BVdd	8
LBCTL	L27	O	BVdd	8
$\overline{\text{LCS}}$[0:4]	M27, H32, J28, J30, B31	O	BV_{DD}	—
$\overline{\text{LCS5}}$	G25	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$	C29	O	BV_{DD}	1
$\overline{\text{LCS7}}$	A30	O	BV_{DD}	1
$\overline{\text{LWE}}$[0]	H30	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[1]	E28	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[2]	E32	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[3]	G27	O	BV_{DD}	5,9
LGPL0	E30	O	BV_{DD}	5,9
LGPL1	J27	O	BV_{DD}	5,9,46
LGPL2	D32	O	BV_{DD}	5,8,9
LGPL3	J25	O	BV_{DD}	5,9
LGPL4	C25	I/O	BV_{DD}	49
LGPL5	F32	O	BV_{DD}	5,9
LCKE	C31	O	BV_{DD}	—
LCLK[0:2]	C27, C26, D25	O	BV_{DD}	—
LSYNC_IN	A28	I	BV_{DD}	—
LSYNC_OUT	A27	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0]	AM27	O	OV_{DD}	5,9,47
$\overline{\text{DMA\_DREQ}}$[0]	AK28	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0]	AK26	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AG32	I	OV_{DD}	—
$\overline{\text{MCP}}$	AF32	I	OV_{DD}	—
IRQ[0:7]	AD30, AG31, AL30, AF31, AD29, AK30, AG30, AF30	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	AD28	O	OV_{DD}	2,4
GPIO				
GPIN[0:7]	AC14, AD15, AB14, AH15, AD14, AH17, AE15, AC15	I	LV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:7]	AM16, AJ15, AJ17, AF13, AK17, AH16, AG17, AL15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—

Table 81. DDR/DDR2 Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
DDR/DDR2 Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the platform clock frequency.

Table 82. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	166	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by CCB clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for more information on this.

23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB) and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 83:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 83. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1

Table 85. QE Clock Multiplier cfg_ce_pll[0:4] (continued)

Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]	Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]
0_1000	8	1_1000	24
0_1001	9	1_1001	25
0_1010	10	1_1010	26
0_1011	11	1_1011	27
0_1100	12	1_1100	28
0_1101	13	1_1101	29
0_1110	14	1_1110	30
0_1111	15	1_1111	31

23.5 Frequency Options

23.5.1 SYSCLK to Platform Frequency Options

Table 86 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 86. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB clock to SYSCLK Ratio	SYSCLK (MHz)									
	16.66	25	33.33	41.66	66.66	83	100	111	133.33	166
	Platform /CCB clock Frequency (MHz)									
2										333
3								333	400	500
4						333	400	445	533	
5					333	415	500			
6					400	500				
8				333	533					
9				375						
10			333	417						
12			400	500						
16		400	533							
20	333	500								

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 1023FC-PBGA the footprint, without the inductance of vias.

Figure 73 shows the PLL power supply filter circuits for all PLLs except SerDes PLL.

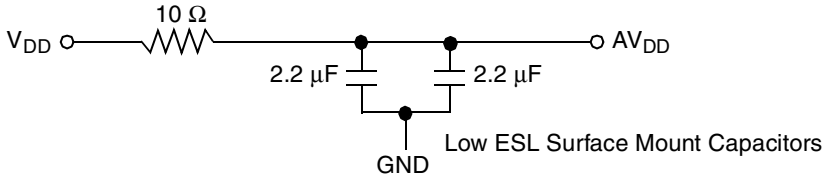
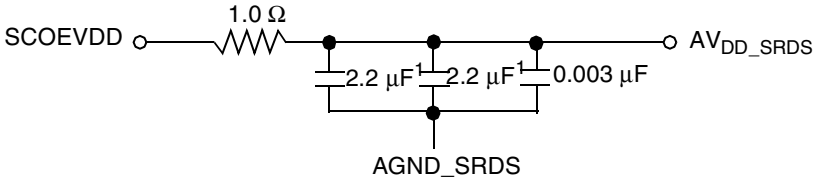


Figure 73. MPC8568E PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} and AGND_SRDS ball to ensure it filters out as much noise as possible. The 0.003-µF capacitor is closest to the ball, followed by the 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 74. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD_SRDS} should be a filtered version of SCOREVDD.
- The transmitter output signals on the SerDes interface are fed from the XV_{DD} power plan.
- Power: XVDD consumes less than 300mW. SCOREVDD + AV_{DD_SRDS} consumes less than 750mW.

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. MPC8568E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.