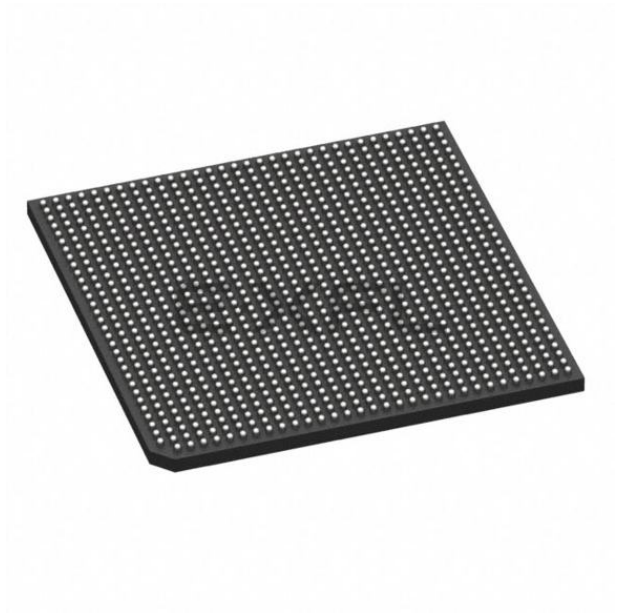


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8568evtaqgg

1.1 MPCP8568E Key Features

- High-performance, Power Architecture® e500v2 core with 36-bit physical addressing
- 512 Kbytes of level-2 cache
- QUICC Engine (QE)
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- A 1x/4x Serial RapidIO® and/or x1/x2/x4 PCI Express interface. If x8 PCI Express is needed, then RapidIO is not available due to the limitation of the pin multiplexing.
- Programmable interrupt controller (PIC)
- Four-channel DMA controller, two I^2C controllers, DUART, and local bus controller (LBC)

NOTE

The MPC8568E and MPC8567E are also available without a security engine in a configuration known as the MPC8568 and MPC8567. All specifications other than those relating to security apply to the MPC8568 and MPC8567 exactly as described in this document.

1.2 MPC8568E Architecture Overview

1.2.1 e500 Core and Memory Unit

The MPC8568E contains a high-performance, 32-bit, Book E–enhanced e500v2 Power Architecture core. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- Double-precision floating-point APU—Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs
- Embedded vector and scalar single-precision floating-point APUs—Provide an instruction set for single-precision (32-bit) floating-point instructions

The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.

— Three 1-Gbps Ethernet interfaces using three GMII, two RGMII/TBI/RTBI
— Up to eight 10/100-Mbps Ethernet interfaces using MII or RMII
— Up to eight T1/E1/J1/E3 or DS-3 serial interfaces

1.2.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8568E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
- Compatible with code written for the Freescale MPC8541E and MPC8555E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  — PKEU—public key execution unit
  — DEU—Data Encryption Standard execution unit
  — AESU—Advanced Encryption Standard unit
  — AFEU—ARC four execution unit
  — MDEU—message digest execution unit
  — KEU—Kasumi execution unit
  — RNG—Random number generator

1.2.5 Enhanced Three-Speed Ethernet Controllers

The MPC8568E has two on-chip enhanced three-speed Ethernet controllers (eTSECs). The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

The MPC8568E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab-compatible.

The buffer descriptors are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

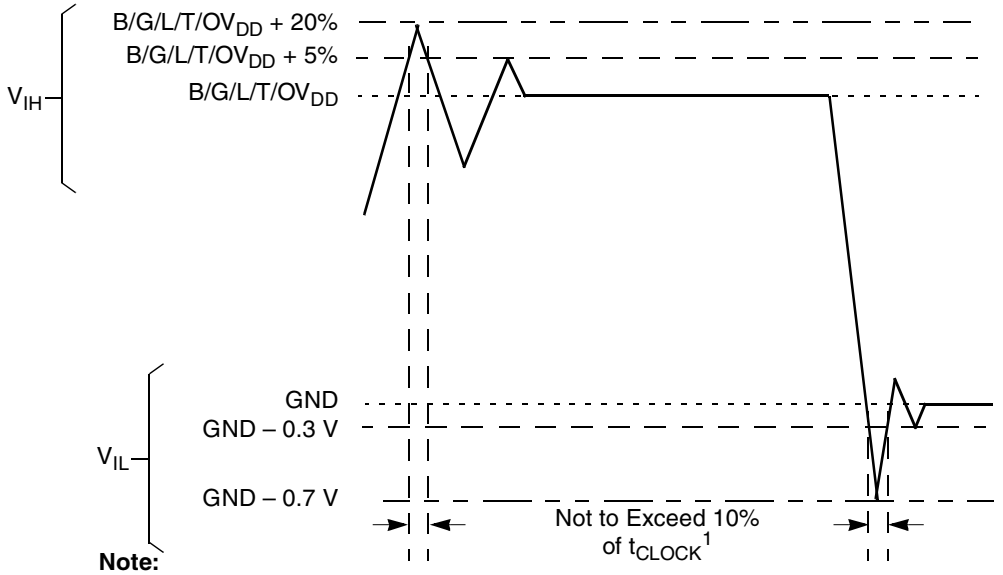
Some of the key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	—
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
Junction temperature range		Tj	0 to105	°C	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8568E.



Note:
1. Note that t_{CLOCK} refers to the clock period associated with the respective interface
   For I2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, tCLOCK references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3)

Figure 2. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/TV_{DD}/OV_{DD}$

Figure 5 shows the DDR SDRAM output timing diagram.

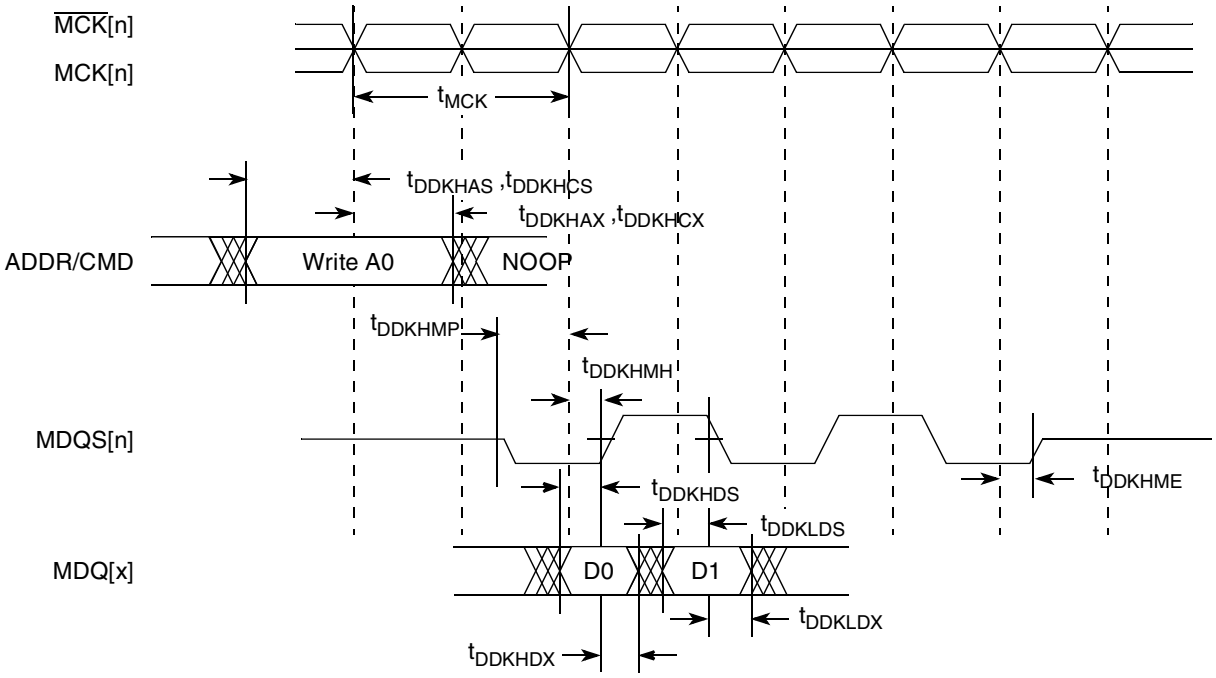


Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

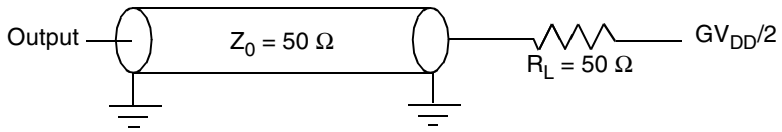


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8568E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V

Table 27. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45		55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 9 shows the GMII transmit AC timing diagram.

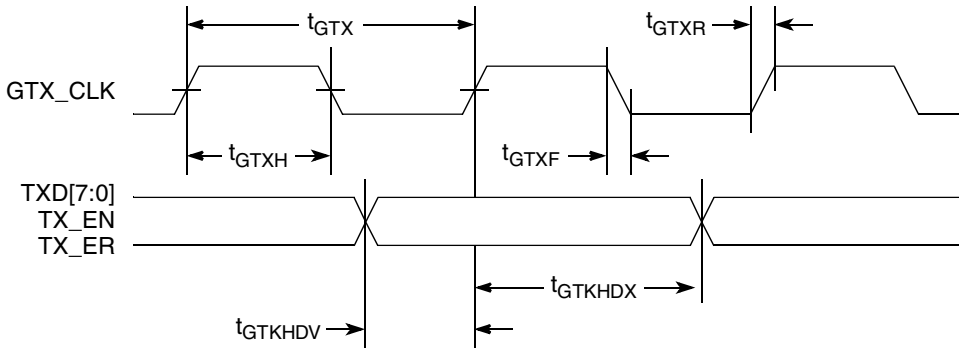


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR} [2]	—	1.0	2.0	ns

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	47	—	53	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX} [3]	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR} [2]	—	1.0	2.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF} [2]	—	1.0	2.0	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	1.0	2.0	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	1.0	2.0	ns
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

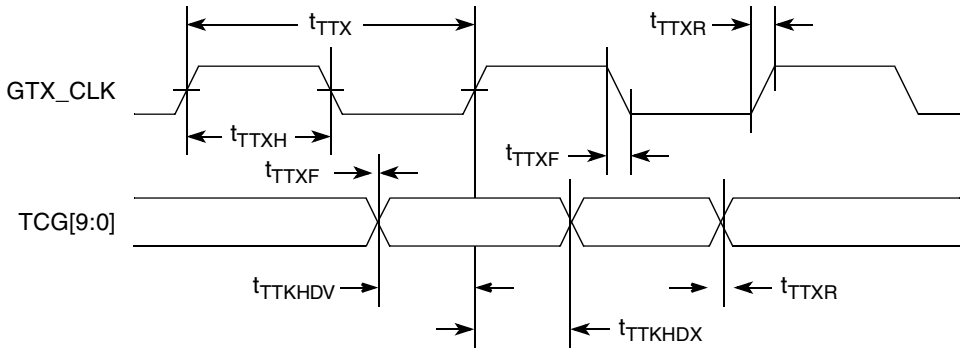


Figure 15. TBI Transmit AC Timing Diagram

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

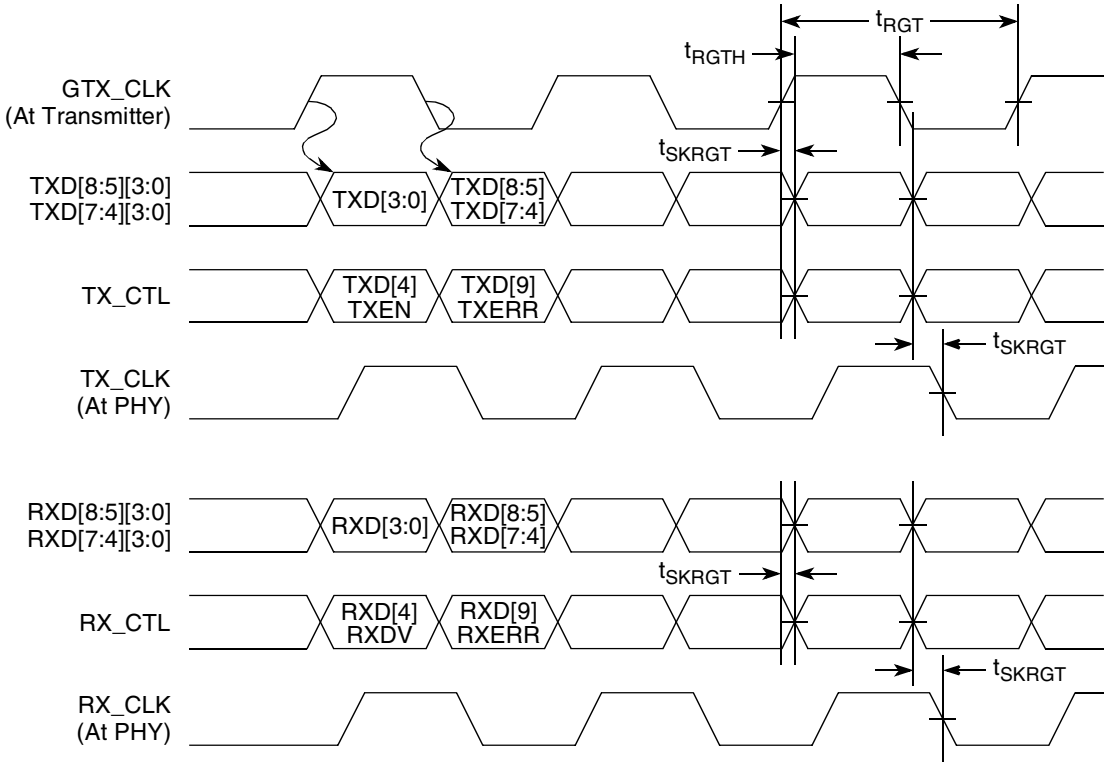


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 35.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

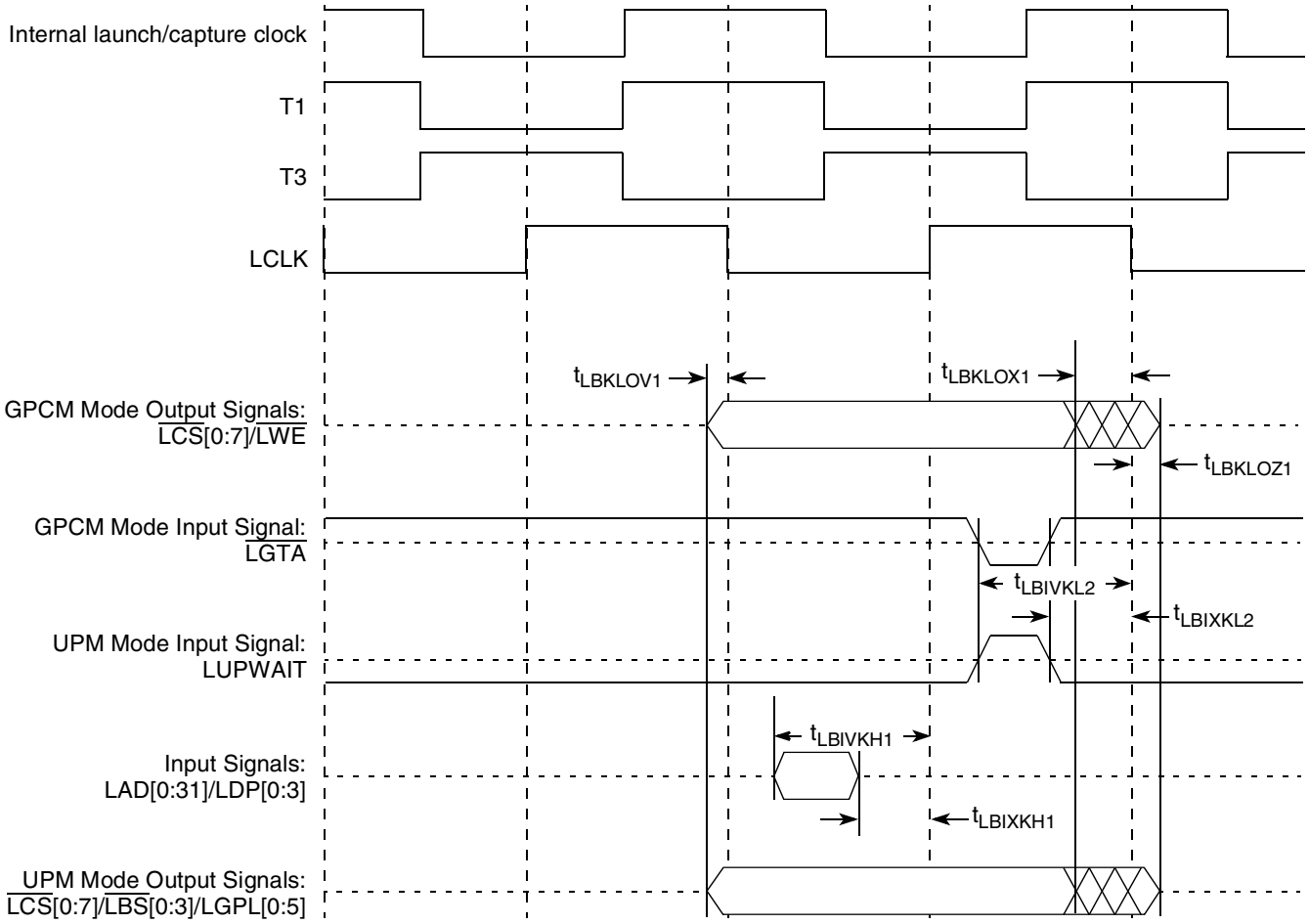


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.

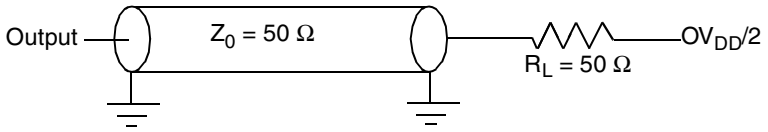


Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.

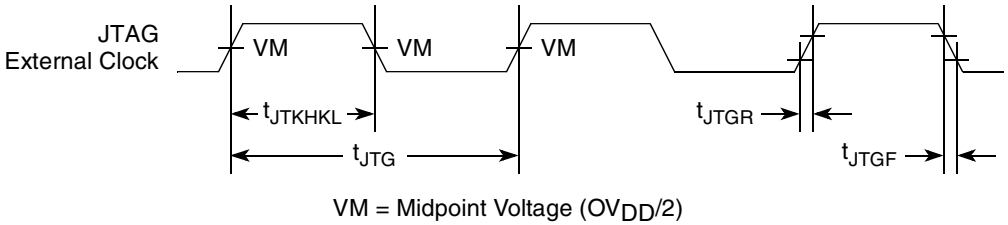


Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the $\overline{\text{TRST}}$ timing diagram.

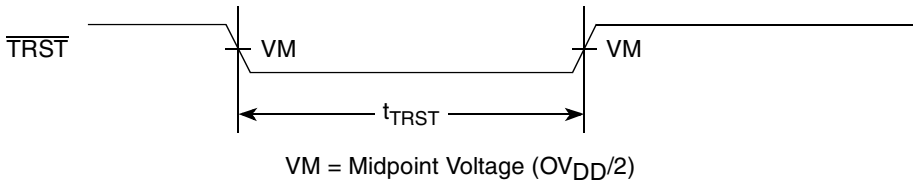


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

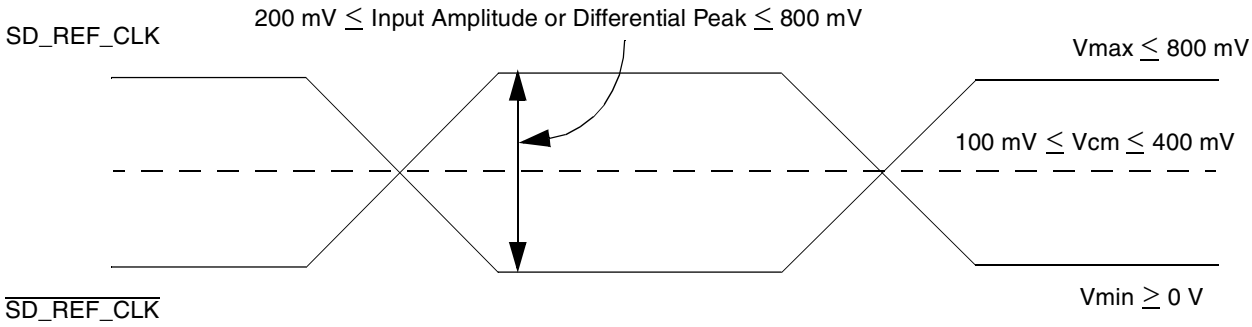


Figure 41. Differential Reference Clock Input DC Requirements (External DC-Coupled)

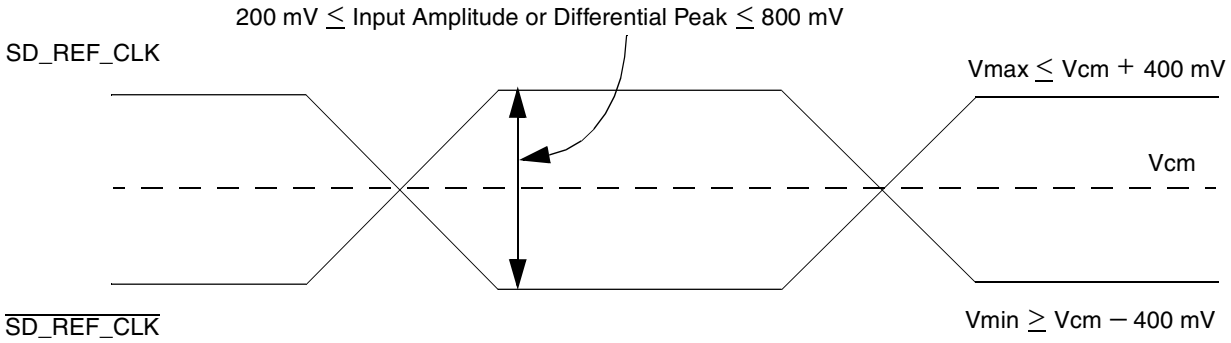


Figure 42. Differential Reference Clock Input DC Requirements (External AC-Coupled)

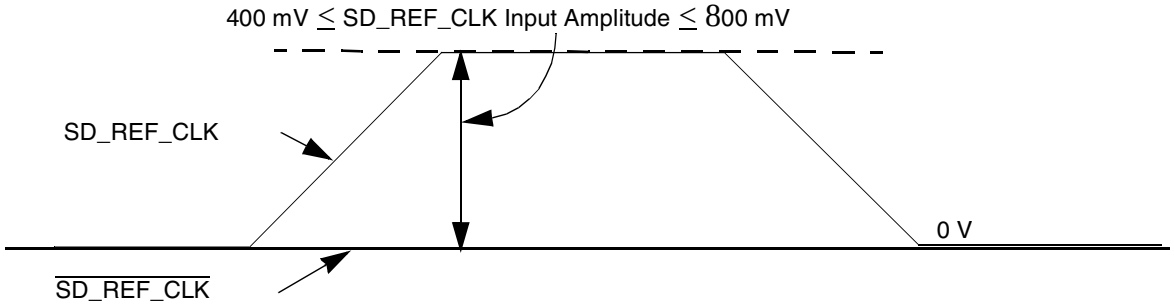


Figure 43. Single-Ended Reference Clock Input DC Requirements

13.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SCOREGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 44 to Figure 47 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8568 SerDes reference clock receiver requirement provided in this document.

Table 52. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 50). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 51). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 51) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 50) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

Table 62. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 63. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

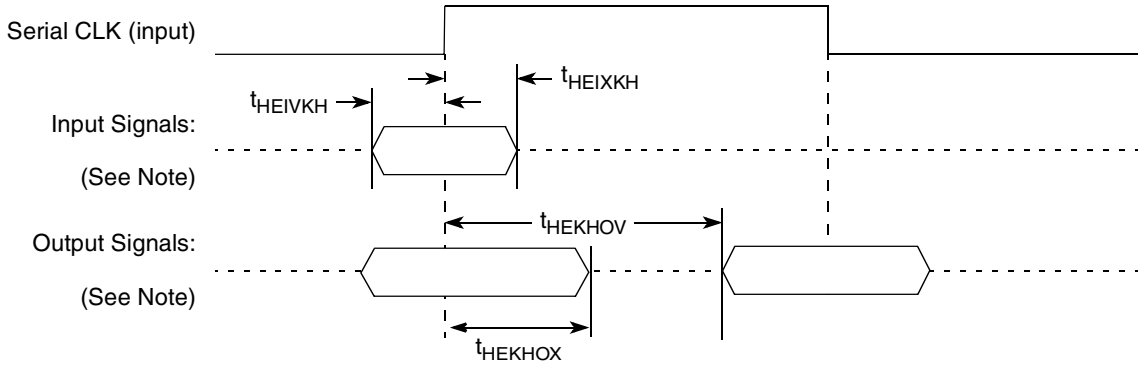
Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in and . Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in is then added to the signal and the test load is replaced by the receiver being tested.

Figure 66 through Figure 67 represent the AC timing from Table 76. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

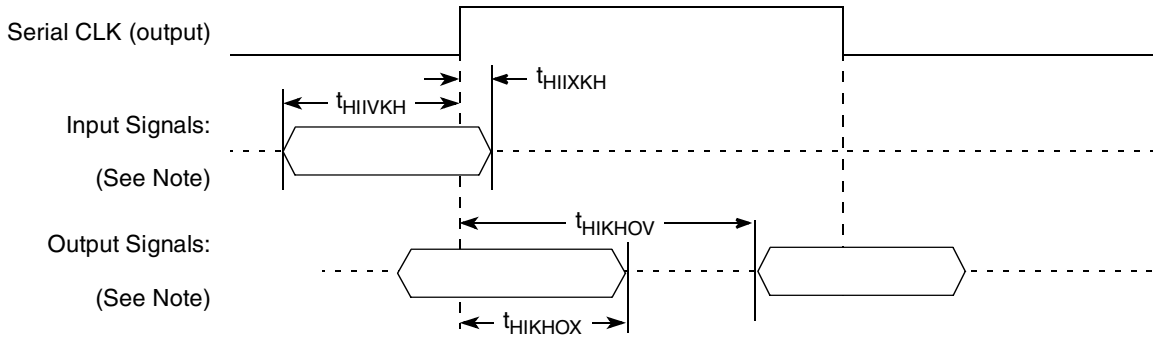
Figure 66 shows the timing with external clock.



Note: The clock edge is selectable

Figure 66. AC Timing (External Clock) Diagram

Figure 67 shows the timing with internal clock.



Note: The clock edge is selectable

Figure 67. AC Timing (Internal Clock) Diagram

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

Table 79 provides the pin-out listing for the MPC8567E 1023 FC-PBGA package.

Table 79. MPC8567E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	—
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:7]	AM16, AJ15, AJ17, AF13, AK17, AH16, AG17, AL15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—

Table 81. DDR/DDR2 Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
DDR/DDR2 Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the platform clock frequency.

Table 82. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	166	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by CCB clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for more information on this.

23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB) and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 83:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 83. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1

Millennium Electronics offer different heat sink-to-ambient thermal resistances, that will allow the MPC8568E to function in various environments.

24.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8568E thermal model without a lid is shown in Figure 70. The substrate is modeled as a block 33x33x1.18 mm with an in-plane conductivity of 24 W/mK and a through-plane conductivity of 0.92 W/mK. The solder balls and air are modeled as a single block 33x33x0.58 mm with an in-plane conductivity of 0.034 W/mK and a through plane conductivity of 12.2 W/mK. The die is modeled as 8.2x12.1 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 5.3 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. See the case outline for actual dimensions.

Conductivity	Value	Unit
Die (8.2 × 12.1 × 0.75mm)		
Silicon	Temperature dependent	W/(m × K)
Bump/Underfill (8.2 × 12.1 × 0.75 mm) Collapsed Resistance		
k_z	5.3	
Substrate (33 × 33× 1.18 mm)		
k_x	24	
k_y	24	
k_z	0.92	
Soldera and Air (33 × 33 × 0.58 mm)		
k_x	0.034	
k_y	0.034	
k_z	12.2	

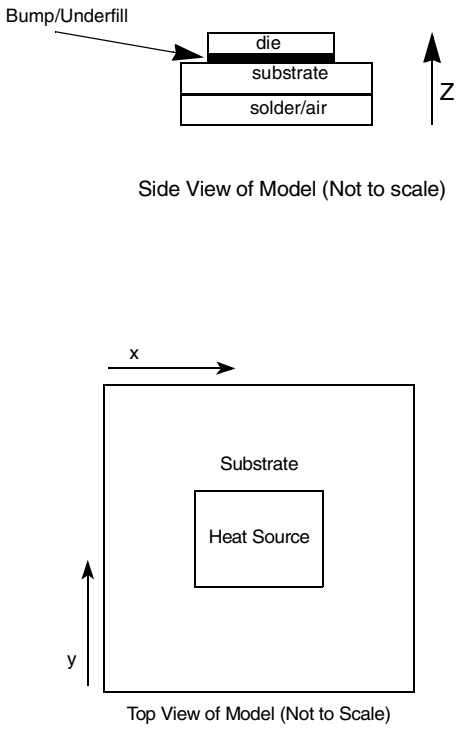


Figure 70. MPC8568E Thermal Model

24.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 87, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance

to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 75 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted.

The COP header shown in Figure 75 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 75; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 75 is common to all known emulators.