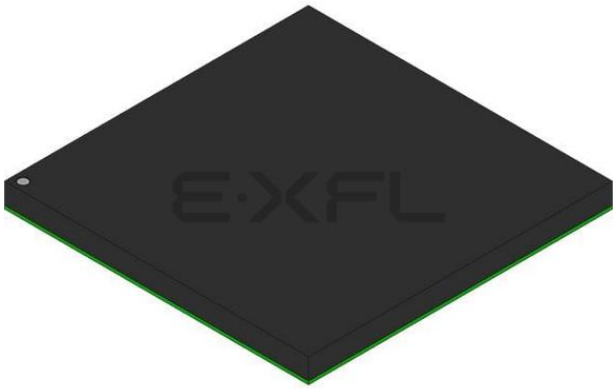

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8568evtaujj

1.2.12 Programmable Interrupt Controller (PIC)

The MPC8568E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

1.2.13 DMA Controller, I^2C, DUART, and Local Bus Controller

The MPC8568E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller also:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors.
- Scattering, gathering, and misaligned transfers are supported. In addition, stride transfers and complex transaction chaining are supported.
- Local attributes such as snoop and L2 write stashing can be specified.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8568E local bus controller (LBC) port allows connections with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Supports zero-bus-turnaround (ZBT) RAM

1.2.14 Power Management

In addition to low-voltage operation and dynamic power management, which automatically minimizes power consumption of blocks when they are idle, four power consumption modes are supported: full on, doze, nap, and sleep.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GVDD is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GVDD is not required.

3 Power Characteristics

The power dissipation of V_{DD} for various core complex bus (CCB) versus the core and QE frequency for MPC8568E is shown in Table 5. Note that this is based on the design estimate only. More accurate power number will be available after we have done the measurement on the silicon.

Table 5. MPC8568E Power Dissipation

CCB Frequency	Core Frequency	QE Frequency	Typical 65°C	Typical 105°C	Maximum	Unit
400	800	400	8.7	12.0	13.0	W
400	1000	400	8.9	12.3	13.6	W
400	1200	400	11.3	15.7	16.9	W
533	1333	533	12.4	17.2	18.7	W

Notes:
1. CCB Frequency is the SoC platform frequency which corresponds to DDR data rate.
2. Typical 65 °C based on V_{DD}=1.1V, Tj=65.
3. Typical 105 °C based on V_{DD}=1.1V, Tj=105.
4. Maximum based on V_{DD}=1.1V, Tj=105.

Table 6. Typical MPC8568E I/O Power Dissipation

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
DDR/DDR2	333 MHz	0.76	0.50									W	Data rate 64-bit with ECC 60% utilization
	400 MHz		0.56									W	
	533 MHz		0.68									W	
Local Bus	33 MHz, 32b			0.07	0.04							W	—
	66 MHz, 32b			0.13	0.07							W	—
	133 MHz, 32b			0.24	0.14							W	—
PCI	33 MHz					0.04						W	—
	66 MHz					0.07						W	—
SRIO	4x, 3.125G										0.49	W	—
PCI Express	8x, 2.5G										0.71	W	—

Figure 3 provides the input timing diagram for the DDR SDRAM interface. t_{DISKEW} can be calculated from t_{CISKEW}. See Table 19 footnote 2.

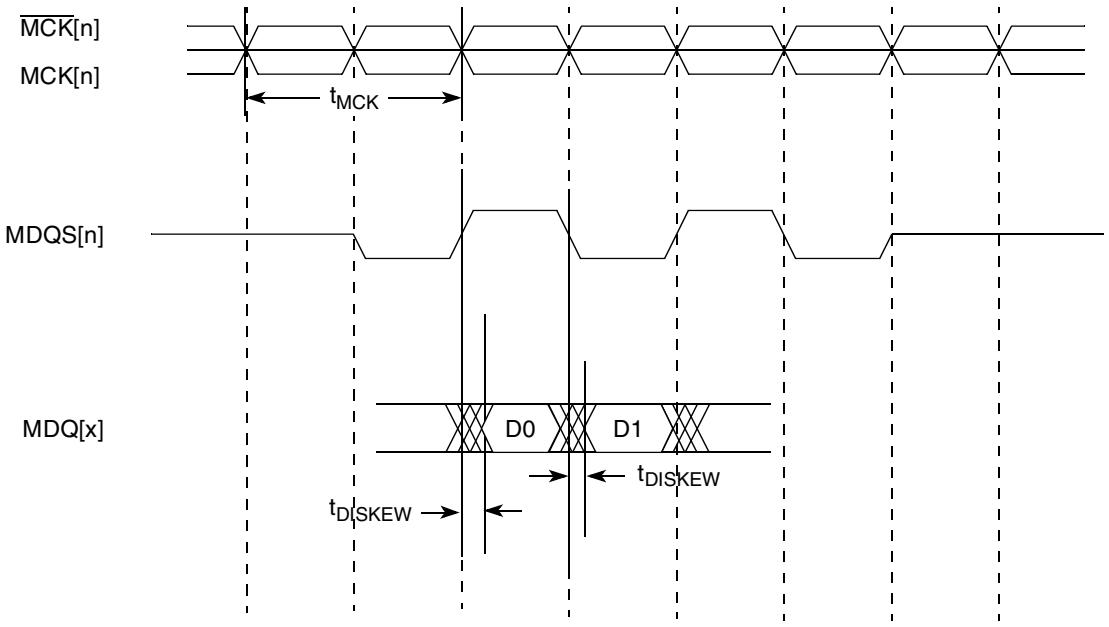

Figure 3. DDR SDRAM Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 20. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		

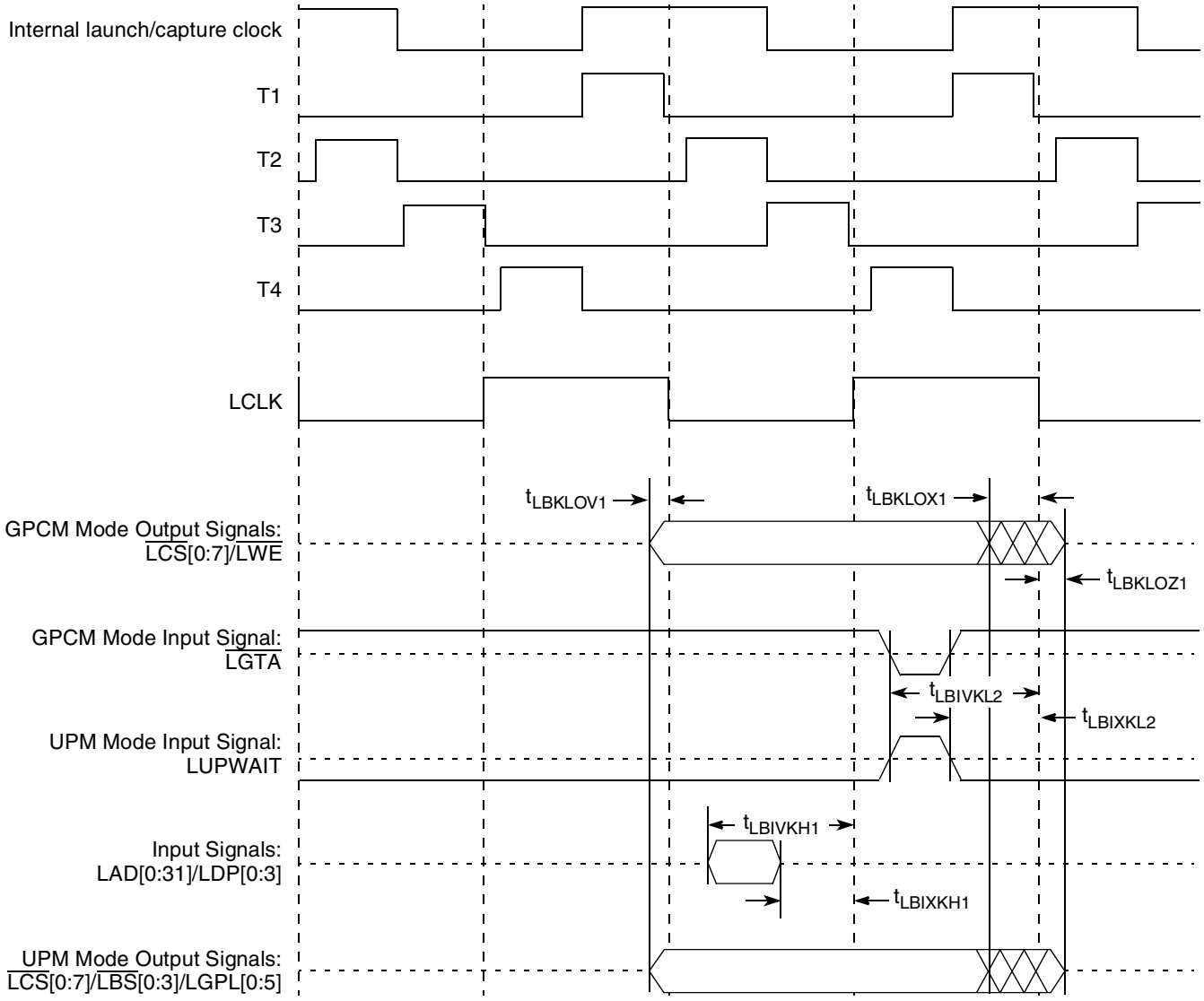

Figure 29. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface of the MPC8568E.

10.1 JTAG DC Electrical Characteristics

Table provides the DC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8568E.

Table 44. JTAG DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = -6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 < V_{IN} < OV_{DD}$	—	±10	uA

10.2 JTAG AC Electrical Characteristics

Table 45 provides the JTAG AC timing specifications as defined in Figure 31 through Figure 33.

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$.

The following sections describe the SerDes reference clock requirements and some application information.

13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 40 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for SCOREVDD and XVDD are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 40. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SCOREGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8mA) while the minimum common mode input level is 0.1V above SCOREGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 ohms to SCOREGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

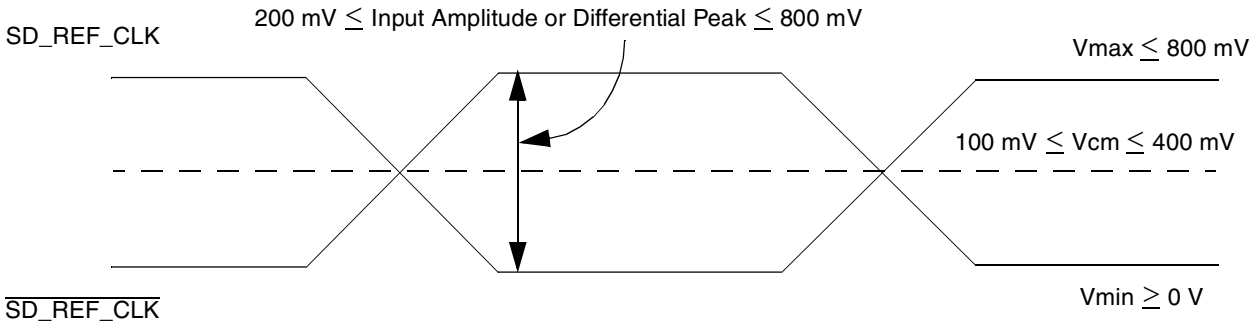

Figure 41. Differential Reference Clock Input DC Requirements (External DC-Coupled)

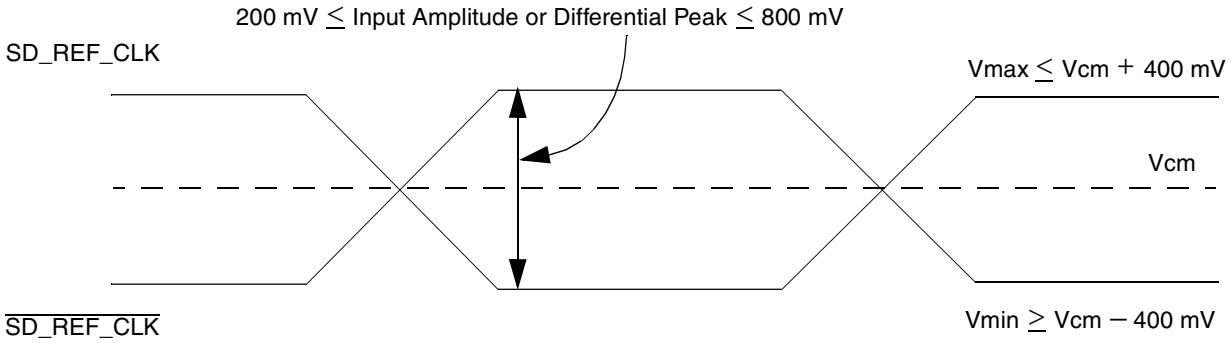

Figure 42. Differential Reference Clock Input DC Requirements (External AC-Coupled)

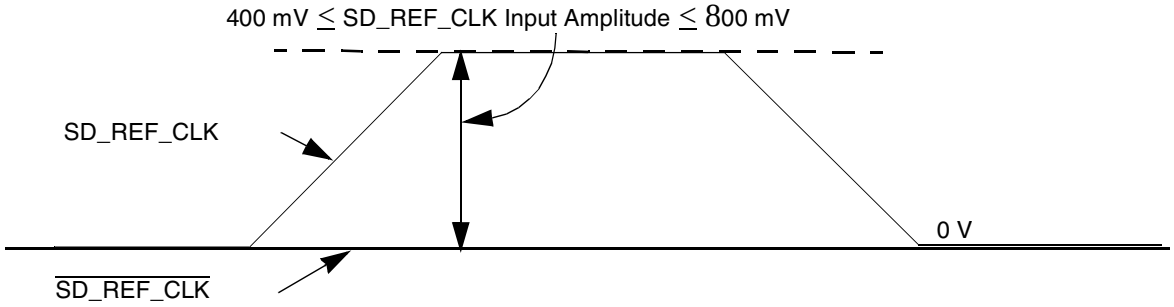

Figure 43. Single-Ended Reference Clock Input DC Requirements

Figure 47 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8568E SerDes reference clock input's DC requirement.

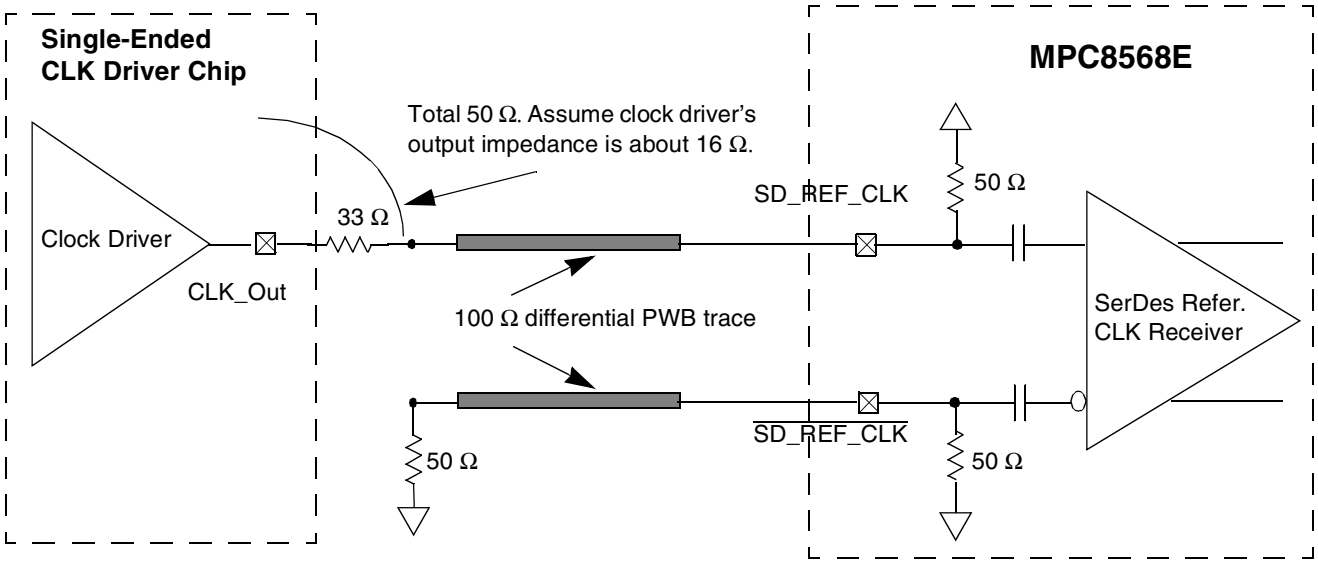

Figure 47. Single-Ended Connection (Reference Only)

13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 14.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 15.2, "AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK"

13.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

Table 51. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.
$T_{crosslink}$	Crosslink Random Timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 49)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 51). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 51 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. MPC8568E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

Table 52. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 – T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp}$ = $\lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC}$ = $DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	10	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = $2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p}$ < $V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

15.2 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Table 50 lists AC requirements.

Table 53. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 52 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

7. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B Volts
8. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD}–V_{\overline{TD}}$
9. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD}-V_{\overline{RD}}$
10. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts
11. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B Volts
12. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A – B) Volts

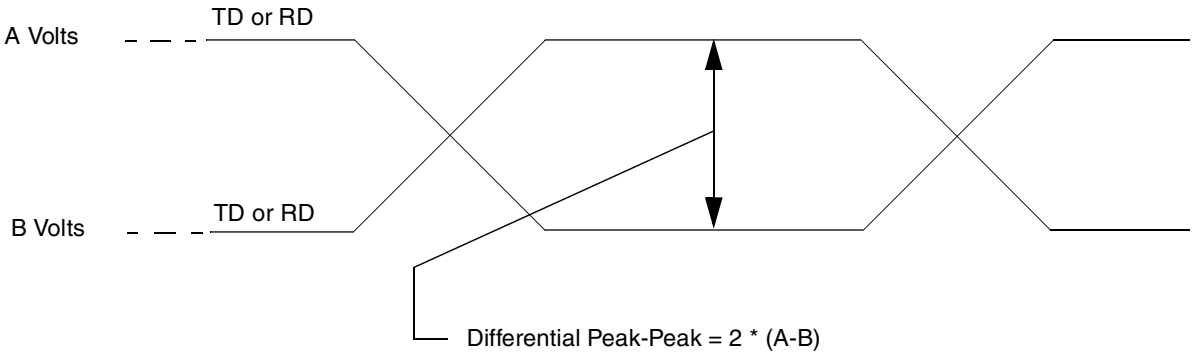

Figure 52. Differential Peak-Peak Voltage of Transmitter or Receiver

Table 54. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 55. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 56. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in and . Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in is then added to the signal and the test load is replaced by the receiver being tested.

16 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8568E.

16.1 Timers DC Electrical Characteristics

Table 65 provides the DC electrical characteristics for the MPC8568E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$ and RTC_CLK.

Table 65. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	µA

16.2 Timers AC Timing Specifications

Table 66 provides the timers input and output AC timing specifications.

Table 66. Timers Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

Figure 56 provides the AC test load for the timers.

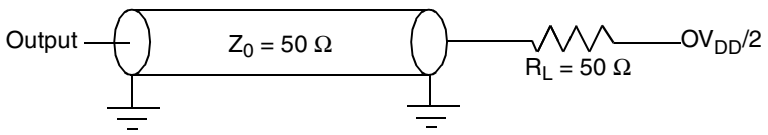

Figure 56. Timers AC Test Load

22 Package and Pinout

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8568E FC-PBGA

The package parameters are as provided in the following list. The package type is 33mm × 33mm, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Pitch	1 mm
Module height	2.23 – 2.75 mm
Solder Balls	96.5% Sn 3.5% Ag
Ball diameter (typical)	0.6 mm

22.2 Mechanical Dimensions of the MPC8568E FC-PBGA

Figure 68 shows the top view, bottom and side view of the MPC8568E 1023 FC-PBGA package.

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
$\overline{\text{MWE}}$	K3	O	GV_{DD}	—
$\overline{\text{MCAS}}$	L3	O	GV_{DD}	—
$\overline{\text{MRAS}}$	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9
LALE	G31	O	BVdd	8
LBCTL	L27	O	BVdd	8
$\overline{\text{LCS}}$[0:4]	M27, H32, J28, J30, B31	O	BV_{DD}	—
$\overline{\text{LCS5}}$	G25	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$	C29	O	BV_{DD}	1
$\overline{\text{LCS7}}$	A30	O	BV_{DD}	1
$\overline{\text{LWE}}$[0]	H30	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[1]	E28	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[2]	E32	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[3]	G27	O	BV_{DD}	5,9
LGPL0	E30	O	BV_{DD}	5,9
LGPL1	J27	O	BV_{DD}	5,9,46
LGPL2	D32	O	BV_{DD}	5,8,9

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—
PE[20]	AH6	I/O	OV_{DD}	—
PE[21:23]	AM1, AE10, AG5	I/O	OV_{DD}	5
PE[24]	AJ1	I/O	OV_{DD}	5
PE[25:31]	AH2, AM2, AE9, AH5, AL1, AD9, AL4	I/O	OV_{DD}	—
PF[7]	AG9	I/O	TV_{DD}	—
PF[8:10]	AF10, AK7, AJ6	I/O	TV_{DD}	5
PF[11:19]	AH7, AF9, AJ7, AJ5, AF7, AG8, AG7, AM5, AK5	I/O	TV_{DD}	—
PF[20]	AK1	I/O	OV_{DD}	—
PF[21:22]	AH3, AL3	I/O	OV_{DD}	5,33
PF[23:31]	AB11, AE7, AJ3, AC11, AG6, AG3, AH4, AM3, AD11	I/O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AL21	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AL23	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AK18	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AL17	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AM17	O	OV_{DD}	2,4

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_REQ[4:1]	AG29, AJ27, AH29, AB17	I	OV_{DD}	—
PCI_REQ[0]	AC17	I/O	OV_{DD}	—
PCI_CLK	AM26	I	OV_{DD}	39
PCI_DEVSEL	AK23	I/O	OV_{DD}	2
PCI_FRAME	AE21	I/O	OV_{DD}	2
PCI_IDSEL	AB19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	B22, C22, E20, A19, C23, A22, A20, C20, G22, E22, E16, F16, E23, F23, F17, H17, A18, A17, B16, C16, B19, C19, E17, A16, A13, A14, A12, C12, A15, B15, B13, C13, G12, G11, H8, F8, D13, F12, E9, F9, A7, B7, C5, E5, C8, E8, D6, A5, E6, G6, E1, F1, G7, E7, E2, D1, C4, A3, B1, C1, A4, B4, C2, D2	I/O	GV_{DD}	—
MECC[0:7]	C11, E11, D9, A8, D12, A11, A9, C9	I/O	GV_{DD}	—
MDM[0:8]	A21, E21, D18, B14, F11, A6, G5, A2, A10	O	GV_{DD}	—
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
MDQS[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
MWE	K3	O	GV_{DD}	—
MCAS	L3	O	GV_{DD}	—
MRAS	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
MCS[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
MCK[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:7]	AM16, AJ15, AJ17, AF13, AK17, AH16, AG17, AL15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AJ20	I	OV_{DD}	25
L2_TSTCLK	AJ19	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH31	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AJ31	I	OV_{DD}	25
Thermal Management				
THERM0	AB30	—	—	14
THERM1	AB31	—	—	14
Power Management				
ASLEEP	AK21	O	OV_{DD}	9,19,29
Power and Ground Signals				
GND	A23, A26, A32, B3, B6, B9, B12, B18, B21, B23, B24, B25, B26, B27, C15, C24, D5, D8, D11, D17, D20, D23, D24, D28, E13, E14, E24, E31, F3, F7, F15, F18, F22, F24, F27, G8, G16, G19, G23, H5, H12, H13, H15, H16, H18, H19, H21, H22, J2, J7, J10, J14, J15, J16, J17, J18, J19, J20, J21, J22, J29, J31, J32, K14, K15, K16, K17, K18, K19, K20, K21, K22, K24, L1, L4, L9, L12, L15, L16, L17, L18, L19, L20, L21, L22, L23, M12, M13, M18, M20, M21, M23, N4, N8, N11, N13, N15, N17, N19, N21, N23, P2, P6, P12, P14, P16, P18, P20, P22, P23, R10, R13, R15, R17, R19, R21, R23, T12, T14, T16, T18, T20, T22, T23, U4, U8, U13, U15, U17, U19, U21, U23, V2, V6, V12, V14, V16, V18, V20, V22, V23, W10, W13, W15, W17, W19, W21, W23, Y12, Y14, Y16, Y18, Y20, Y22, Y23, AA4, AA8, AA12, AA13, AA15, AA17, AA19, AA21, AA22, AA23, AB2, AB6, AB12, AB23, AB29, AB32, AC10, AC23, AC24, AC25, AC28, AC29, AC30, AC31, AC32, AD16, AD17, AD19, AD21, AD25, AD26, AD27, AD31, AE8, AE12, AF2, AF4, AF6, AF16, AF21, AF25, AG10, AG14, AG18, AG24, AG28, AH23, AJ4, AJ8, AJ12, AJ21, AJ30, AJ32, AK2, AK10, AK16, AK32, AL6, AL14, AL18, AL19, AL20, AL22, AL24, AL25, AL26, AL31, AL32, AM19, AM21, AM23, AM25, AM30, AM31, AM32	—	—	—
SCOREGND	K28, K29, K30, L28, L31, M28, M30, N32, P28, P30, R28, T29, U32, V30, W28, W31, Y28, Y29, AA29, AA30, AA32, AB28	Ground for SerDes receiver	—	—
XGND	N24, N26, P25, R27, T24, U26, V25, W27, Y24, AA26, AB25, AC27	Ground for SerDes transmitter	—	—