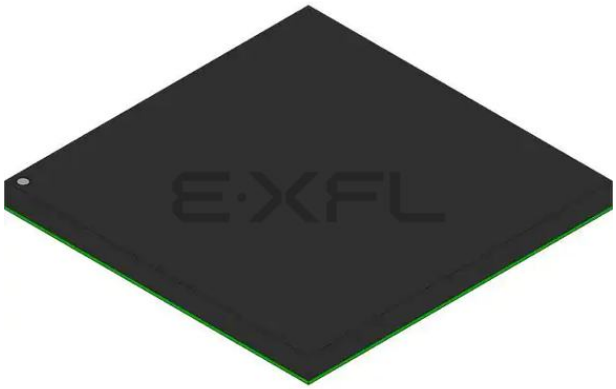

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Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
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1.1 MPCP8568E Key Features

- High-performance, Power Architecture® e500v2 core with 36-bit physical addressing
- 512 Kbytes of level-2 cache
- QUICC Engine (QE)
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- A 1x/4x Serial RapidIO® and/or x1/x2/x4 PCI Express interface. If x8 PCI Express is needed, then RapidIO is not available due to the limitation of the pin multiplexing.
- Programmable interrupt controller (PIC)
- Four-channel DMA controller, two I^2C controllers, DUART, and local bus controller (LBC)

NOTE

The MPC8568E and MPC8567E are also available without a security engine in a configuration known as the MPC8568 and MPC8567. All specifications other than those relating to security apply to the MPC8568 and MPC8567 exactly as described in this document.

1.2 MPC8568E Architecture Overview

1.2.1 e500 Core and Memory Unit

The MPC8568E contains a high-performance, 32-bit, Book E–enhanced e500v2 Power Architecture core. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- Double-precision floating-point APU—Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs
- Embedded vector and scalar single-precision floating-point APUs—Provide an instruction set for single-precision (32-bit) floating-point instructions

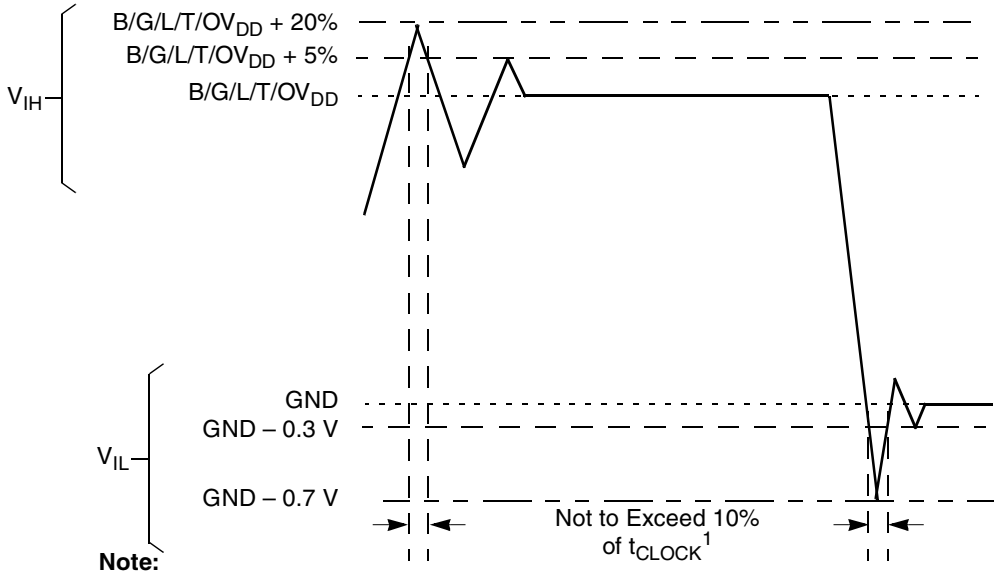
The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	—
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
Junction temperature range		Tj	0 to105	°C	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8568E.



Note:
1. Note that t_{CLOCK} refers to the clock period associated with the respective interface
   For I2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, tCLOCK references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3)

Figure 2. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/TV_{DD}/OV_{DD}$

Table 6. Typical MPC8568E I/O Power Dissipation (continued)

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
eTSEC Ethernet	MII						0.01					W	Multiply with number of the interfaces
	GMII/TBI						0.07					W	
	RGMII/RTBI							0.04				W	
eTSEC FIFO I/O	16b, 200 MHz						0.20					W	Multiply with number of the interfaces
	16b, 155 MHz						0.16					W	
	8b, 200 MHz						0.11					W	
	8b, 155 MHz						0.08					W	
QE UCC	MII/RMII								0.01			W	Multiply with number of the interfaces If UCC is programmed for other protocols, scale Ethernet power dissipation to the number of signals and the clock rate
	GMII/TBI								0.07			W	
	RGMII/RTBI									0.04		W	

Note: This is the power for each individual interface. The power must be calculated for each interface being utilized.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8568E.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3

4.4 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8568E.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	 — —	 — —	 0.75 1.0	ns	—
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TVDD = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

4.5 FIFO Clock Speed Restrictions

Note the following FIFO maximum speed restrictions based on the platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 167 MHz

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 8, “Ethernet Interface and MII Management.”

8.1.1 Ethernet Interface DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	47	—	53	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX} [3]	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR} [2]	—	1.0	2.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF} [2]	—	1.0	2.0	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	1.0	2.0	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	1.0	2.0	ns
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

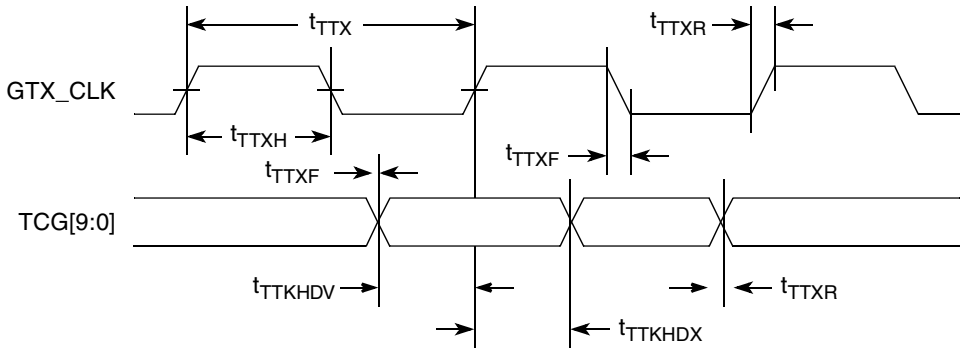


Figure 15. TBI Transmit AC Timing Diagram

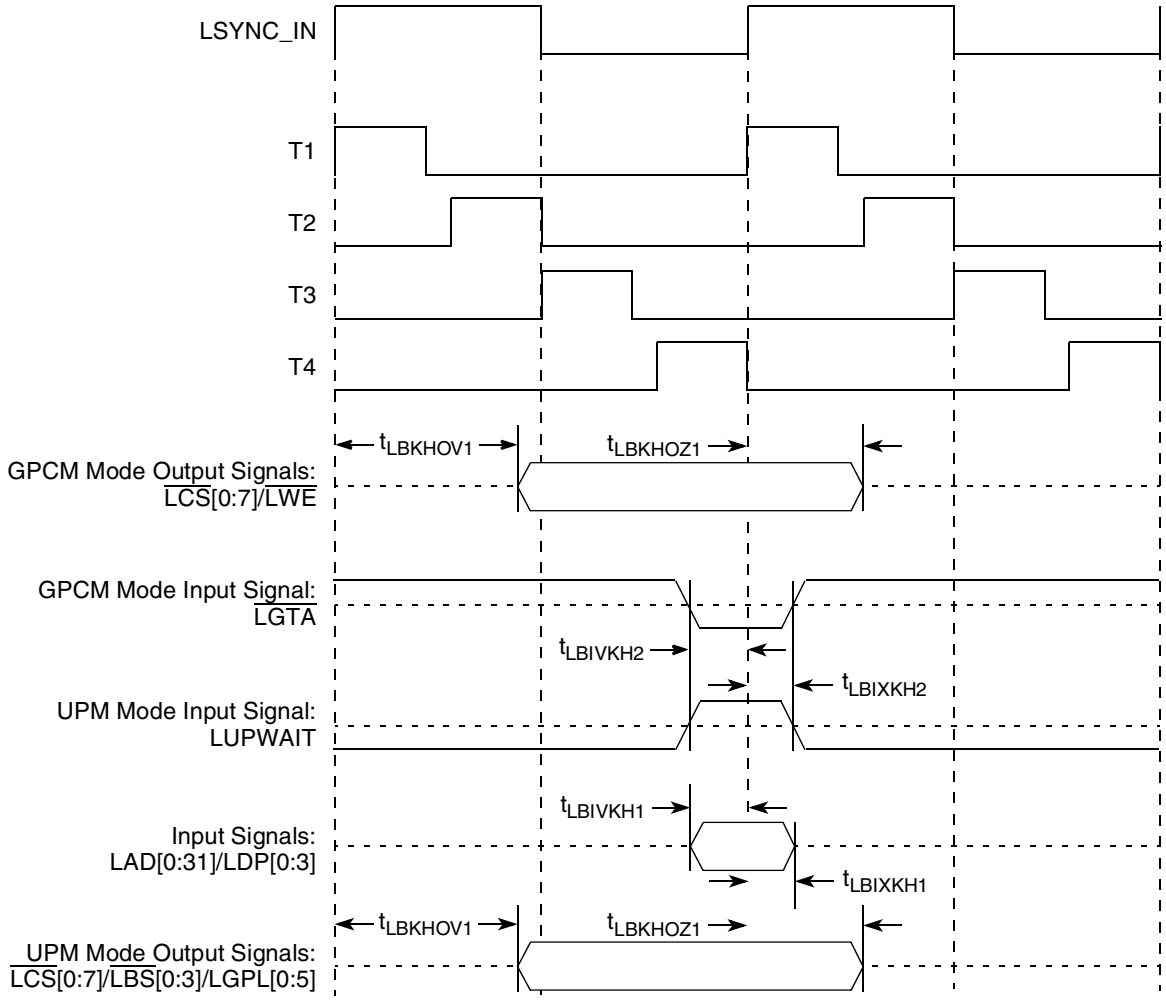


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Table 47. I²C AC Electrical Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol [1]	Min	Max	Unit
Capacitive load for each bus line	C_b	—	400	pF

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8568 provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8568 acts as the I²C bus master while transmitting, the MPC8568 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8568 would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8568 as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*

Figure 30 provides the AC test load for the I²C.

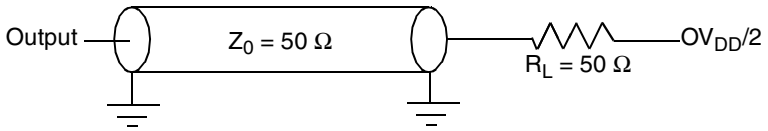


Figure 34. I²C AC Test Load

Figure 35 shows the AC timing diagram for the I²C bus.

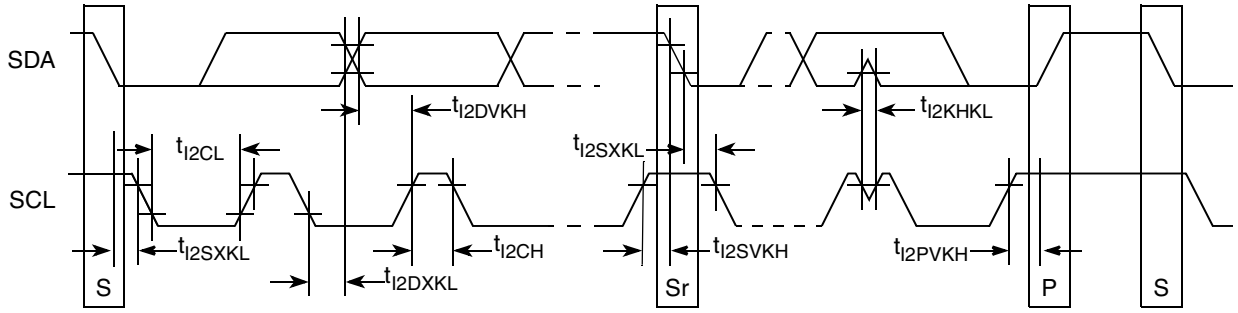


Figure 35. I²C Bus AC Timing Diagram

Table 59. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 53 with the parameters specified in Table 60 when measured at the output pins of the device and the device is driving a 100 Ohm +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

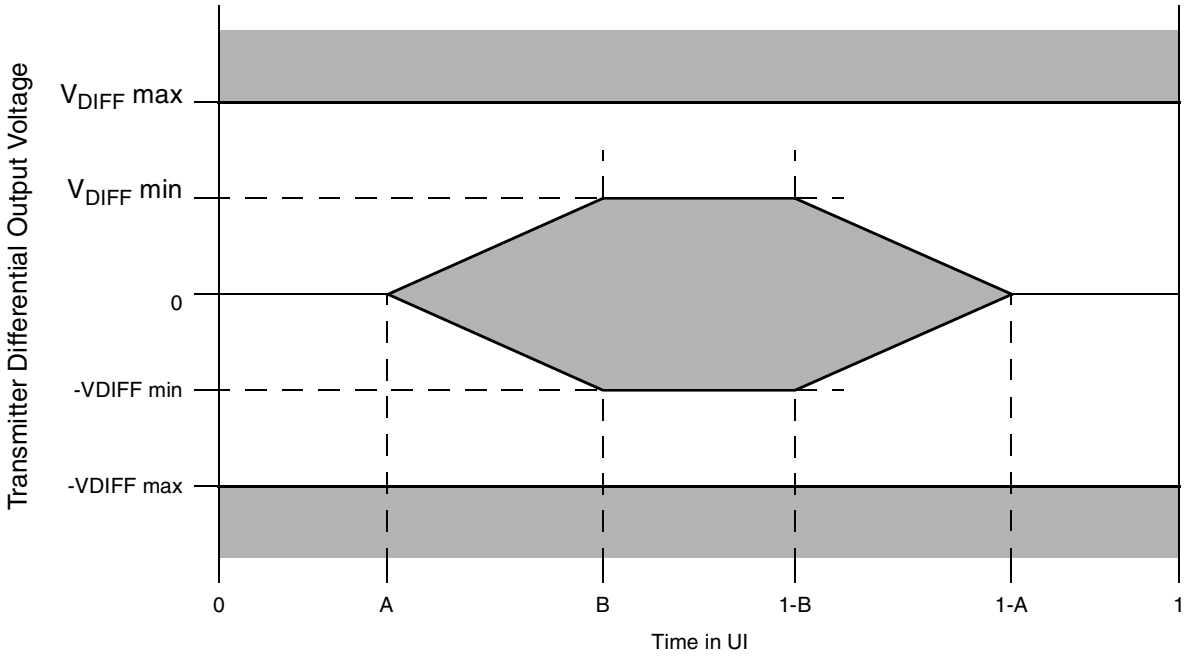


Figure 53. Transmitter Output Compliance Mask

Table 60. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 61. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8568E.

18.1 SPI DC Electrical Characteristics

Table 69 provides the DC electrical characteristics for the MPC8568E SPI.

Table 69. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	μA

18.2 SPI AC Timing Specifications

Table 70 and provide the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 57 provides the AC test load for the SPI.

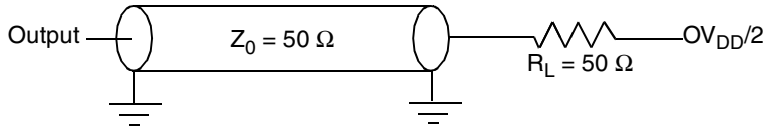


Figure 57. SPI AC Test Load

Figure 64 shows the Utopia timing with internal clock.

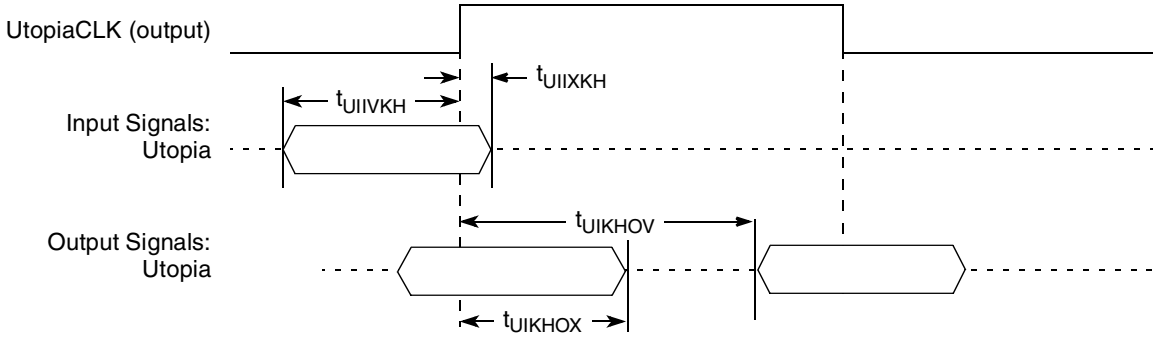


Figure 64. Utopia AC Timing (Internal Clock) Diagram

21 HDLC, BISYNC, Transparent and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent and synchronous UART of the MPC8568E.

21.1 HDLC, BISYNC, Transparent and Synchronous UART DC Electrical Characteristics

Table 75 provides the DC electrical characteristics for the MPC8568E HDLC, BISYNC, Transparent and Synchronous UART protocols.

Table 75. HDLC, BiSync, Transparent and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

21.2 HDLC, BISYNC, Transparent and Synchronous UART AC Timing Specifications

Table 76 provides the input and output AC timing specifications for HDLC, BiSync, Transparent and Synchronous UART protocols.

Table 76. HDLC, BiSync, Transparent AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	6.5	ns
Outputs—External clock delay	t_{HEKHOV}	1	8	ns

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL3	J25	O	BV_{DD}	5,9
LGPL4	C25	I/O	BV_{DD}	49
LGPL5	F32	O	BV_{DD}	5,9
LCKE	C31	O	BV_{DD}	—
LCLK[0:2]	C27, C26, D25	O	BV_{DD}	—
LSYNC_IN	A28	I	BV_{DD}	—
LSYNC_OUT	A27	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0]	AM27	O	OV_{DD}	5,9,46
$\overline{\text{DMA\_DREQ}}$[0]	AK28	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0]	AK26	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AG32	I	OV_{DD}	—
$\overline{\text{MCP}}$	AF32	I	OV_{DD}	—
IRQ[0:7]	AD30, AG31, AL30, AF31, AD29, AK30, AG30, AF30	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	AD28	O	OV_{DD}	2,4
Interface				
EC_MDC	AE17	O	OV_{DD}	5,9
EC_MDIO	AF17	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	AM14	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	AE14, AM11, AK11, AF11, AJ14, AJ13, AD12, AE13	I	LV_{DD}	—
TSEC1_TXD[7]	AH12	O	LV_{DD}	5, 9
TSEC1_TXD[6:1]	AL13, AL11, AK13, AH13, AG11, AD13	O	LV_{DD}	—
TSEC1_TXD[0]	AM13	O	LV_{DD}	5, 9
TSEC1_COL	AG13	I	LV_{DD}	—
TSEC1_CRS	AB13	I/O	LV_{DD}	20
TSEC1_GTX_CLK	AG12	O	LV_{DD}	—
TSEC1_RX_CLK	AE11	I	LV_{DD}	—
TSEC1_RX_DV	AH11	I	LV_{DD}	—
TSEC1_RX_ER	AM12	I	LV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AV_{DD_CORE}	AM24	Power for e500 PLL (1.1V)	—	26
AV_{DD_PLAT}	AM20	Power for CCB PLL (1.1V)	—	26
AV_{DD_SRDS}	R29	Power for SRDSPLL (1.1V)	—	26
AGND_SRDS	R31	Ground for SRDSPLL	—	
SENSEVDD	M17	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A24	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	K32	I	200Ω to GND	—
SD_IMP_CAL_TX	AA28	I	100Ω to GND	—
SD_PLL_TPA	R30	O	—	24
Reserved Pins				
Reserved	AE17, AH12, AL13, AL11, AK13, AH13, AG11, AD13, AM13, AG12, AC13, AL12, AJ16, AM15, AK15	N/A	N/A	42
Reserved	AF17, AM14, AE14, AM11, AK11, AF11, AJ14, AJ13, AD12, AE13, AG13, AB13, AE11, AH11, AM12, AJ11, AB15, AB16, AE16, AG15, AF15, AH14	N/A	N/A	45

23.5.2 Minimum Platform Frequency Requirements for PCI Express, SRIO, PCI interfaces Operation

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Note that the “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

For proper PCI operation in synchronous mode, the minimum CCB:SYSCLK ratio is 6:1.

24 Thermal

This section describes the thermal specifications of the MPC8568E.

24.1 Thermal Characteristics

Table 87 provides the package thermal characteristics.

Table 87. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on single layer board (1s)	$R_{\theta JA}$	16	•C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JA}$	13	•C/W	1, 2
Junction-to-board	$R_{\theta JB}$	9	•C/W	3
Junction-to-case	$R_{\theta JC}$	<0.1	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

24.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the

system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 69. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

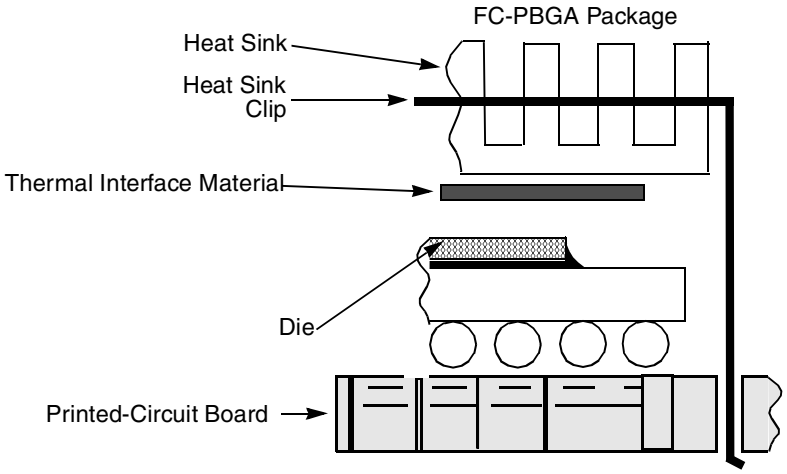


Figure 69. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, and

Thermagon Inc.
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

888-246-9050

25 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8568E.

25.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 23.2, “CCB/SYSCLK PLL Ratio.”
2. The e500 core PLL generates the core clock using the platform clock as the input. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 23.3, “e500 Core PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.
6. QE PLL generates the QE clock from the externally supplied SYSCLK.

25.2 Power Supply Design and Sequencing

25.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_PCI}, AV_{DD_LBIU}, and AV_{DD_SRDS}, AV_{DD_CE} respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 73, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 1023FC-PBGA the footprint, without the inductance of vias.

Figure 73 shows the PLL power supply filter circuits for all PLLs except SerDes PLL.

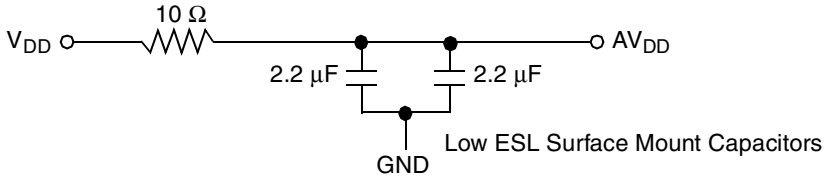
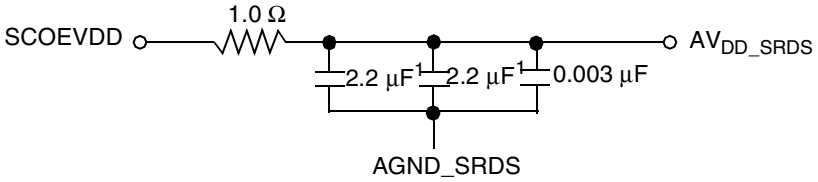


Figure 73. MPC8568E PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} and AGND_SRDS ball to ensure it filters out as much noise as possible. The 0.003-µF capacitor is closest to the ball, followed by the 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 74. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD_SRDS} should be a filtered version of SCOREVDD.
- The transmitter output signals on the SerDes interface are fed from the XV_{DD} power plan.
- Power: XVDD consumes less than 300mW. SCOREVDD + AV_{DD_SRDS} consumes less than 750mW.

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. MPC8568E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SCOREVDD and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

25.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}$ TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD} and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}$ $L_{VDD,}$ TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD} and GND pins of the device.

25.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8568E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 75. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

- $\overline{\text{SD\_TX}}$[7:0]

25.9.2 Unused input

25.9.2.1 SerDes block power not supplied

If the high speed interface is not used at all, then SCOREVDD/XVDD/AV_{DD_SRDS} can be tied to GND, all receiver inputs should be tied to the GND as well. This includes:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$
- $\overline{\text{SD\_RX\_CLK}}$
- $\overline{\text{SD\_RX\_FRM\_CTL}}$

25.9.2.2 SerDes Interface Partly used

If the high-speed SerDes interface is partly unused, any of the unused receiver pins should be terminated as follows:

- SD_RX[7:0] = tied to SCOREGND
- $\overline{\text{SD\_RX}}$[7:0] = tied to SCOREGND
- SD_REF_CLK = tied to SCOREGND
- $\overline{\text{SD\_REF\_CLK}}$ = tied to SCOREGND

NOTE

Power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

During HRESET/POR, the high-speed interface must be in Serial RapidIO mode and/or PCI Express mode according to the state of the PE[8:10]. Software must disable this mode through DEVDISR[SRIO] or DEVDISR[PCIE] accordingly during software initialization.

26 Ordering Information

Contact your local Freescale sales office or regional marketing team for order information.