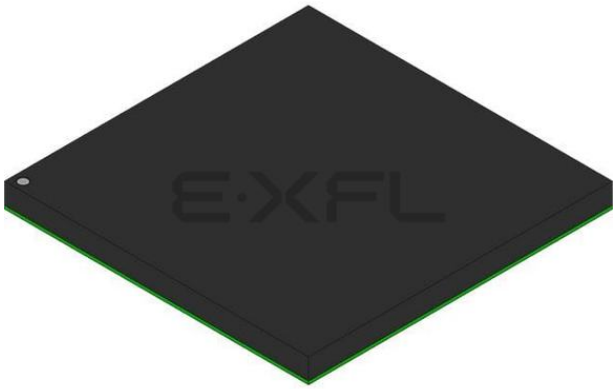

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8568vtaujj

1 MPC8568E Overview

This section provides a high-level overview of MPC8568E features. Figure 1 shows the major functional units within the MPC8568E.

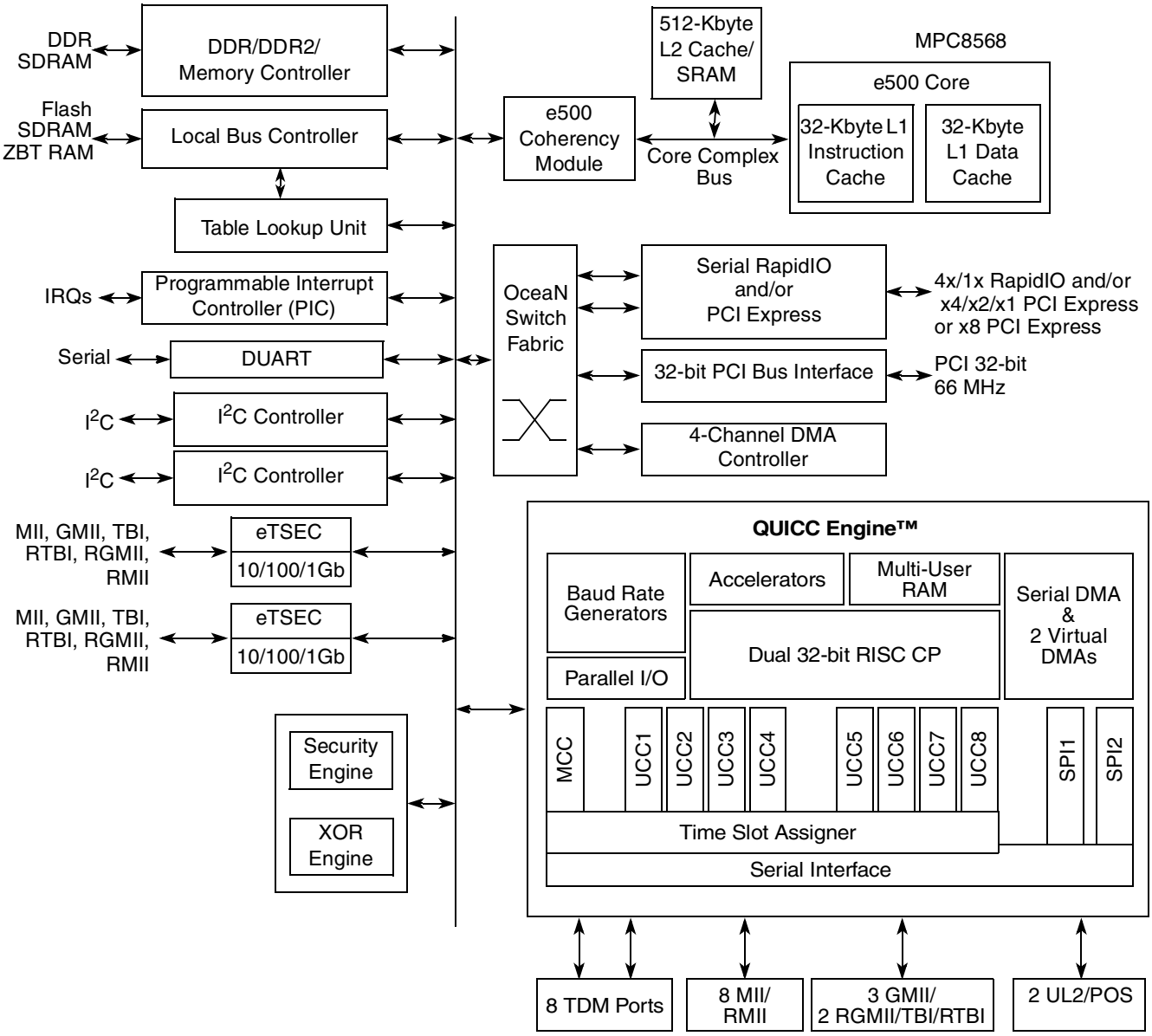

Figure 1. MPC8568E Block Diagram

1.1 MPCP8568E Key Features

- High-performance, Power Architecture® e500v2 core with 36-bit physical addressing
- 512 Kbytes of level-2 cache
- QUICC Engine (QE)
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- A 1x/4x Serial RapidIO® and/or x1/x2/x4 PCI Express interface. If x8 PCI Express is needed, then RapidIO is not available due to the limitation of the pin multiplexing.
- Programmable interrupt controller (PIC)
- Four-channel DMA controller, two I^2C controllers, DUART, and local bus controller (LBC)

NOTE

The MPC8568E and MPC8567E are also available without a security engine in a configuration known as the MPC8568 and MPC8567. All specifications other than those relating to security apply to the MPC8568 and MPC8567 exactly as described in this document.

1.2 MPC8568E Architecture Overview

1.2.1 e500 Core and Memory Unit

The MPC8568E contains a high-performance, 32-bit, Book E–enhanced e500v2 Power Architecture core. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- Double-precision floating-point APU—Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs
- Embedded vector and scalar single-precision floating-point APUs—Provide an instruction set for single-precision (32-bit) floating-point instructions

The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.

— Three 1-Gbps Ethernet interfaces using three GMII, two RGMII/TBI/RTBI
— Up to eight 10/100-Mbps Ethernet interfaces using MII or RMII
— Up to eight T1/E1/J1/E3 or DS-3 serial interfaces

1.2.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8568E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
- Compatible with code written for the Freescale MPC8541E and MPC8555E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  — PKEU—public key execution unit
  — DEU—Data Encryption Standard execution unit
  — AESU—Advanced Encryption Standard unit
  — AFEU—ARC four execution unit
  — MDEU—message digest execution unit
  — KEU—Kasumi execution unit
  — RNG—Random number generator

1.2.5 Enhanced Three-Speed Ethernet Controllers

The MPC8568E has two on-chip enhanced three-speed Ethernet controllers (eTSECs). The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

The MPC8568E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab-compatible.

The buffer descriptors are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

Some of the key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ)$=2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: t_{DISKEW} =+/-(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

Table 24. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

Table 27. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45		55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 9 shows the GMII transmit AC timing diagram.

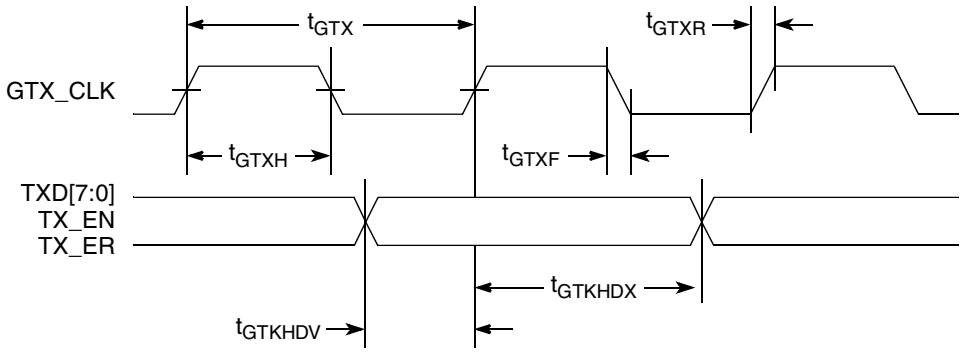

Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR} [2]	—	1.0	2.0	ns

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n* TSECn_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	1.0	2.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	1.0	2.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

A timing diagram for TBI receive appears in Figure 17.

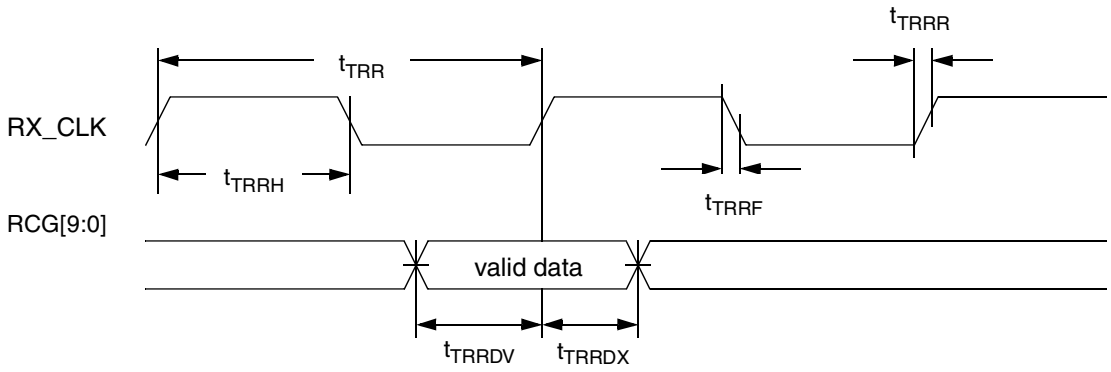

Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}[5]	7.2	8.0	8.8	ns

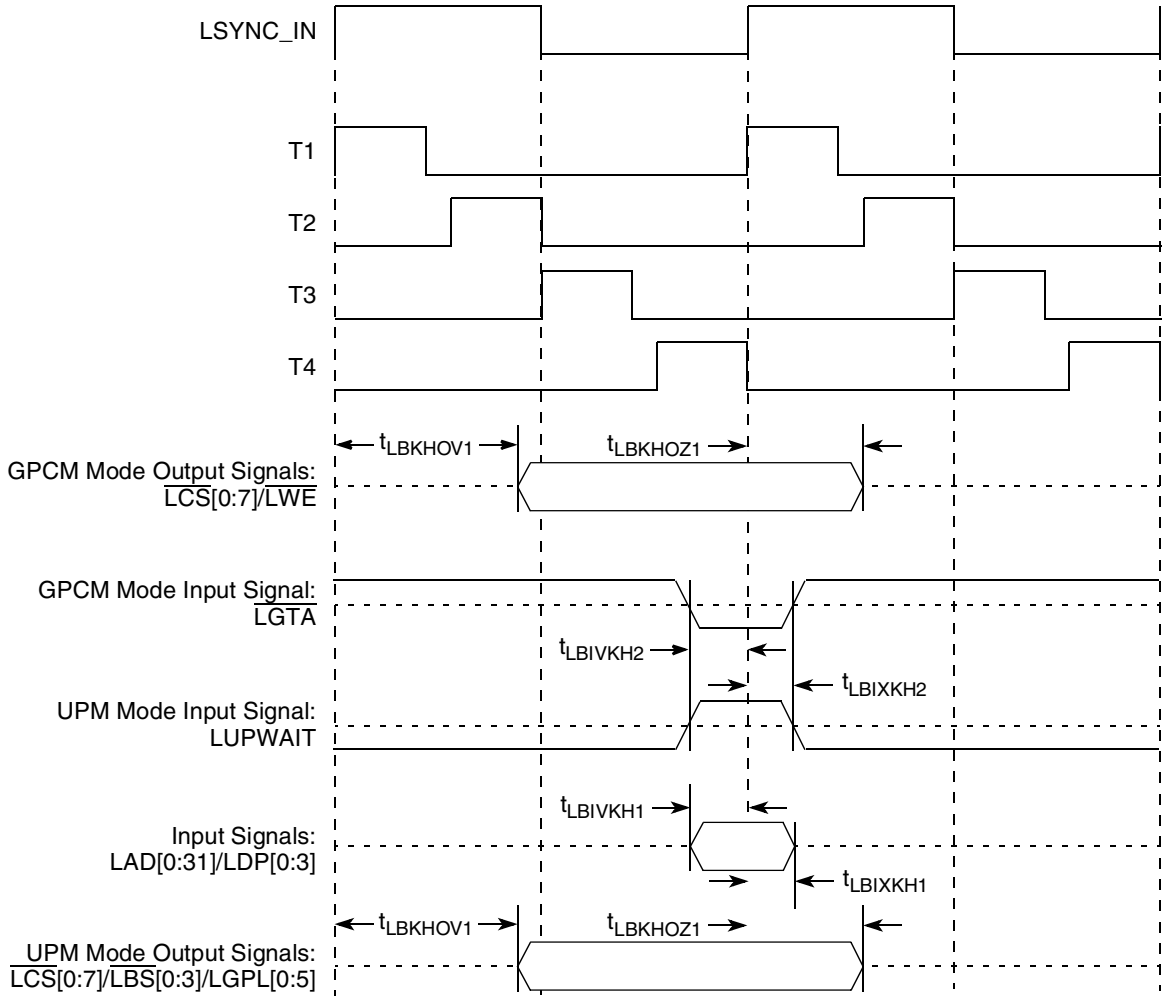

Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.

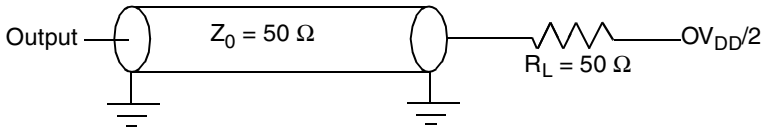

Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.

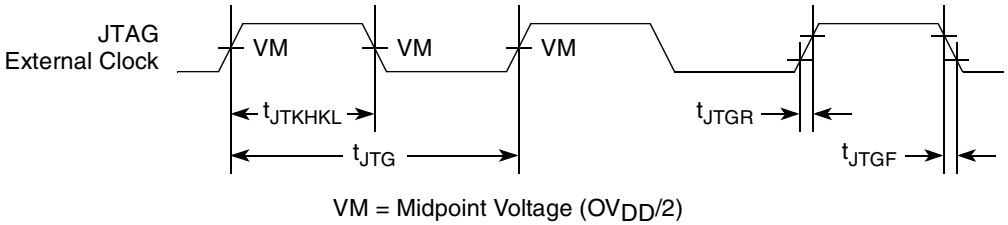

Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the $\overline{\text{TRST}}$ timing diagram.

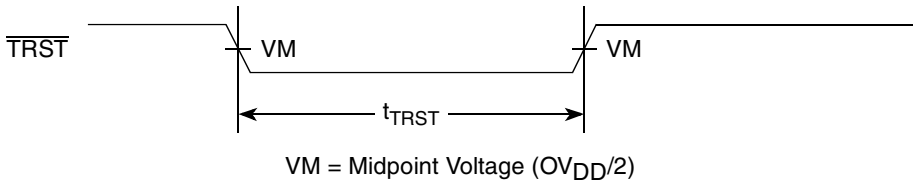

Figure 32. $\overline{\text{TRST}}$ Timing Diagram

Table 46. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8568E PowerQUICC III Integrated Communications Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 47 provides the AC timing parameters for the I²C interfaces.

Table 47. I²C AC Electrical Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	µs
High period of the SCL clock	t_{I2CH}	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs
Data setup time	t_{I2DVKH}	100	—	ns
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— —	µs
Data output delay time	t_{I2OVKL}	—	0.9 [3]	µs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

13.3 SerDes Transmitter and Receiver Reference Circuits

Figure 48 shows the reference circuits for SerDes data lane's transmitter and receiver.

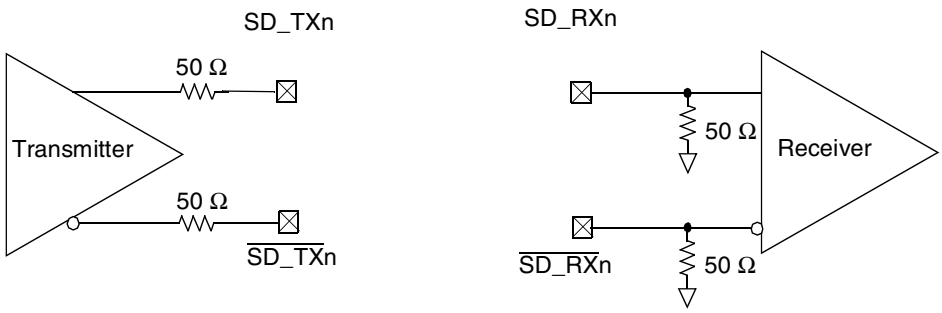

Figure 48. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 14, "PCI Express"
- Section 15, "Serial RapidIO"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

14 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8568E.

14.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 13, "High-Speed Serial Interfaces (HSSI)."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 50 lists AC requirements.

Table 50. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 60. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 61. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 71. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

19.2 TDM/SI AC Timing Specifications

Table 72 provides the TDM/SI input and output AC timing specifications.

Table 72. TDM/SI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 60 provides the AC test load for the TDM/SI.

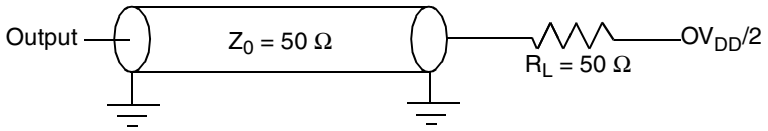

Figure 60. TDM/SI AC Test Load

Figure 61 represents the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

Table 79 provides the pin-out listing for the MPC8567E 1023 FC-PBGA package.

Table 79. MPC8567E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	—
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALE	G31	O	BVdd	8
LBCTL	L27	O	BVdd	8
$\overline{\text{LCS}}$[0:4]	M27, H32, J28, J30, B31	O	BV_{DD}	—
$\overline{\text{LCS5}}$	G25	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$	C29	O	BV_{DD}	1
$\overline{\text{LCS7}}$	A30	O	BV_{DD}	1
$\overline{\text{LWE}}$[0]	H30	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[1]	E28	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[2]	E32	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[3]	G27	O	BV_{DD}	5,9
LGPL0	E30	O	BV_{DD}	5,9
LGPL1	J27	O	BV_{DD}	5,9,46
LGPL2	D32	O	BV_{DD}	5,8,9
LGPL3	J25	O	BV_{DD}	5,9
LGPL4	C25	I/O	BV_{DD}	49
LGPL5	F32	O	BV_{DD}	5,9
LCKE	C31	O	BV_{DD}	—
LCLK[0:2]	C27, C26, D25	O	BV_{DD}	—
LSYNC_IN	A28	I	BV_{DD}	—
LSYNC_OUT	A27	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0]	AM27	O	OV_{DD}	5,9,47
$\overline{\text{DMA\_DREQ}}$[0]	AK28	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0]	AK26	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AG32	I	OV_{DD}	—
$\overline{\text{MCP}}$	AF32	I	OV_{DD}	—
IRQ[0:7]	AD30, AG31, AL30, AF31, AD29, AK30, AG30, AF30	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	AD28	O	OV_{DD}	2,4
GPIO				
GPIN[0:7]	AC14, AD15, AB14, AH15, AD14, AH17, AE15, AC15	I	LV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

23 Clocking

This section describes the PLL configuration of the MPC8568E. Note that the platform clock is identical to the core complex bus (CCB) clock.

23.1 Clock Ranges

Table 80 provides the clocking specifications for the processor cores and Table 81 provides the clocking specifications for the DDR/DDR2 memory bus. Table 82 provides the clocking specifications for the local bus.

Table 80. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	533	800	533	1000	533	1333	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio," and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 81. DDR/DDR2 Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
DDR/DDR2 Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the platform clock frequency.

Table 82. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	166	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by CCB clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for more information on this.

23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB) and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 83:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 83. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1

Table 83. CCB Clock Ratio (continued)

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0101	5:1	1101	20:1
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

23.3 e500 Core PLL Ratio

Table 84 describes the clock ratio between the e500 core complex bus (CCB)platform and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in Table 84.

Table 84. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

23.4 QE/SYSCLK PLL Ratio

The QE clock is defined by a multiplier and divisor applied to the SYSCLK input signal, as shown in the following equation:

QE clock = SYSCLK * cfg_ce_pll[0:4].

The multiplier and divisor is determined by the binary value of PA[0:4] at power up.

Table 85. QE Clock Multiplier cfg_ce_pll[0:4]

Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]	Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]
0_0000	16	1_0000	16
0_0001	Reserved	1_0001	17
0_0010	2	1_0010	18
0_0011	3	1_0011	19
0_0100	4	1_0100	20
0_0101	5	1_0101	21
0_0110	6	1_0110	22
0_0111	7	1_0111	23

Millennium Electronics offer different heat sink-to-ambient thermal resistances, that will allow the MPC8568E to function in various environments.

24.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8568E thermal model without a lid is shown in Figure 70. The substrate is modeled as a block 33x33x1.18 mm with an in-plane conductivity of 24 W/mK and a through-plane conductivity of 0.92 W/mK. The solder balls and air are modeled as a single block 33x33x0.58 mm with an in-plane conductivity of 0.034 W/mK and a through plane conductivity of 12.2 W/mK. The die is modeled as 8.2x12.1 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 5.3 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. See the case outline for actual dimensions.

Conductivity	Value	Unit
Die (8.2 × 12.1 × 0.75mm)		
Silicon	Temperature dependent	W/(m × K)
Bump/Underfill (8.2 × 12.1 × 0.75 mm) Collapsed Resistance		
k_z	5.3	
Substrate (33 × 33× 1.18 mm)		
k_x	24	
k_y	24	
k_z	0.92	
Soldera and Air (33 × 33 × 0.58 mm)		
k_x	0.034	
k_y	0.034	
k_z	12.2	

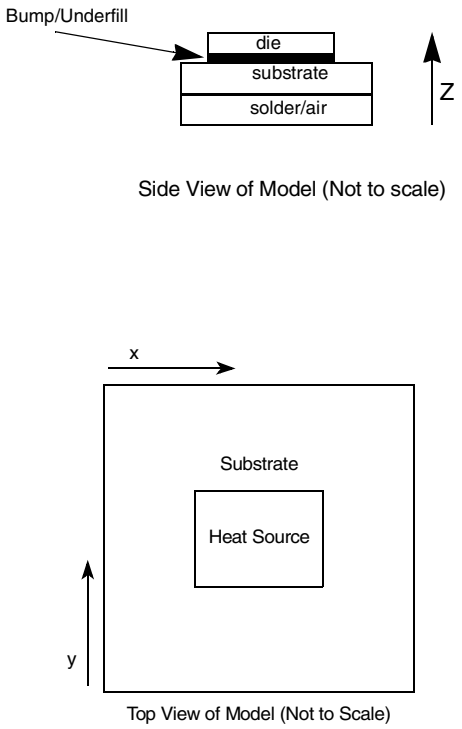

Figure 70. MPC8568E Thermal Model

24.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 87, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance