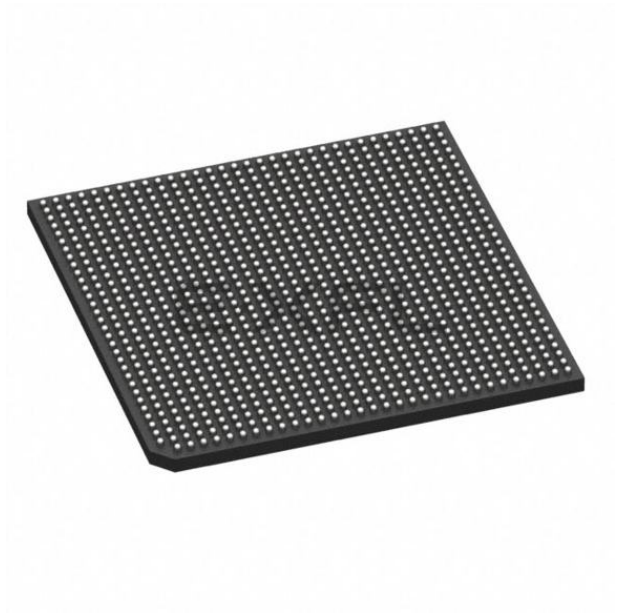

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8567evtaujj

— Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

1.2.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8568E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by eight local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8568E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8568E to be part of larger address maps such as the PCI or PCI Express 64-bit address environment and the RapidIO environment.

1.2.3 QUICC Engine

- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Includes support for the following protocols:
  - ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
  - ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
  - IMA and ATM Transmission convergence sub-layer
  - ATM OAM handling features compatible with ITU-T I.610
  - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
  - IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - ATM (AAL2/AAL5) to Ethernet (IP) interworking
  - Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
  - 256 channels of HDLC/Transparent or 128 channels of SS#7
- Includes support for the following serial interfaces:
  - Two UL2/POS-PHY interfaces with 124 Multi-PHY addresses on UTOPIA interface each or 31 Multi-PHY addresses on the POS interface each.

Table 7. SYSCLK AC Timing Specifications (continued)

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.2 PCI Clock Timing

Table 8 provides the PCI clock (PCI_CLK) AC timing specifications for the MPC8568E.

Table 8. PCI_CLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI_CLK frequency	f_{PCI_CLK}	—	—	66.7	MHz	—
PCI_CLK cycle time	t_{PCI_CLK}	15	—	—	ns	—
PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	1
PCI_CLK duty cycle	t_{KHK}/t_{PCI_CLK}	40	—	60	%	2
PCI_CLK jitter	—	—	—	+/– 150	ps	3,4

Notes:
1. Rise and fall times for PCI_CLK are measured at 0.4 V and 2.7 V.
2. Timing is guaranteed by design and characterization.
3. This represents the total input jitter—short term and long term—and is guaranteed by design.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the Time Base unit of the e500. There is no need for jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency. RTC may be grounded if not needed.

4.4 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8568E.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	 — —	 — —	 0.75 1.0	ns	—
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TVDD = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

4.5 FIFO Clock Speed Restrictions

Note the following FIFO maximum speed restrictions based on the platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 167 MHz

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8568E. Table 10 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the MPC8568E.

Table 11 provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Platform PLL lock times	—	100	µs	—
QE PLL lock times	—	100	µs	—
CPU PLL lock times	—	100	µs	—
PCI PLL lock times	—	100	µs	—
Local bus PLL	—	100	µs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8568E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

Table 30. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

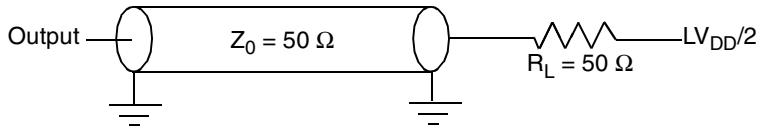


Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.

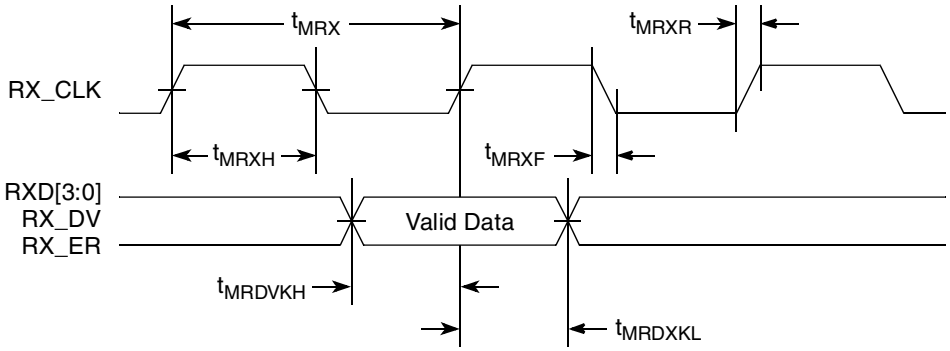


Figure 14. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n* TSECn_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	1.0	2.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	1.0	2.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

A timing diagram for TBI receive appears in Figure 17.

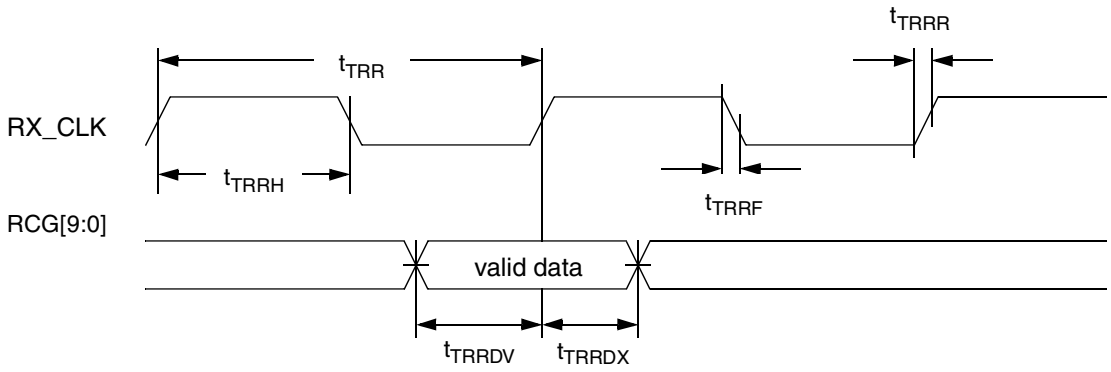


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}[5]	7.2	8.0	8.8	ns

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

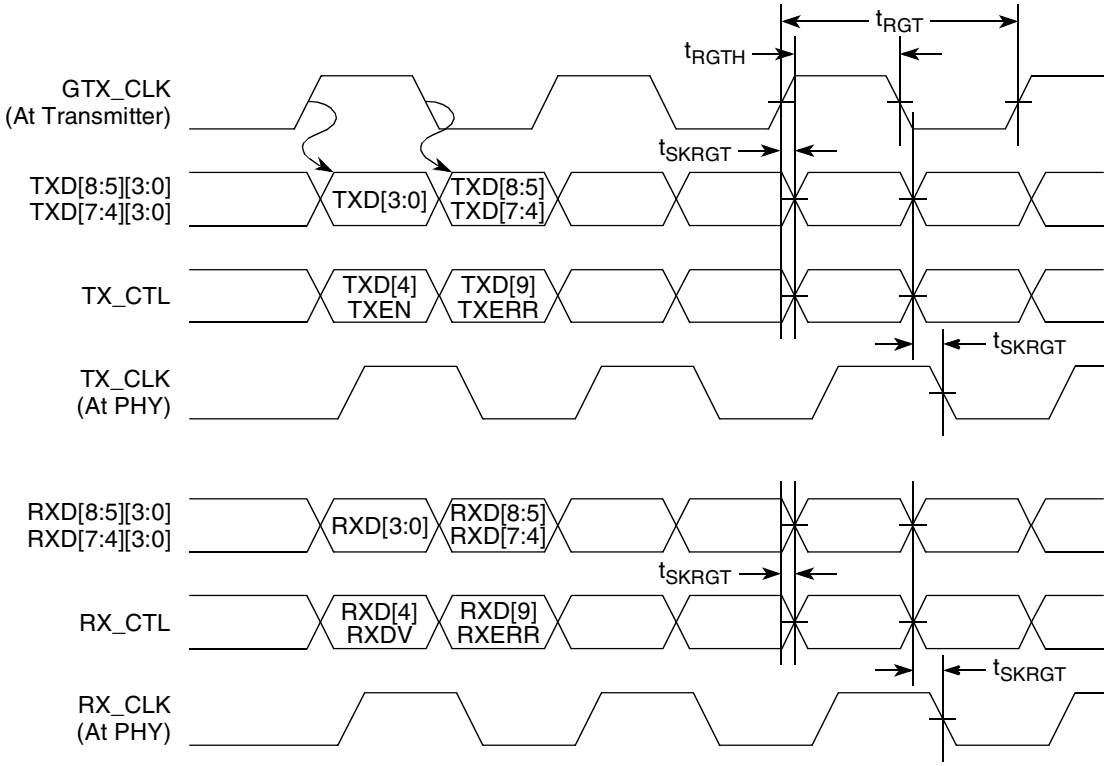


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 35.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

Table 43. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	-0.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	-0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

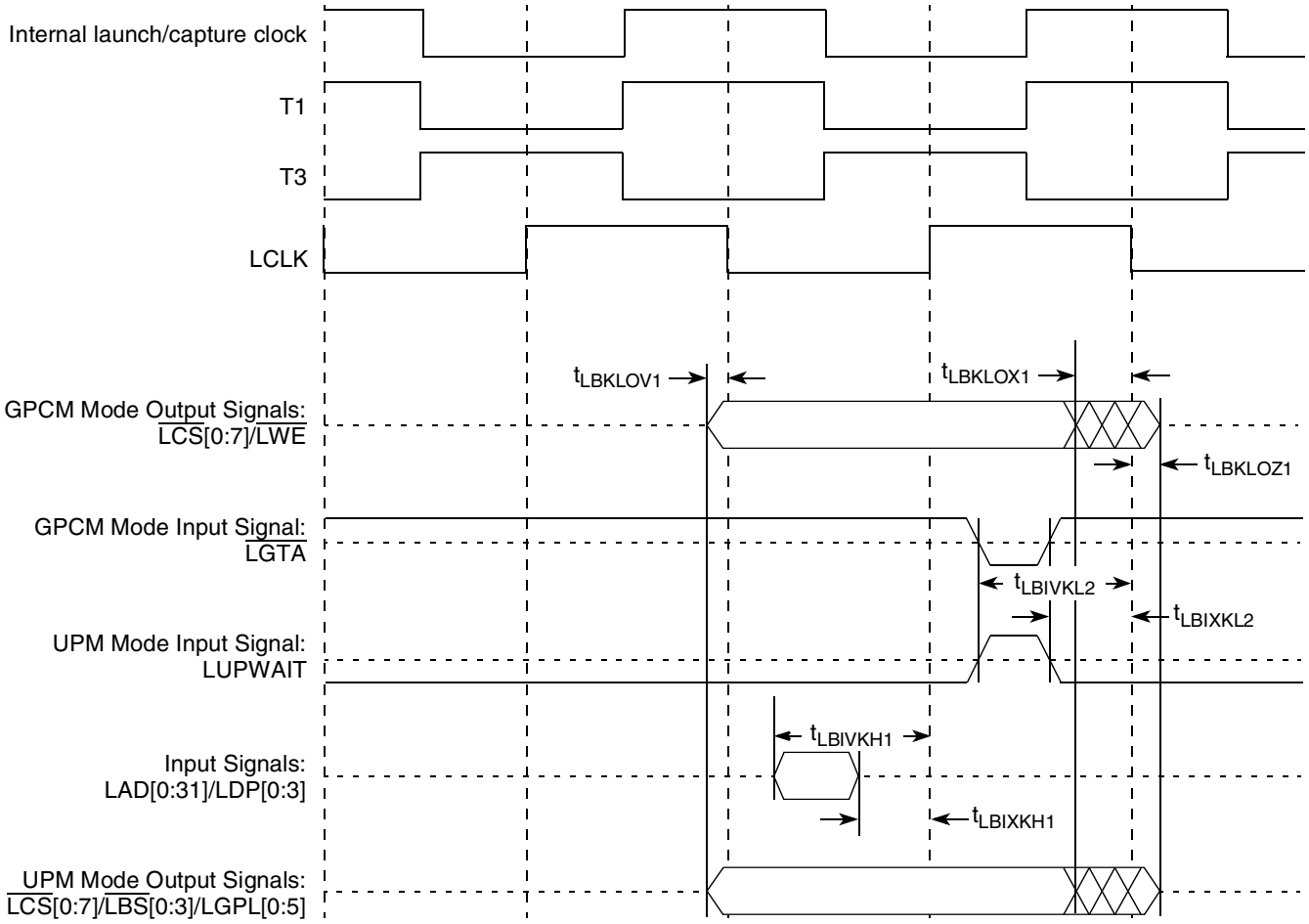


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

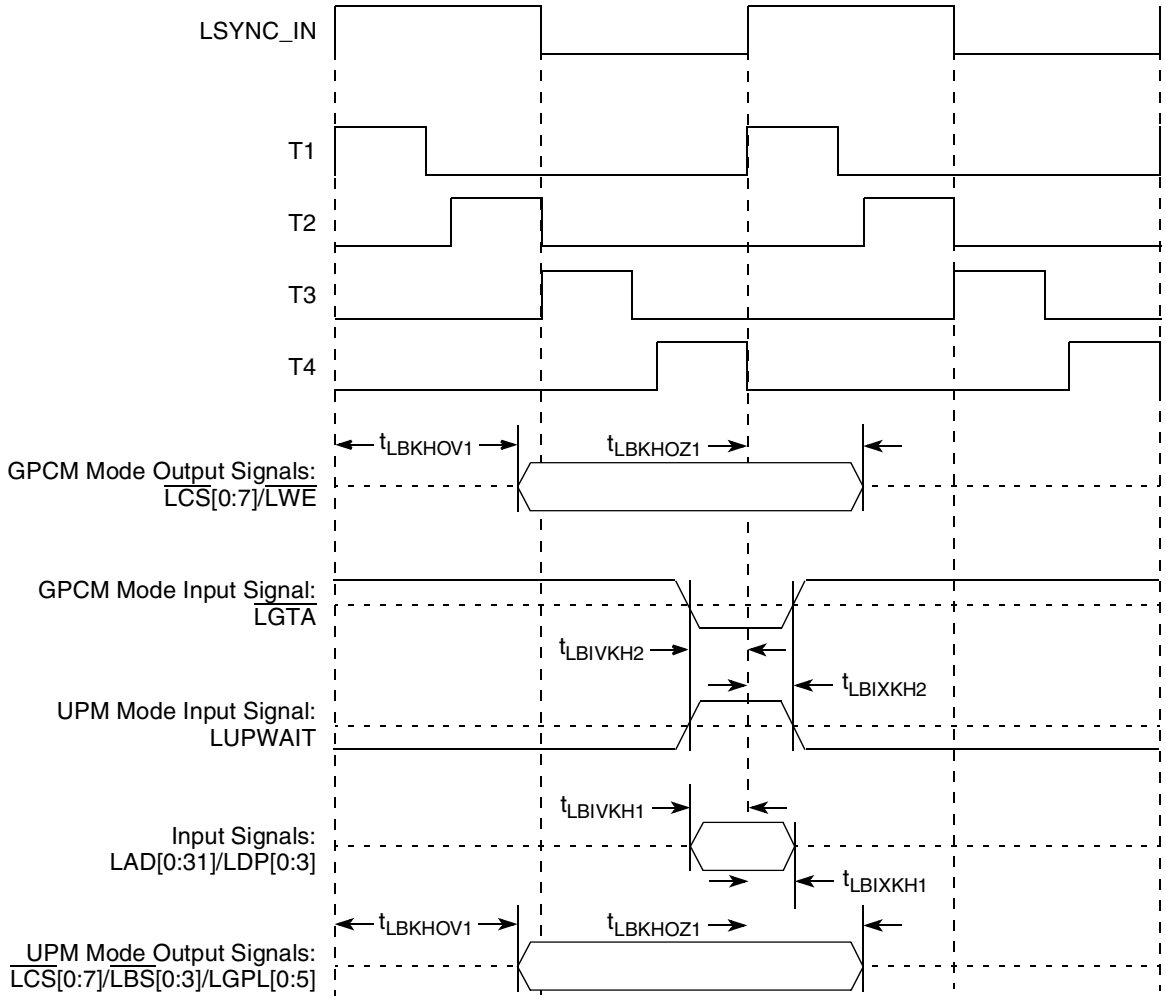


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$.

The following sections describe the SerDes reference clock requirements and some application information.

13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 40 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for SCOREVDD and XVDD are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 40. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SCOREGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8mA) while the minimum common mode input level is 0.1V above SCOREGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 ohms to SCOREGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

Figure 47 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8568E SerDes reference clock input's DC requirement.

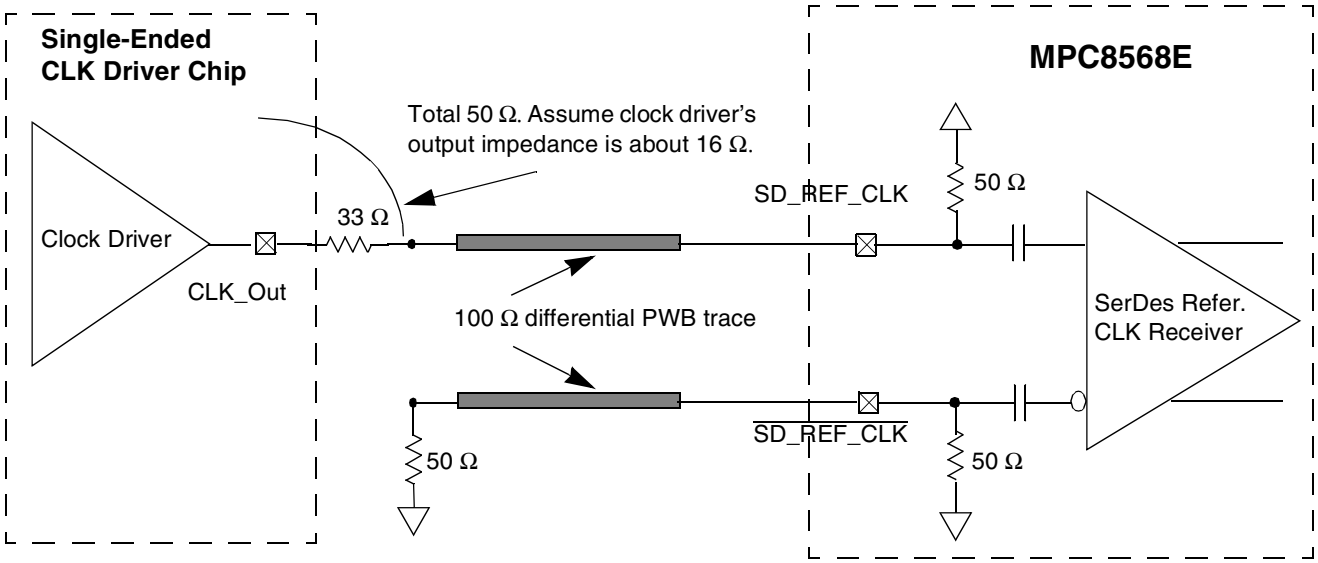


Figure 47. Single-Ended Connection (Reference Only)

13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 14.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 15.2, "AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK"

13.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

Table 51. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS($\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$\|V_{TX-CM-DC\ (during\ L0)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\|$<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\|$ <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = $\|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\|$ <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	10	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4

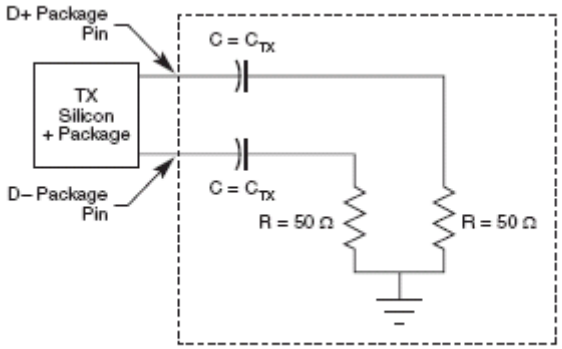


Figure 51. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8568E, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

22 Package and Pinout

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8568E FC-PBGA

The package parameters are as provided in the following list. The package type is 33mm × 33mm, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Pitch	1 mm
Module height	2.23 – 2.75 mm
Solder Balls	96.5% Sn 3.5% Ag
Ball diameter (typical)	0.6 mm

22.2 Mechanical Dimensions of the MPC8568E FC-PBGA

Figure 68 shows the top view, bottom and side view of the MPC8568E 1023 FC-PBGA package.

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Debug				
TRIG_IN	AL29	I	OV_{DD}	—
TRIG_OUT	AM29	O	OV_{DD}	6,9,19,29
MSRCID[0:1]	AK29, AJ29	O	OV_{DD}	5,6,9
MSRCID[2:4]	AM28, AL28, AK27	O	OV_{DD}	6,19,29
MDVAL	AJ28	O	OV_{DD}	6
CLK_OUT	AF18	O	OV_{DD}	11
Clock				
RTC	AH20	I	OV_{DD}	—
SYSCLK	AK22	I	OV_{DD}	—
JTAG				
TCK	AH18	I	OV_{DD}	—
TDI	AH19	I	OV_{DD}	12
TDO	AJ18	O	OV_{DD}	11
TMS	AK19	I	OV_{DD}	12
$\overline{\text{TRST}}$	AK20	I	OV_{DD}	12
DFT				
L1_TSTCLK	AJ20	I	OV_{DD}	25
L2_TSTCLK	AJ19	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH31	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AJ31	I	OV_{DD}	25
Thermal Management				
THERM0	AB30	—	—	14
THERM1	AB31	—	—	14
Power Management				
ASLEEP	AK21	O	OV_{DD}	9,19,29

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

Table 79 provides the pin-out listing for the MPC8567E 1023 FC-PBGA package.

Table 79. MPC8567E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	—
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2

23.5.2 Minimum Platform Frequency Requirements for PCI Express, SRIO, PCI interfaces Operation

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Note that the “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

For proper PCI operation in synchronous mode, the minimum CCB:SYSCLK ratio is 6:1.

24 Thermal

This section describes the thermal specifications of the MPC8568E.

24.1 Thermal Characteristics

Table 87 provides the package thermal characteristics.

Table 87. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on single layer board (1s)	$R_{\theta JA}$	16	•C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JA}$	13	•C/W	1, 2
Junction-to-board	$R_{\theta JB}$	9	•C/W	3
Junction-to-case	$R_{\theta JC}$	<0.1	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

24.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP, PA[5].

Three test pins also require pull-up resistors (100 Ω–1 KΩ). These pins are L1_TSTCLK, L2_TSTCLK, and LSSD_MODE. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

25.7 Configuration Pin Muxing

The MPC8568E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins. These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip pull-up resistors of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform /system clocks after HRESET deassertion to ensure capture of the reset value). When the HRESET is negated, the pull-up resistor is also disabled, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

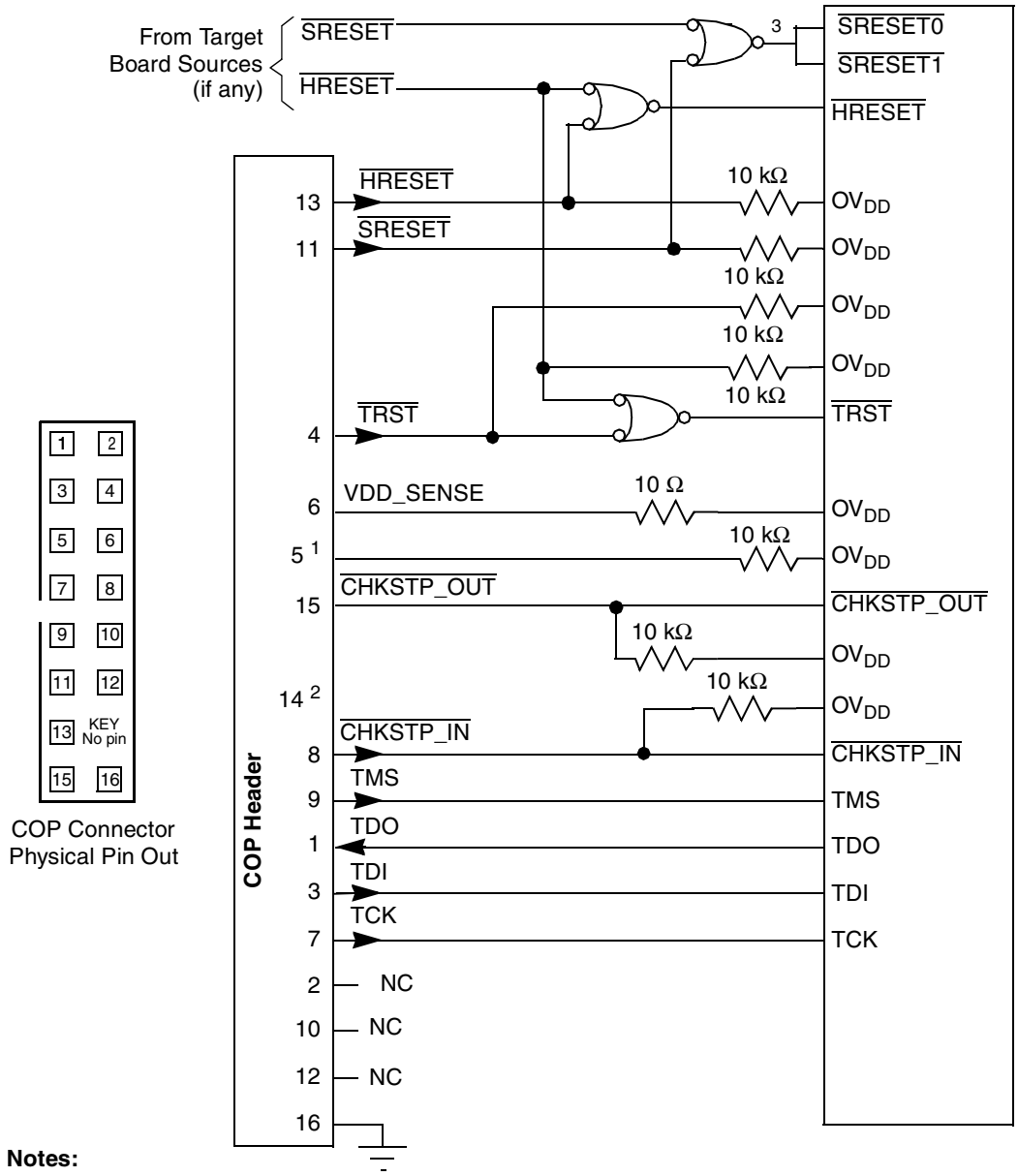
Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

25.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement Power Architecture. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Use a NOR gate with sufficient drive strength to drive two inputs.

Figure 75. JTAG Interface Connection

25.9 Guidelines for High-Speed Interface Termination

25.9.1 Unused output

Any of the outputs that are unused should be left unconnected. These signals are:

- SD_TX[7:0]