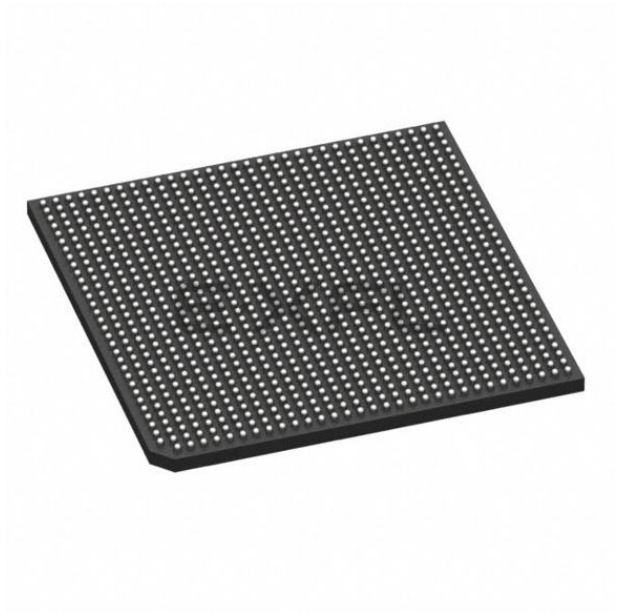

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCPBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8568evtaujj

Table 1. Supported eTSEC1 and eTSEC2 Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

1.2.6 DDR SDRAM Controller

The MPC8568E supports DDR SDRAM and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbits, 2 Gbits and 4 Gbits. Four chip select signals support

1.2.15 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8568E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	SCOREVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
eTSEC1, eTSEC2 I/O Voltage	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
QE UCC1/UCC2 Ethernet Interface I/O Voltage	TV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	3
Local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

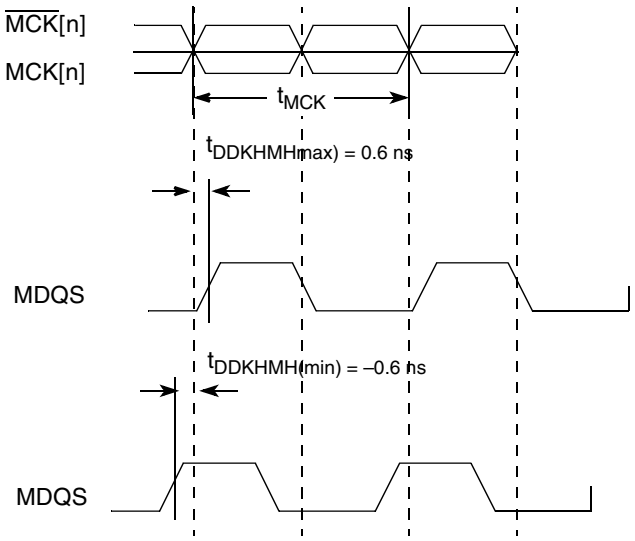


Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR SDRAM output timing diagram.

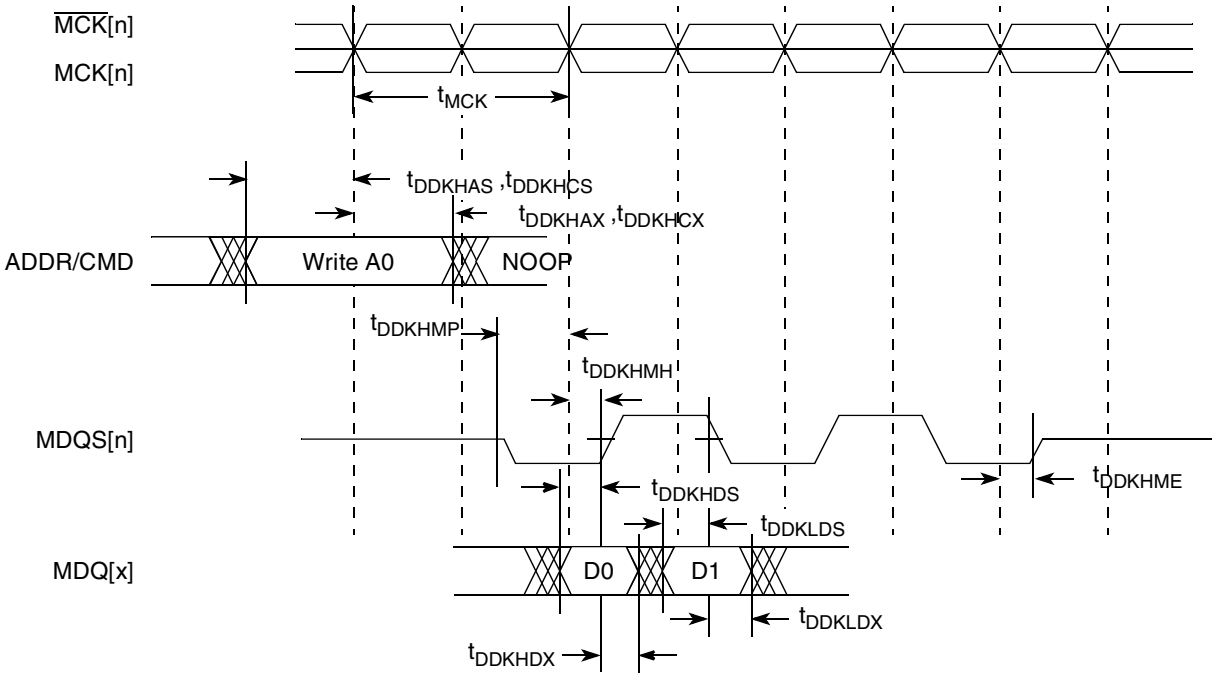


Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

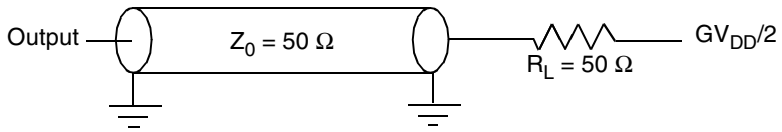


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8568E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

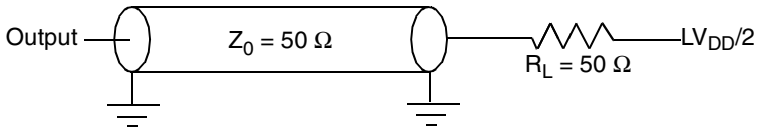


Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.

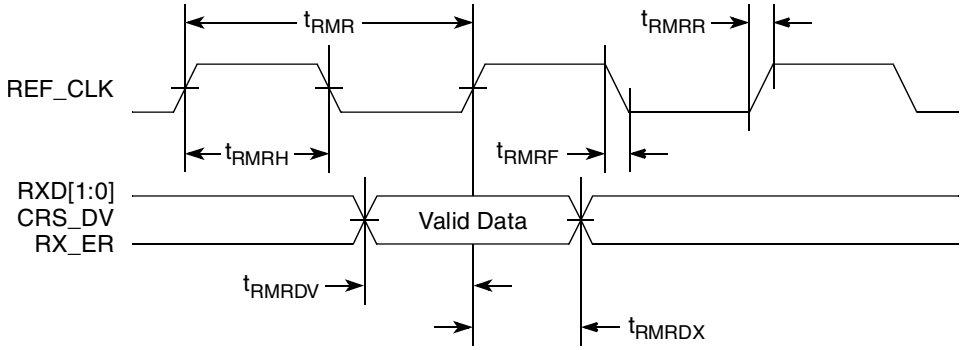


Figure 21. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

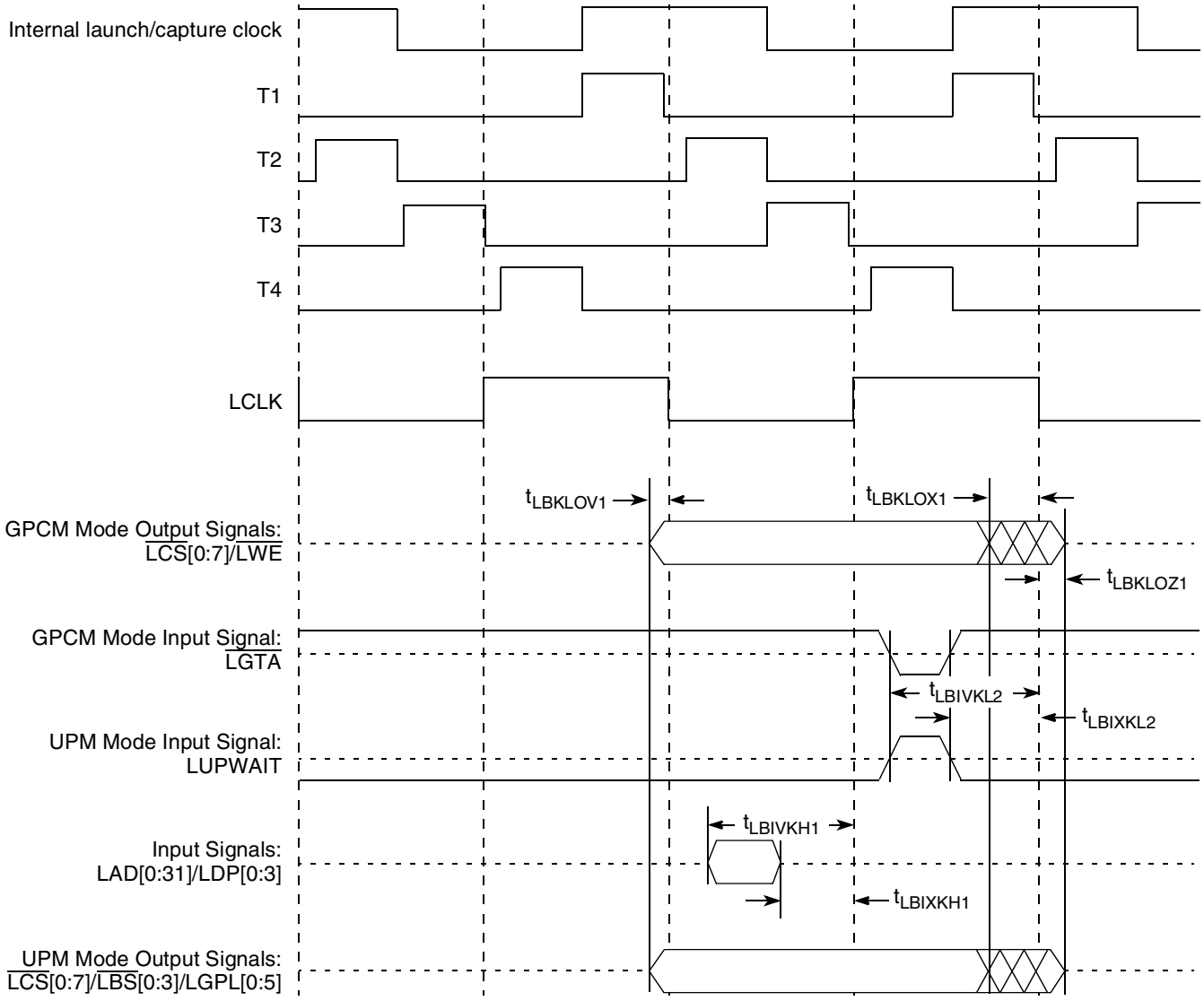


Figure 29. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

Figure 44 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8568 SerDes reference clock input's DC requirement.

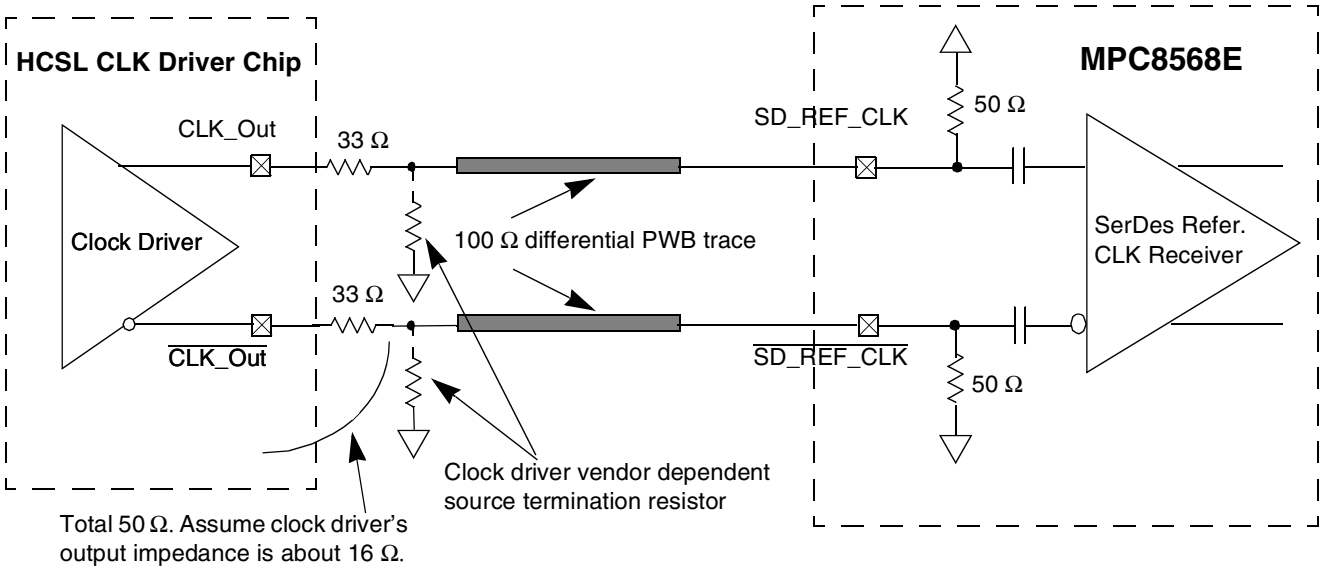


Figure 44. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8568 SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

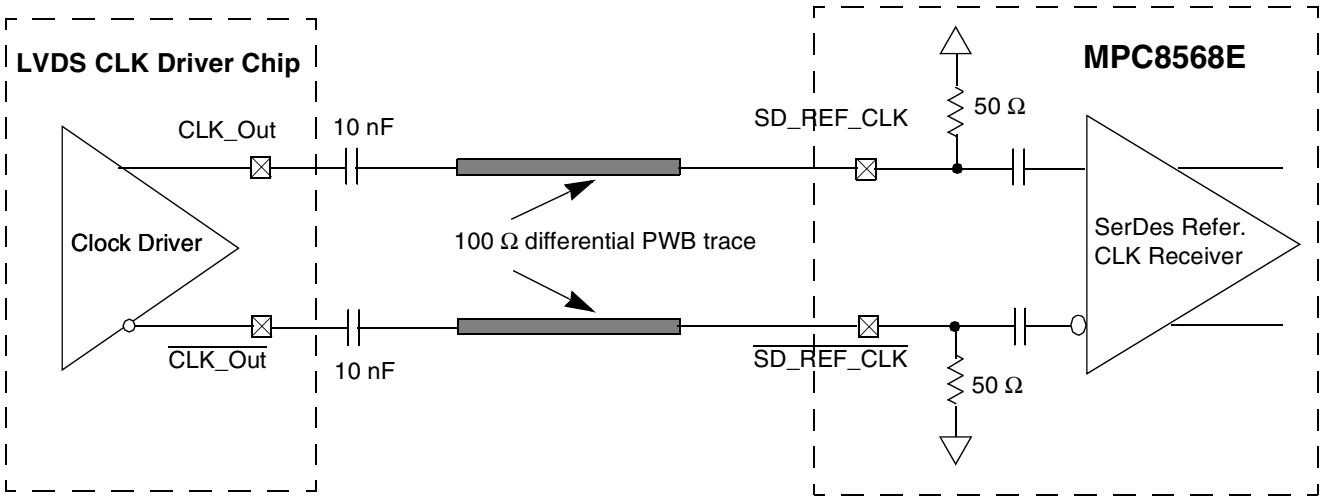


Figure 45. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

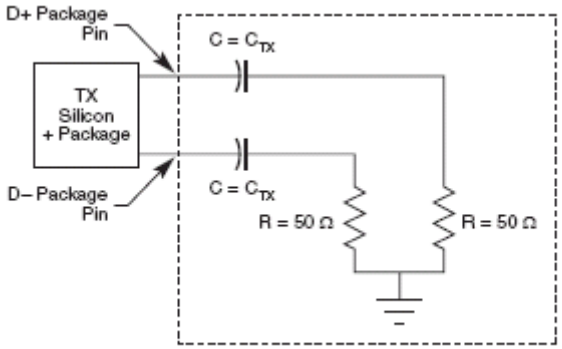


Figure 51. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8568E, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

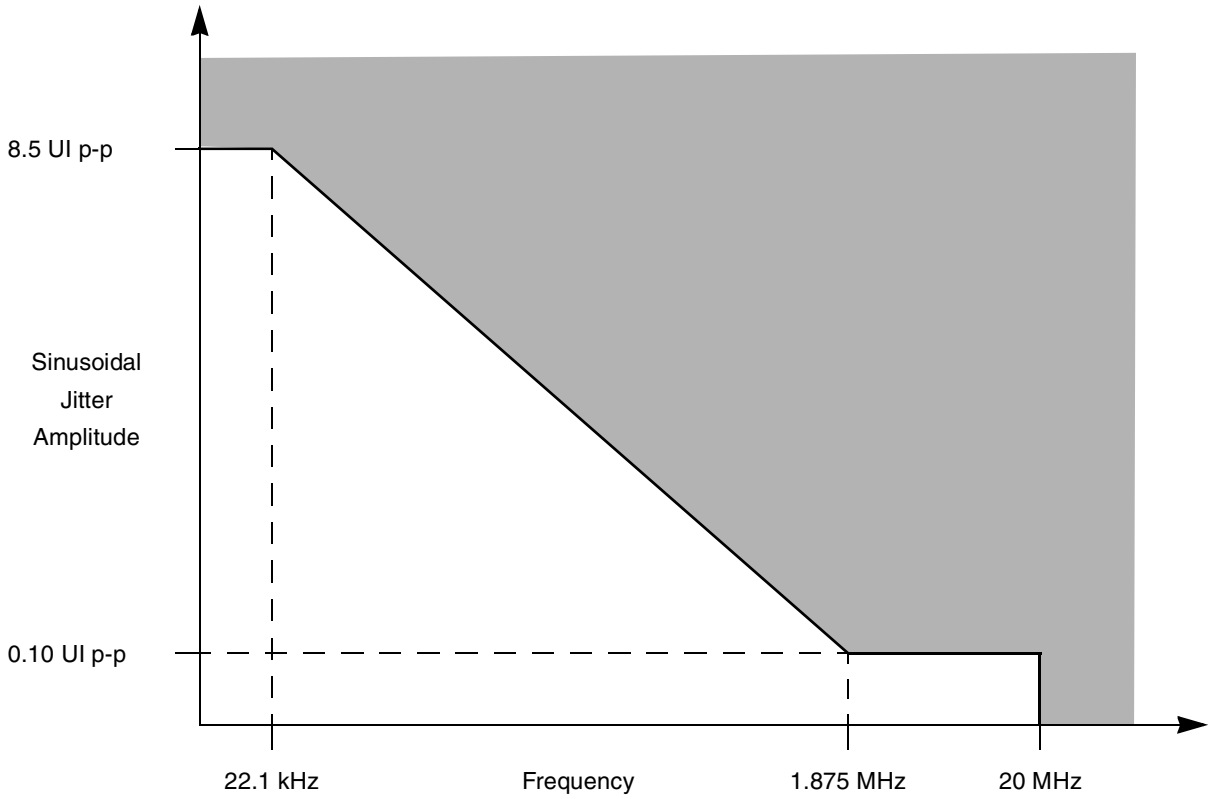


Figure 54. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 61, Table 62, Table 63) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 55 with the parameters specified in Table . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω +/– 5% differential resistive load.

17 PIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8568E.

17.1 PIC DC Electrical Characteristics

Table 67 provides the DC electrical characteristics for the external interrupt pins of the MPC8568E.

Table 67. PIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—		±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

17.2 PIC AC Timing Specifications

Table 68 provides the PIC input and output AC timing specifications.

Table 68. PIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8568E.

18.1 SPI DC Electrical Characteristics

Table 69 provides the DC electrical characteristics for the MPC8568E SPI.

Table 69. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	μA

18.2 SPI AC Timing Specifications

Table 70 and provide the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 57 provides the AC test load for the SPI.

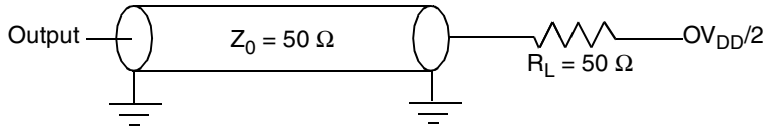


Figure 57. SPI AC Test Load

Table 76. HDLC, BiSync, Transparent AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 77. Synchronous UART AC Timing Specifications

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns
Outputs—External clock delay	t_{HEKHOV}	1	14	ns
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	11	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 65 provides the AC test load.

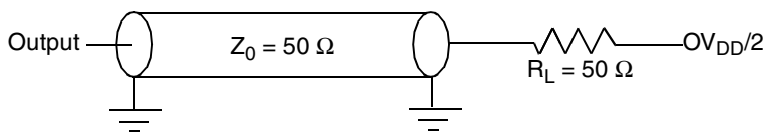


Figure 65. AC Test Load

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A24	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	K32	I	200Ω to GND	—
SD_IMP_CAL_TX	AA28	I	100Ω to GND	—
SD_PLL_TPA	R30	O	—	24

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_REQ[4:1]	AG29, AJ27, AH29, AB17	I	OV_{DD}	—
PCI_REQ[0]	AC17	I/O	OV_{DD}	—
PCI_CLK	AM26	I	OV_{DD}	39
PCI_DEVSEL	AK23	I/O	OV_{DD}	2
PCI_FRAME	AE21	I/O	OV_{DD}	2
PCI_IDSEL	AB19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	B22, C22, E20, A19, C23, A22, A20, C20, G22, E22, E16, F16, E23, F23, F17, H17, A18, A17, B16, C16, B19, C19, E17, A16, A13, A14, A12, C12, A15, B15, B13, C13, G12, G11, H8, F8, D13, F12, E9, F9, A7, B7, C5, E5, C8, E8, D6, A5, E6, G6, E1, F1, G7, E7, E2, D1, C4, A3, B1, C1, A4, B4, C2, D2	I/O	GV_{DD}	—
MECC[0:7]	C11, E11, D9, A8, D12, A11, A9, C9	I/O	GV_{DD}	—
MDM[0:8]	A21, E21, D18, B14, F11, A6, G5, A2, A10	O	GV_{DD}	—
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
MDQS[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
MWE	K3	O	GV_{DD}	—
MCAS	L3	O	GV_{DD}	—
MRAS	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
MCS[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
MCK[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9

system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 69. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

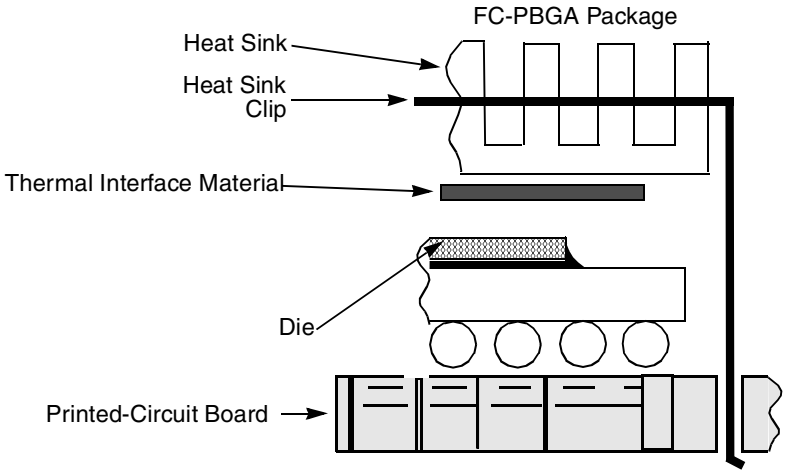


Figure 69. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, and

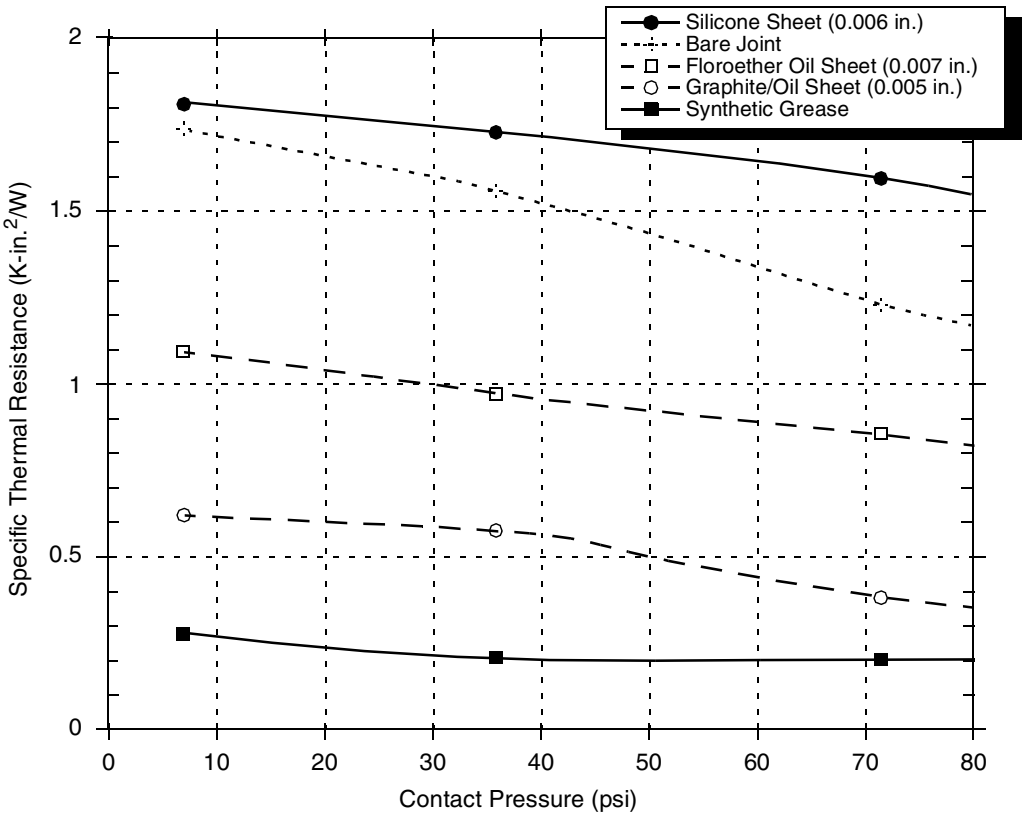


Figure 72. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 1023FC-PBGA the footprint, without the inductance of vias.

Figure 73 shows the PLL power supply filter circuits for all PLLs except SerDes PLL.

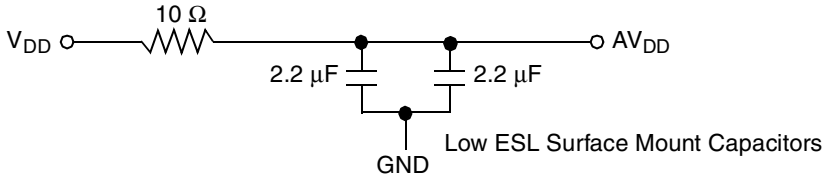
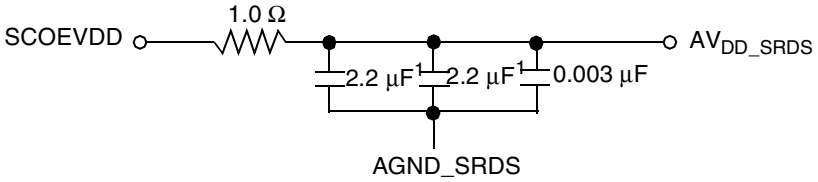


Figure 73. MPC8568E PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} and AGND_SRDS ball to ensure it filters out as much noise as possible. The 0.003-µF capacitor is closest to the ball, followed by the 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 74. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD_SRDS} should be a filtered version of SCOREVDD.
- The transmitter output signals on the SerDes interface are fed from the XV_{DD} power plan.
- Power: XVDD consumes less than 300mW. SCOREVDD + AV_{DD_SRDS} consumes less than 750mW.

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. MPC8568E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

- $\overline{\text{SD\_TX}}$[7:0]

25.9.2 Unused input

25.9.2.1 SerDes block power not supplied

If the high speed interface is not used at all, then SCOREVDD/XVDD/AV_{DD_SRDS} can be tied to GND, all receiver inputs should be tied to the GND as well. This includes:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$
- $\overline{\text{SD\_RX\_CLK}}$
- $\overline{\text{SD\_RX\_FRM\_CTL}}$

25.9.2.2 SerDes Interface Partly used

If the high-speed SerDes interface is partly unused, any of the unused receiver pins should be terminated as follows:

- SD_RX[7:0] = tied to SCOREGND
- $\overline{\text{SD\_RX}}$[7:0] = tied to SCOREGND
- SD_REF_CLK = tied to SCOREGND
- $\overline{\text{SD\_REF\_CLK}}$ = tied to SCOREGND

NOTE

Power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

During HRESET/POR, the high-speed interface must be in Serial RapidIO mode and/or PCI Express mode according to the state of the PE[8:10]. Software must disable this mode through DEVDISR[SRIO] or DEVDISR[PCIE] accordingly during software initialization.

26 Ordering Information

Contact your local Freescale sales office or regional marketing team for order information.

26.1 Part Marking

Parts are marked as the example shown in Figure 76.

FC-PBGA

Notes:

MPC856Xxxxxxx is the orderable part number
ATWLYYWW is the freescale assembly, year and workweek code
MMMMM is the mask code
CCCC is the contry code for assembly.
YWWLAZ is the trace code for assembly.

Figure 76. Part Marking for FC-PBGA Device

26.2 Part Number Decoder

Figure 77 shows the MPC8568E/MPC8567E number decoder.

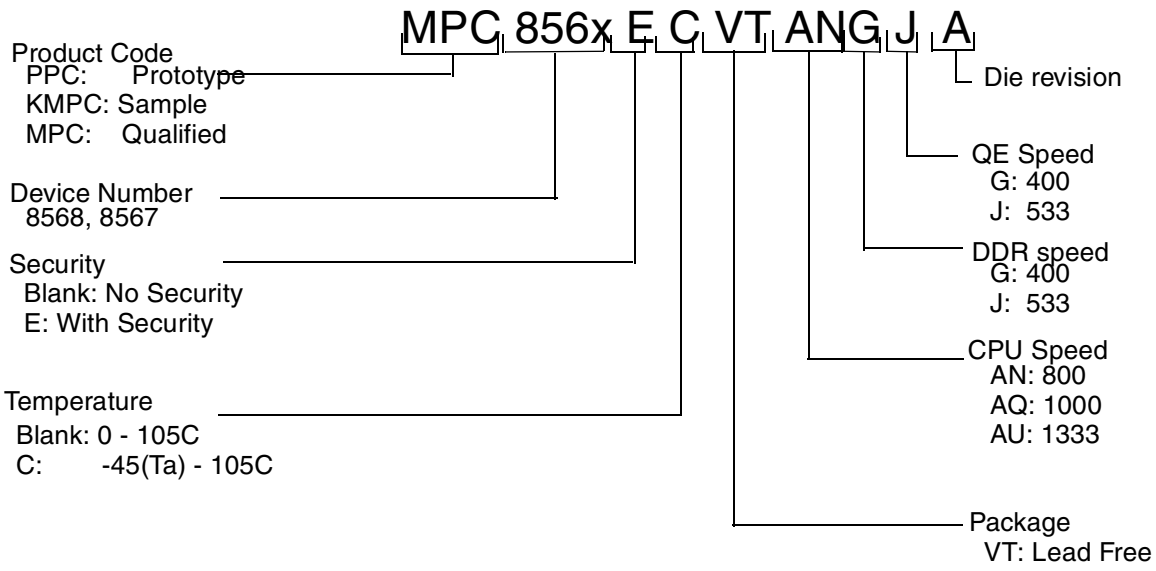


Figure 77. MPC8568E Part Number Decoder

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Document Number: MPC8568EEC
Rev. 1
10/2010

freescale semiconductor