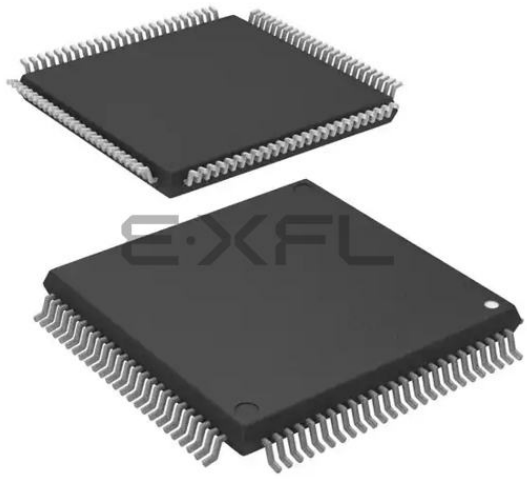

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38099fp10v

User's Manual

16

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

H8/38099 Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer H8 Family / H8/300H Super Low Power Series

H8/38099F
H8/38099
H8/38098

Renesas Electronics
www.renesas.com

Rev.2.00 2007.07

4.2 Input/Output Pins

Table 4.1 shows the pin configuration of the interrupt controller.

Table 4.1 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{NMI}}$	Input	Nonmaskable external interrupt pin Rising or falling edge can be selected
IRQAEC	Input	Maskable external interrupt pin Rising, falling, or both edges can be selected
$\overline{\text{IRQ4}}$	Input	Maskable external interrupt pins Rising or falling edge can be selected
$\overline{\text{IRQ3}}$	Input	
$\overline{\text{IRQ1}}$	Input	
$\overline{\text{IRQ0}}$	Input	
$\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$	Input	Maskable external interrupt pins Accepted at a rising or falling edge

4.3 Register Descriptions

The interrupt controller has the following registers.

- Interrupt edge select register (IEGR)
- Wakeup edge select register (WEGR)
- Interrupt enable register 1 (IENR1)
- Interrupt enable register 2 (IENR2)
- Interrupt request register 1 (IRR1)
- Interrupt request register 2 (IRR2)
- Wakeup interrupt request register (IWPR)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt priority register F (IPRF)
- Interrupt mask register (INTM)

6.5 Usage Notes

6.5.1 Standby Mode Transition and Pin States

When a SLEEP instruction is executed in active (high-speed) mode or active (medium-speed) mode while the SSBY and TMA3 bits in SYSCR1 are set to 1 and the LSON bit in SYSCR1 is cleared to 0, a transition is made to standby mode. At the same time, pins go to the high-impedance state (except pins for which the pull-up MOS is designated as on). Figure 6.2 shows the timing in this case.

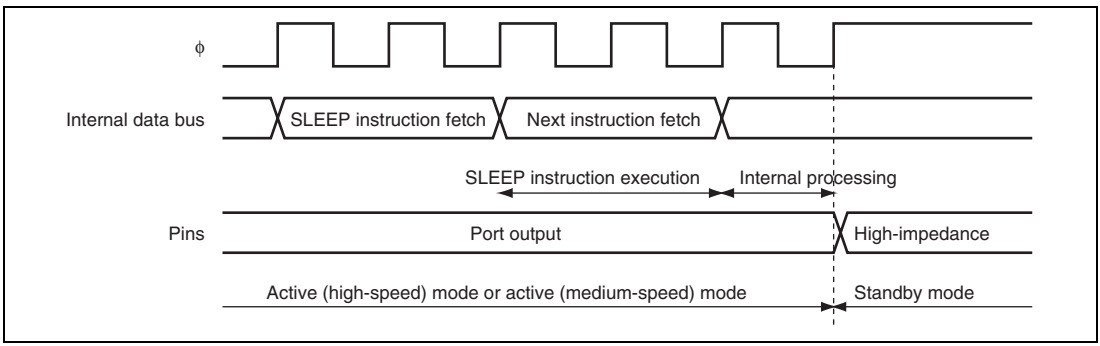
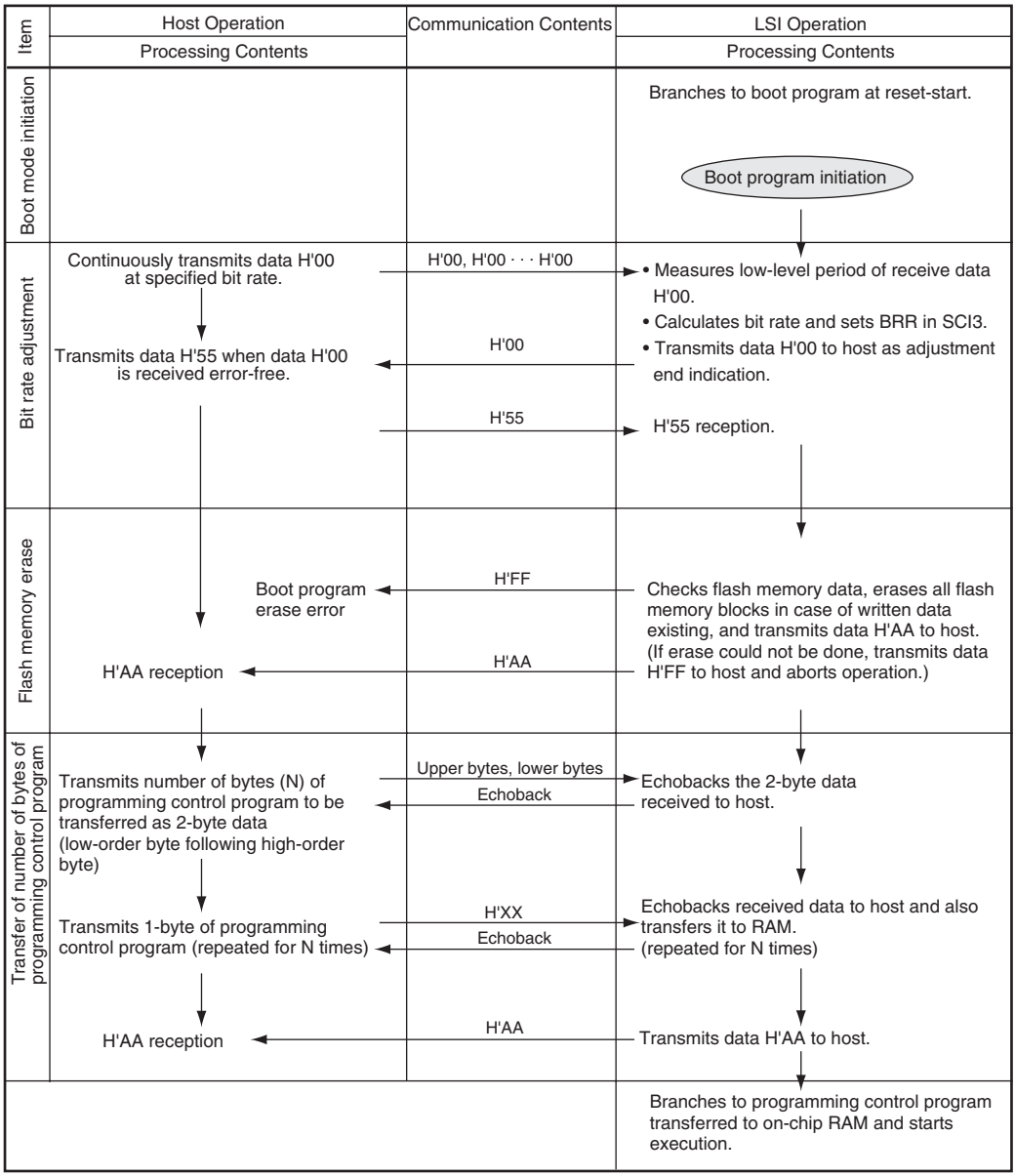
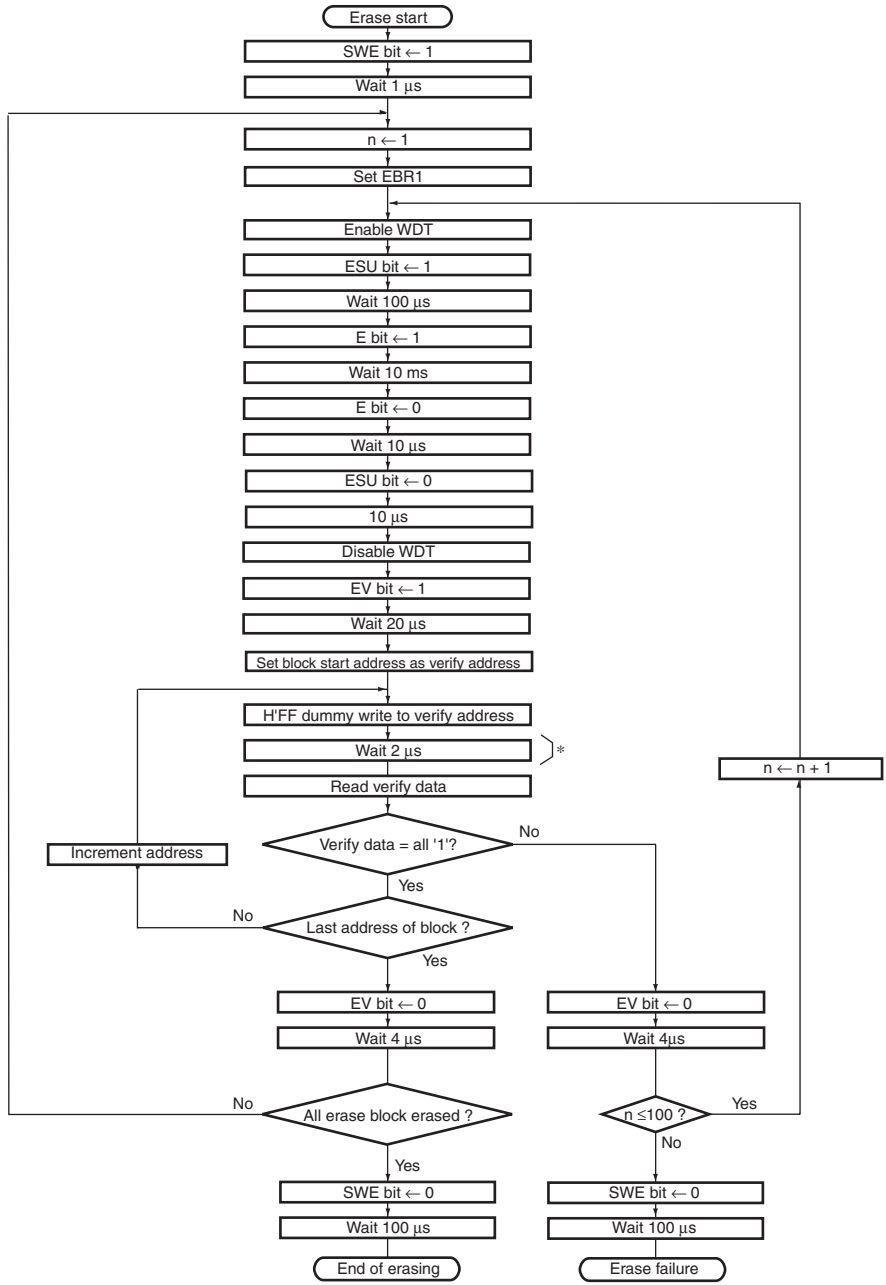


Figure 6.2 Standby Mode Transition and Pin States

Table 7.2 Boot Mode Operation





Note: * The RTS instruction must not be used during a period between dummy writing of H'FF to a verify address and verify data reading.

Figure 7.5 Erase/Erase-Verify Flowchart

- P15/TIOCB2 pin

Register Name	TMDR_2	TIOR_2	TCR_2	PCR1	Pin Function
Bit Name	MD1, MD0	IOB3 to IOB0	CCLR1, CCLR0	PCR15	
Setting Value	B'00	B'0x00	B'xx	0	P15 input pin
				1	P15 output pin
		B'1xxx		0	P15 input/TIOCB2 input pin
				1	P15 output/TIOCB2 input pin
		B'0001 to B'0011, B'0101 to B'0111		x	TIOCB2 output pin
	B'01	B'xxxx		0	P15 input pin
				1	P15 output pin
	B'10			0	P15 input pin
				1	P15 output pin
	B'11	B'xx00		0	P15 input pin
				1	P15 output pin
		Other than B'xx00	B'10	0	P15 input pin
				1	P15 output pin
			Other than B'10	x	TIOCB2 output pin

[Legend]
x: Don't care

11.2 Input/Output Pins

Table 11.1 shows the input/output pins of the timer C.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer C event input	TMIC	Input	Input pin for event input to TCC
Timer C up/down select	UD	Input	Timer C up/down-count selection

11.3 Register Descriptions

Timer C has the following registers. For details on clock halt register 3 (CKSTPR3), see section 6.1.4, Clock Halt Registers 1 to 3 (CKSTPR1 to CKSTPR3).

- Timer mode register C (TMC)
- Timer counter C (TCC)
- Timer load register (TLC)
- Clock halt register 3 (CKSTPR3)

11.3.1 Timer Mode Register C (TMC)

TMC is an 8-bit read/write register for selecting the auto-reload function and input clock, and performing up/down-counter control.

Upon reset, TMC is initialized to H'10.

Bit	Bit Name	Initial Value	R/W	Description
7	TMC7	0	R/W	Auto-Reload Function Select Selects whether timer C is used as an interval timer or auto-reload timer. 0: Interval timer function 1: Auto-reload function
6	TMC6	0	R/W	Counter Up/Down Control
5	TMC5	0	R/W	Specifies whether TCC functions as an up-counter or down-counter, or whether selection of counting up or down is controlled by the input signal level on the UD pin. 00: TCC is an up-counter 01: TCC is a down-counter 1x: Selection through the signal level on the UD pin UD pin input high: Down-counter UD pin input low: Up-counter
4	—	1	—	Reserved This bit is always read as 1 and cannot be modified.

17.3.12 Serial Extended Mode Register (SEMR)

SEMR controls extended functions of the SCI3_1, i.e. specifies the basic clock in asynchronous mode.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved The write value should always be 0.
3	ABCS	0	R/W	Asynchronous Mode Basic Clock Select Selects the basic clock for one-bit interval in asynchronous mode. The ABCS setting is enabled in asynchronous mode (COM = 0 in SMR3) 0: Basic clock with a frequency 16 times the transfer rate 1: Basic clock with a frequency 8 times the transfer rate Clear this bit to 0 when the IrDA function is enabled.
2 to 0	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.

17.4.4 Serial Data Reception

Figure 17.7 shows an example of operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI3 monitors the communication line. If a start bit is detected, the SCI3 performs internal synchronization, receives data in RSR, and checks the parity bit and stop bit.

- Parity check

  The SCI3 checks that the number of 1 bits in the receive data conforms to the parity (odd or even) set in bit PM in the serial mode register (SMR).
- Stop bit check

  The SCI3 checks that the stop bit is 1. If two stop bits are used, only the first is checked.
- Status check

  The SCI3 checks that bit RDRF is set to 0, indicating that the receive data can be transferred from RSR to RDR.

2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag is still set to 1), the OER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI3 interrupt request is generated. Receive data is not transferred to RDR.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI3 interrupt request is generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE3 bit in SCR is set to 1 at this time, an ERI3 interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI3 interrupt request is generated. Continuous reception is possible because the RXI3 interrupt routine reads the receive data transferred to RDR before reception of the next receive data has been completed.

17.5.4 Serial Data Reception (Clock Synchronous Mode)

Figure 17.12 shows an example of SCI3 operation for reception in clock synchronous mode. In serial reception, the SCI3 operates as described below.

1. The SCI3 performs internal initialization synchronous with a synchronous clock input or output, starts receiving data.
2. The SCI3 stores the received data in RSR.
3. If an overrun error occurs (when reception of the next data is completed while the RDRF flag in SSR is still set to 1), the OER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI3 interrupt request is generated, receive data is not transferred to RDR, and the RDRF flag remains to be set to 1.
4. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI3 interrupt request is generated.

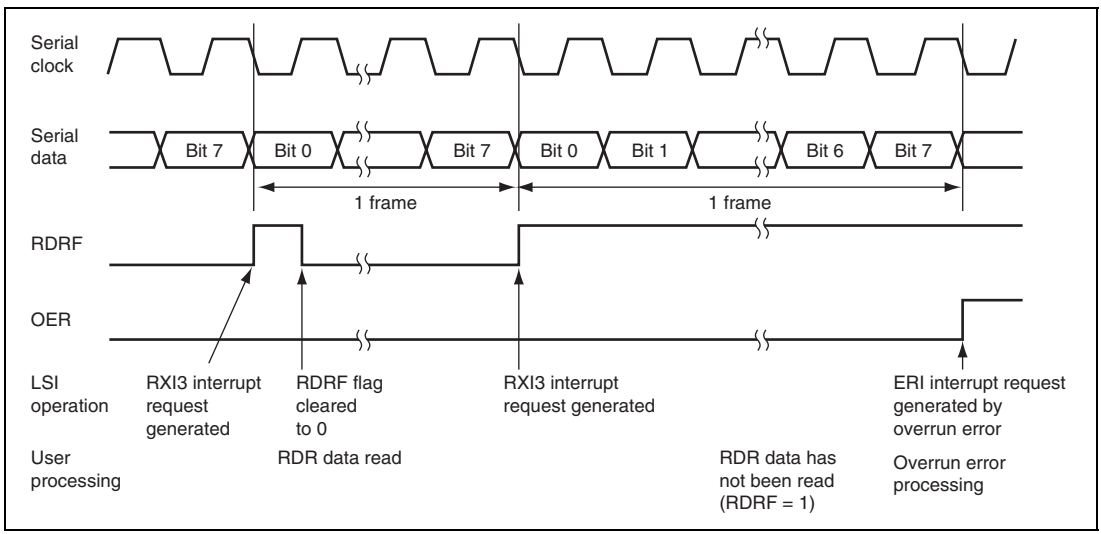


Figure 17.12 Example of SCI3 Reception Operation in Clock Synchronous Mode

21.3.1 LCD Port Control Register (LPCR)

LPCR selects the duty cycle, LCD driver, and pin functions.

Bit	Bit Name	Initial Value	R/W	Description
7	DTS1	0	R/W	Duty Cycle Select 1 and 0
6	DTS0	0	R/W	Common Function Select
5	CMX	0	R/W	The combination of DTS1 and DTS0 selects static, 1/2, 1/3, or 1/4 duty. CMX specifies whether or not the same waveform is to be output from multiple pins to increase the common drive power when not all common pins are used due to the selected duty. For details, see table 21.2.
4	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
3	SGS3	0	R/W	Segment Driver Select 3 to 0
2	SGS2	0	R/W	Select the segment drivers to be used.
1	SGS1	0	R/W	For details, see table 21.3.
0	SGS0	0	R/W	

Table 21.2 Duty Cycle and Common Function Selection

Bit 7: DTS1	Bit 6: DTS0	Bit 5: CMX	Duty Cycle	Common Drivers	Notes
0	0	0	Static	COM1	Do not use COM4, COM3, and COM2
		1		COM4 to COM1	COM4, COM3, and COM2 output the same waveform as COM1
	1	0	1/2 duty	COM2 to COM1	Do not use COM4 and COM3
		1		COM4 to COM1	COM4 outputs the same waveform as COM3, and COM2 outputs the same waveform as COM1
1	0	0	1/3 duty	COM3 to COM1	Do not use COM4
		1		COM4 to COM1	Do not use COM4
	1	x	1/4 duty	COM4 to COM1	—

[Legend]

x: Don't care

22.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. For slave receive mode operation timing, refer to figures 22.11 and 22.12. The reception procedure and operations in slave receive mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting) Set the MST and TRS bits in ICCR1 to select slave receive mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise of the 9th clock pulse. At the same time, RDRF in ICSR is set to read ICDRR (dummy read). (Since the read data show the slave address and R/$\overline{W}$, it is not used.)
3. Read ICDRR every time RDRF is set. If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read. The change of the acknowledge before reading ICDRR, to be returned to the master device, is reflected to the next transmit frame.
4. The last byte data is read by reading ICDRR.

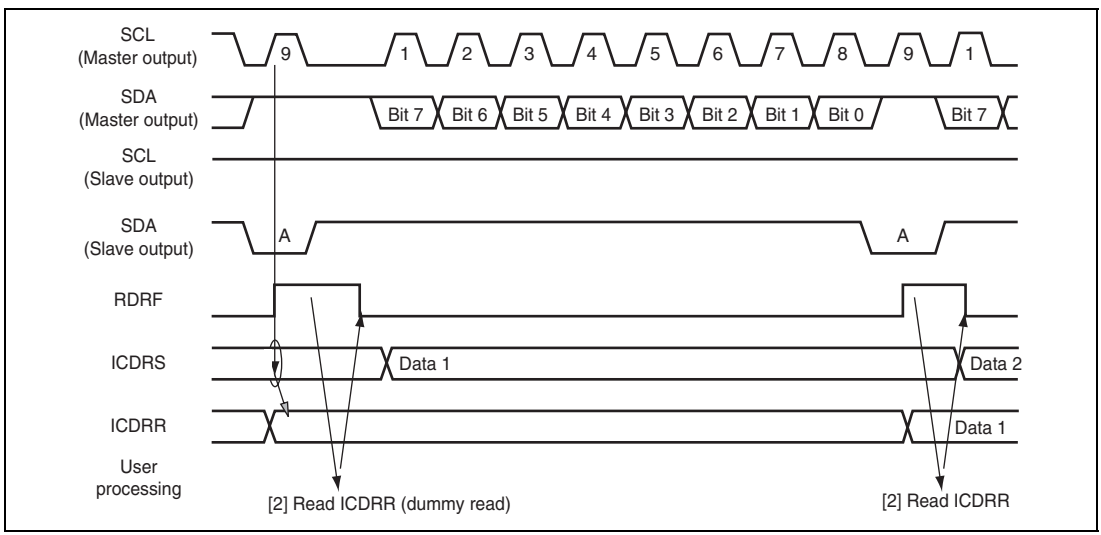
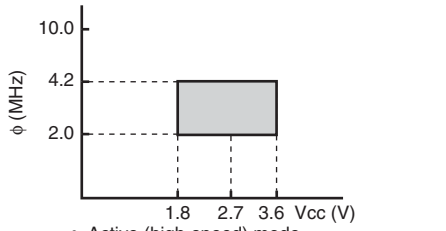


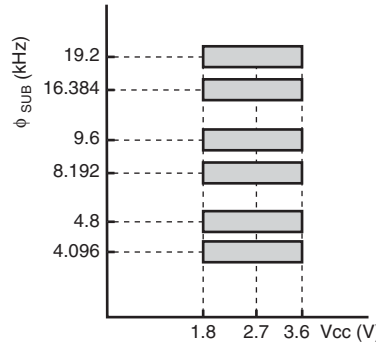
Figure 22.11 Slave Receive Mode Operation Timing (1)

Register Name	Abbre-viation	Bit No.	Address*1	Module Name	Data Bus Width	Access State
I^2C bus status register	ICSR	8	H'F07C	IIC2	8	2
Slave address register	SAR	8	H'F07D	IIC2	8	2
I^2C bus transmit data register	ICDRT	8	H'F07E	IIC2	8	2
I^2C bus receive data register	ICDRR	8	H'F07F	IIC2	8	2
Interrupt priority register A	IPRA	8	H'F080	Interrupts	8	2
Interrupt priority register B	IPRB	8	H'F081	Interrupts	8	2
Interrupt priority register C	IPRC	8	H'F082	Interrupts	8	2
Interrupt priority register D	IPRD	8	H'F083	Interrupts	8	2
Interrupt priority register E	IPRE	8	H'F084	Interrupts	8	2
Interrupt priority register F	IPRF	8	H'F085	Interrupts	8	2
Serial mode register 3_3	SMR3_3	8	H'F088	SCI3_3	8	3
Bit rate register 3_3	BRR3_3	8	H'F089	SCI3_3	8	3
Serial control register 3_3	SCR3_3	8	H'F08A	SCI3_3	8	3
Transmit data register 3_3	TDR3_3	8	H'F08B	SCI3_3	8	3
Serial status register 3_3	SSR3_3	8	H'F08C	SCI3_3	8	3
Receive data register 3_3	RDR3_3	8	H'F08D	SCI3_3	8	3
Address break control register 2	ABRKCR2	8	H'F096	Address break	8	2
Address break status register 2	ABRKSR2	8	H'F097	Address break	8	2
Break address register 2H	BAR2H	8	H'F098	Address break	8	2
Break address register 2L	BAR2L	8	H'F099	Address break	8	2
Break data register 2H	BDR2H	8	H'F09A	Address break	8	2
Break data register 2L	BDR2L	8	H'F09B	Address break	8	2
Break address register 2E	BAR2E	8	H'F09D	Address break	8	2
Timer mode register G	TMG	8	H'FF84	Timer G	8	2
Input capture register GF	ICRGF	8	H'FF85	Timer G	8	2
Input capture register GR	ICRGR	8	H'FF86	Timer G	8	2
Event counter PWM compare register	ECPWCR	16	H'FF8C	AEC*2	16	2
Event counter PWM data register	ECPWDR	16	H'FF8E	AEC*2	16	2
Wakeup edge select register	WEGR	8	H'FF90	Interrupts	8	2

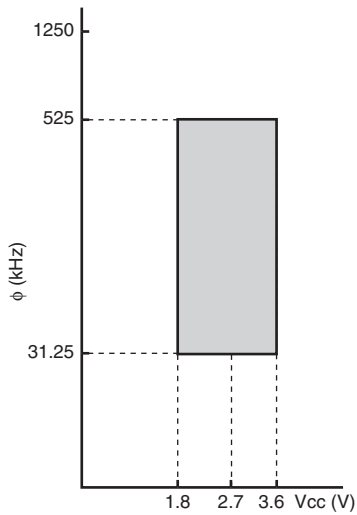
(2) System clock oscillator selected (4-MHz version)



- Active (high-speed) mode
- Sleep (high-speed) mode (other than CPU)



- Subactive mode
- Subsleep mode (other than CPU)
- Watch mode (other than CPU)



- Active (medium-speed) mode
- Sleep (medium-speed) mode (other than CPU)

Figure 26.4 Power Supply Voltage and Operating Frequency Range (2)

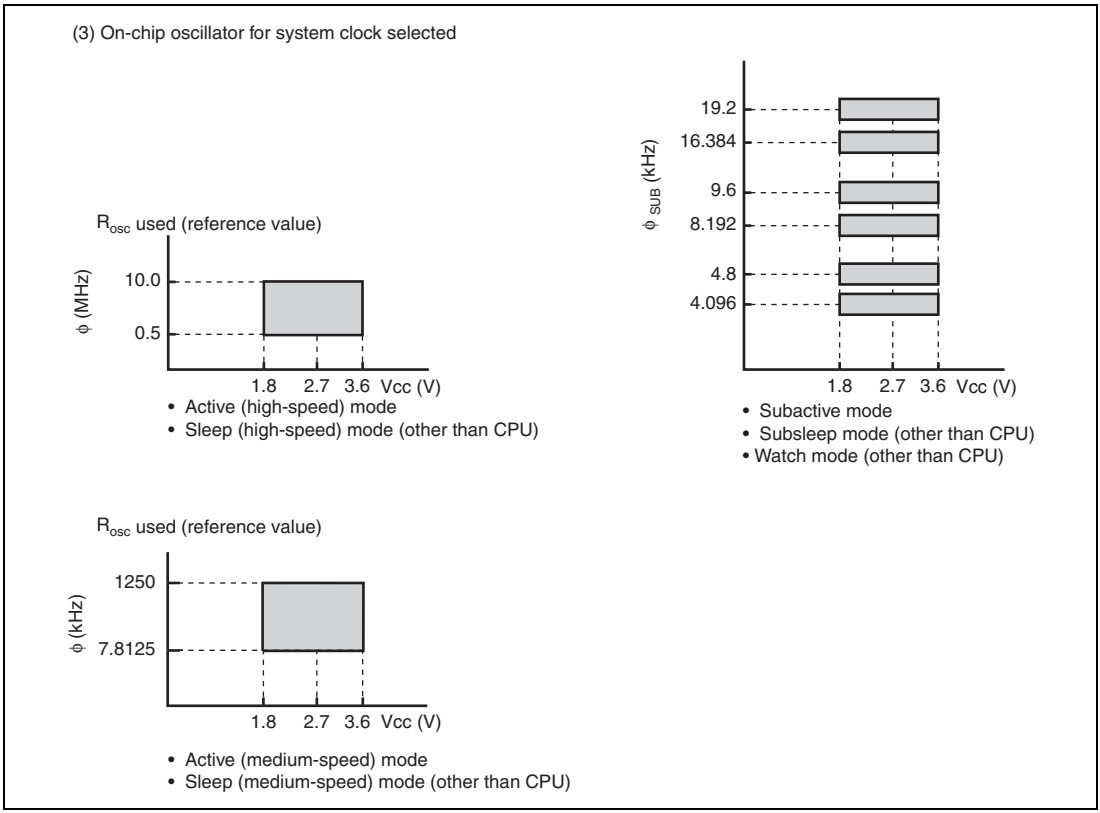


Figure 26.5 Power Supply Voltage and Operating Frequency Range (3)

26.4.3 AC Characteristics

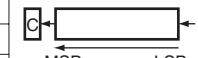
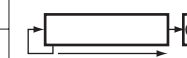
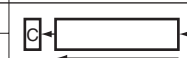
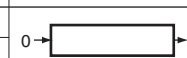
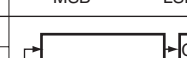
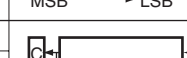
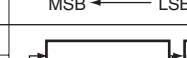
Table 26.13 lists the control signal timing, table 26.14 lists the serial interface timing, and table 26.15 lists the I^2C bus interface timing.

Table 26.13 Control Signal Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V	2.0	—	4.2		
System clock on-chip oscillation frequency	f_{Rosc}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	0.5	—	10.0		*3
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	100	—	500	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V	238	—	500		
System clock on-chip oscillation clock (ϕ_{ROSC}) cycle time	t_{ROSC}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	100	—	2000		*3
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	32	µs	

4. Shift Instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
SHAL	SHAL.B Rd	B		2									—	—	↕	↕	↕	↕	2	
	SHAL.W Rd	W		2									—	—	↕	↕	↕	↕	2	
	SHAL.L ERd	L		2									—	—	↕	↕	↕	↕	2	
SHAR	SHAR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHAR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHAR.L ERd	L		2									—	—	↕	↕	0	↕	2	
SHLL	SHLL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHLL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHLL.L ERd	L		2									—	—	↕	↕	0	↕	2	
SHLR	SHLR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHLR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHLR.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTXL	ROTXL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTXL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTXL.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTXR	ROTXR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTXR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTXR.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTL	ROTL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTL.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTR	ROTR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTR.L ERd	L		2									—	—	↕	↕	0	↕	2	

A.3 Number of Execution States

The status of execution for each instruction of the H8/300H CPU and the method of calculating the number of states required for instruction execution are shown below. Table A.4 shows the number of cycles of each type occurring in each instruction, such as instruction fetch and data read/write. Table A.3 shows the number of states required for each cycle. The total number of states required for execution of an instruction can be calculated by the following expression:

$$\text{Execution states} = I \times S_I + J \times S_J + K \times S_K + L \times S_L + M \times S_M + N \times S_N$$

Examples: When instruction is fetched from on-chip ROM, and an on-chip RAM is accessed.

BSET #0, @FF00

From table A.4:
I = L = 2, J = K = M = N= 0

From table A.3:
$S_I = 2$, $S_L = 2$

Number of states required for execution = $2 \times 2 + 2 \times 2 = 8$

When instruction is fetched from on-chip ROM, branch address is read from on-chip ROM, and on-chip RAM is used for stack area.

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From table A.4:
I = 2, J = K = 1, L = M = N = 0

From table A.3:
$S_I = S_J = S_K = 2$

Number of states required for execution = $2 \times 2 + 1 \times 2 + 1 \times 2 = 8$