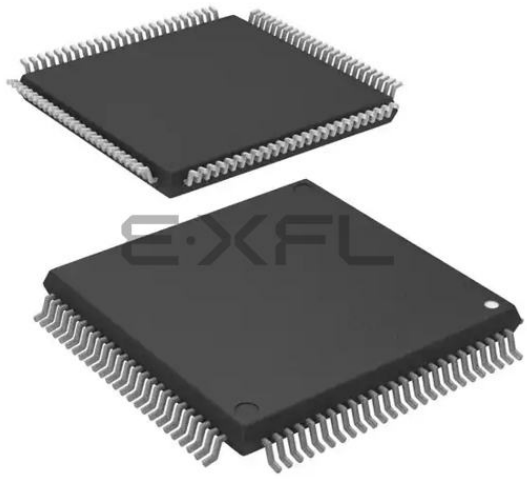

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38099fp10wv

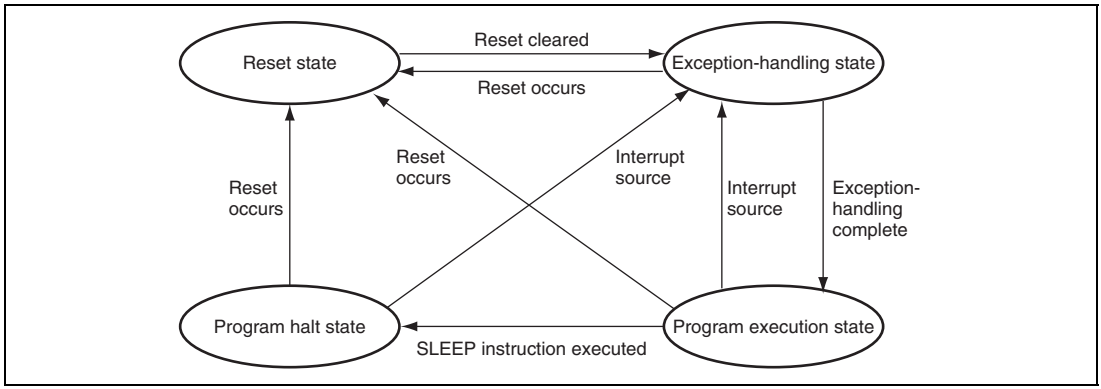


Figure 2.12 State Transitions

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4 or R4L, which starts from the address indicated by ER5, to the address indicated by ER6. Set R4 or R4L and ER6 so that the end address of the destination address (value of ER6 + R4 or ER6 + R4L) does not exceed H'00FFFFFF (the value of ER6 must not change from H'00FFFFFF to H'01000000 during execution).

Example 2: When the BSET instruction is executed for port 5

P57 and P56 are input pins, with a low-level signal input at P57 and a high-level signal input at P56. P55 to P50 are output pins and output low-level signals. An example to output a high-level signal at P50 with a BSET instruction is shown below.

- Prior to executing BSET instruction

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0

- BSET instruction executed

```
BSET    #0,    @PDR5:8
```

The BSET instruction is executed for port 5.

- After executing BSET instruction

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	1
PDR5	0	1	0	0	0	0	0	1

- Description on operation

1. When the BSET instruction is executed, first the CPU reads port 5.
   Since P57 and P56 are input pins, the CPU reads the pin states (low-level and high-level input).
   P55 to P50 are output pins, so the CPU reads the value in PDR5. In this example PDR5 has a value of H'80, but the value read by the CPU is H'40.
2. Next, the CPU sets bit 0 of the read data to 1, changing the PDR5 data to H'41.

Section 3 Exception Handling

Exception handling may be caused by a reset or interrupts.

- Reset

  A reset has the highest exception priority. Exception handling starts as soon as the reset is cleared by the $\overline{\text{RES}}$ pin. The chip is also reset when the watchdog timer overflows, and exception handling starts. Exception handling is the same as exception handling by the $\overline{\text{RES}}$ pin.

- Interrupts

  External interrupts other than NMI and internal interrupts other than address break are masked by the I bit in CCR, and kept masked while the I bit is set to 1. Exception handling starts when the current instruction or exception handling ends, if an interrupt request has been issued.

Figure 3.5 shows the procedure for setting a bit in a port mode register and clearing the interrupt request flag. This procedure also applies to AEGSR setting.

When switching a pin function, mask the interrupt before setting the bit in the port mode register (or AEGSR). After accessing the port mode register (or AEGSR), execute at least one instruction (e.g., NOP), then clear the interrupt request flag from 1 to 0. If the instruction to clear the flag to 0 is executed immediately after the port mode register (or AEGSR) access without executing an instruction, the flag will not be cleared.

An alternative method is to avoid the setting of interrupt request flags when pin functions are switched by keeping the pins at the high level so that the conditions in table 3.2 are not satisfied. However, the procedure in figure 3.5 is recommended because IECPWM is an internal signal and determining its value is complicated.

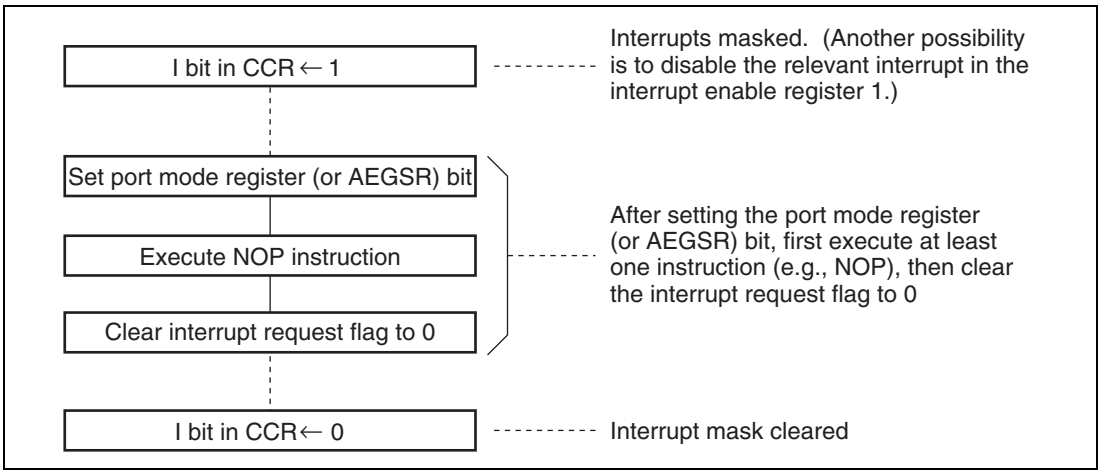


Figure 3.5 Port Mode Register (or AEGSR) Setting and Interrupt Request Flag Clearing Procedure

4.3.2 Wakeup Edge Select Register (WEGR)

WEGR selects the sense of an edge that generates interrupt requests of the $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pins.

Bit	Bit Name	Initial Value	R/W	Description
7	WKEGS7	0	R/W	WKP7 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP7}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP7}}$ pin input
6	WKEGS6	0	R/W	WKP6 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP6}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP6}}$ pin input
5	WKEGS5	0	R/W	WKP5 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP5}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP5}}$ pin input
4	WKEGS4	0	R/W	WKP4 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP4}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP4}}$ pin input
3	WKEGS3	0	R/W	WKP3 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP3}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP3}}$ pin input
2	WKEGS2	0	R/W	WKP2 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP2}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP2}}$ pin input
1	WKEGS1	0	R/W	WKP1 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP1}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP1}}$ pin input
0	WKEGS0	0	R/W	WKP0 Edge Select 0: Detects a falling edge of the $\overline{\text{WKP0}}$ pin input 1: Detects a rising edge of the $\overline{\text{WKP0}}$ pin input

4.3.8 Interrupt Priority Registers A to F (IPRA to IPRF)

IPR sets mask levels (levels 2 to 0) for interrupts other than the NMI and address break. The correspondence between interrupt sources and IPR settings is shown in table 4.2.

Setting a value in the range from H'0 to H'3 in the 2-bit groups of bits 7 and 6, 5 and 4, 3 and 2, and 1 and 0 sets the mask level of the corresponding interrupt. Bits 3 to 0 in IPRE and bits 1 and 0 in IPRF are reserved.

Bit	Bit Name	Initial Value	R/W	Description
7	IPRn7	0	R/W	Set the mask level of the corresponding interrupt source.
6	IPRn6	0	R/W	00: Mask level 0 (Lowest)
				01: Mask level 1
				1x: Mask level 2 (Highest)
5	IPRn5	0	R/W	Set the mask level of the corresponding interrupt source.
4	IPRn4	0	R/W	00: Mask level 0 (Lowest)
				01: Mask level 1
				1x: Mask level 2 (Highest)
3	IPRn3	0	R/W	Set the mask level of the corresponding interrupt source.
2	IPRn2	0	R/W	00: Mask level 0 (Lowest)
				01: Mask level 1
				1x: Mask level 2 (Highest)
1	IPRn1	0	R/W	Set the mask level of the corresponding interrupt source.
0	IPRn0	0	R/W	00: Mask level 0 (Lowest)
				01: Mask level 1
				1x: Mask level 2 (Highest)

[Legend]
x: Don't care
n = A to F

5.2.4 Selecting On-Chip Oscillator for System Clock

The on-chip oscillator is selected by the input level on the IRQAEC pin during a reset*. The selection of the system clock oscillator or on-chip oscillator for the system clock is as listed in table 5.1. The level being input on the IRQAEC pin during a reset should be fixed to either Vcc or GND, depending on the oscillator type to be selected. The level will be determined upon reset cancellation

When the on-chip oscillator for the system clock is selected, connection of a resonator to OSC1 or OSC2 is not necessary. In this case, the OSC1 pin should be fixed to Vcc or GND. The OSC2 pin should be left open.

Notes: When programming or erasing the flash memory, e.g. by on-board programming, the system clock oscillator should always be selected. Use of the on-chip emulator requires either a connected resonator or the supply of an external clock signal, even if the on-chip oscillator for the system clock is selected.

* This reset represents an external reset or power-on reset, but not a reset by the watchdog timer.

Table 5.1 Selection of the System Clock Oscillator or On-Chip Oscillator for the System Clock

IRQAEC Input Level (During a Reset)	Oscillator of System Clock Pulse Generator Circuit	OSCF	IRQAECF
Low	System clock oscillator	0	0
High	On-chip oscillator for system clock	1	1

5.4 Prescalers

This LSI has two prescalers (prescaler S and prescaler W), and each has its own input clock signal.

Prescaler S is a 17-bit counter that has the system clock (ϕ) as its input clock. Its prescaled outputs provide the internal clock signals that drive the on-chip peripheral modules.

Prescaler W is an 8-bit counter that has a frequency-divided signal ($\phi_w/4$) derived from the watch clock (ϕ_w) as its input clock. Its prescaled outputs provide the internal clock signals that drive the on-chip peripheral modules.

5.4.1 Prescaler S

Prescaler S is a 17-bit counter using the system clock (ϕ) as its input clock. A divided output is used as an internal clock of an on-chip peripheral module. Prescaler S is initialized to H'00000 at a reset, and starts counting up on exit from the reset state. Prescaler S stops and is initialized to H'00000 in standby mode, watch mode, subactive mode, and subsleep mode. The CPU cannot read from or write to prescaler S.

The output from prescaler S is shared by the on-chip peripheral modules. In active (medium-speed) mode and sleep mode (medium-speed), the clock input to prescaler S is determined by the division ratio designated by the MA1 and MA0 bits in SYSCR2.

5.4.2 Prescaler W

Prescaler W is an 8-bit counter that has a frequency-divided signal ($\phi_w/4$) derived from the watch clock (ϕ_w) as its input clock. This signal is further divided to produce internal clock signals for the on-chip peripheral modules. Prescaler W is initialized to H'00 by a reset, and starts counting up on exit from the reset state. Prescaler W stops in standby mode, but continues to operate in watch mode, subactive mode, and subsleep mode.

- CKSTPR2

Bit	Bit Name	Initial Value	R/W	Description
7	ADBCKSTP	1	R/W	Address Break Module Standby The address break enters standby mode when this bit is cleared to 0.
6	TPUCKSTP	1	R/W	TPU Module Standby The TPU enters standby mode when this bit is cleared to 0.
5	IICCKSTP	1	R/W	IIC2 Module Standby The IIC2 enters standby mode when this bit is cleared to 0.
4	PW2CKSTP	1	R/W	PWM2 Module Standby The PWM2 enters standby mode when this bit is cleared to 0.
3	AECCKSTP	1	R/W	Asynchronous Event Counter Module Standby The asynchronous event counter enters standby mode when this bit is cleared to 0.
2	WDCKSTP	1	R/W*[4]	Watchdog Timer Module Standby The watchdog timer enters standby mode when this bit is cleared to 0.
1	PW1CKSTP	1	R/W	PWM1 Module Standby The PWM1 enters standby mode when this bit is cleared to 0.
0	LDCKSTP	1	R/W	LCD Module Standby The LCD controller/driver enters standby mode when this bit is cleared to 0.

11.5 Timer C Operation States

Table 11.2 summarizes the timer C operation states.

Table 11.2 Timer C Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCC	Interval	Reset	Functioning*1	Functioning*1	Functioning/ Halted*2	Functioning/ Halted*3	Functioning/ Halted*3	Halted	Halted
	Auto reload	Reset	Functioning*1	Functioning*1	Functioning/ Halted*2	Functioning/ Halted*3	Functioning/ Halted*3	Halted	Halted
TMC		Reset	Functioning	Retained	Retained	Functioning	Retained	Retained	Retained

Notes: 1. When $\phi_w/4$, $\phi_w/256$, or $\phi_w/1024$ is selected as the TCC internal clock in active mode or sleep mode, since the system clock and internal clock are mutually asynchronous, synchronization is maintained by a synchronization circuit. This results in a maximum count cycle error of $1/\phi$ (s).

2. When the counter is operated in watch mode, select $\phi_w/4$, $\phi_w/256$, or $\phi_w/1024$ as the clock.

3. When the counter is operated in subactive mode or subsleep mode, either select $\phi_w/4$, $\phi_w/256$, or $\phi_w/1024$ as the internal clock or select an external clock. The counter will not operate on any other internal clock. If $\phi_w/4$ is selected as the internal clock for the counter when $\phi_w/8$ has been selected as subclock ϕ_{SUB}, the lower 2 bits of the counter operate on the same cycle, and the operation of the least significant bit is unrelated to the operation of the counter.

(2) Interval Timer Operation

When the TMIG bit in PMRF is cleared to 0, timer G functions as an interval timer.

Following a reset, TCG starts counting on the ϕ/64 internal clock. The input clock can be selected from four internal clock sources by bits CKS1 and CKS0 in TMG. TCG increments on the selected clock, and when it overflows from H'FF to H'00, the OVFL bit in TMG is set to 1. If the OVIE bit in TMG is 1 at this time, IRRTG in IRR2 is set to 1, and if the IENTG bit in IENR2 is 1, timer G sends an interrupt request to the CPU. For details on interrupts, see section 4, Interrupt Controller.

13.5.2 Count Timing

TCG is incremented by internal clock input. Bits CKS1 and CKS0 in TMG select one of four internal clock sources (ϕ/64, ϕ/32, ϕ/2, or ϕ_w/4) created by dividing the system clock (ϕ) or watch clock (ϕ_w).

13.5.3 Input Capture Input Timing

(1) Without Noise Cancellation Function

For input capture input, dedicated input capture functions are provided for rising and falling edges.

Figure 13.4 shows the timing for rising/falling edge input capture input.

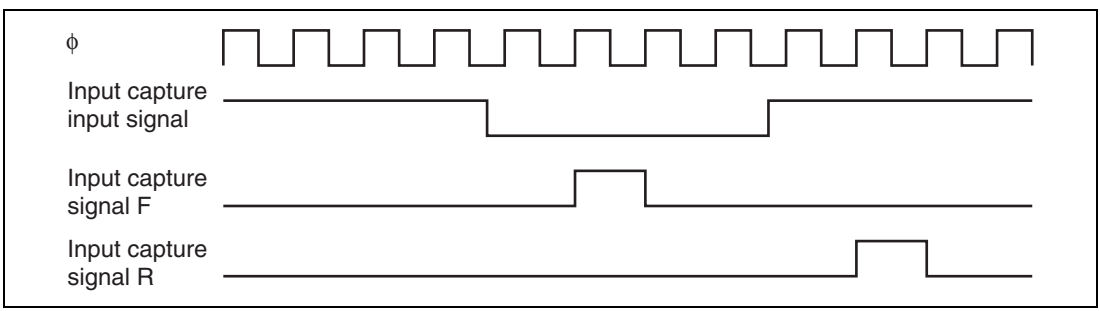


Figure 13.4 Input Capture Input Timing (without Noise Cancellation Function)

Bit	Bit Name	Initial Value	R/W	Description
5	ORER	0	R/(W)*	Overrun Error Indicates that an overrun error occurs during reception and then abnormal termination occurs. In transfer mode, the output level of the SO4 pin is fixed to low while this flag is set to 1. When the RE bit in SCR4 is cleared to 0, the ORER flag is not affected and retains its previous state. When RDR4 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the ORER flag set to 1, and transmission cannot be continued either. [Setting condition] • Next serial reception is completed while RDRF = 1 [Clearing condition] • Writing of 0 to bit ORER after reading ORER = 1
4	TEND	0	R/(W)*	Transmit End Indicates that the TDRE flag has been set to 1 at transmission of the last bit of transmit data. [Setting condition] • TDRE = 1 at transmission of the last bit of transmit data [Clearing conditions] • Writing of 0 to bit to TEND after reading TEND = 1 • Data is written to TDR4 with an instruction
3	CKS3	1	R/W	Clock Source Select and Pin Function Select the clock source to be supplied and set the input/output for the SCK4 pin. The prescaler division ratio and transfer clock cycle when an internal clock is selected are shown in table 18.2. When an external clock is selected, the external clock cycle should be at least 4/ϕ.
2	CKS2	0	R/W	
1	CKS1	0	R/W	
0	CKS0	0	R/W	

Note: * Only 0 can be written to clear the flag.

18.4.3 Data Transmission/Reception

Before data transmission and reception, clear the TE and RE bits in SCR4 to 0 and then initialize as the following procedure of figure 18.3.

Note: Before changing operating modes or communication format, the TE and RE bits must be cleared to 0. Clearing the TE bit to 0 sets the TDRE flag to 1. Note that clearing the RE bit to 0 does not affect the RDRF or ORER flag and the contents of RDR4.
When the external clock is used, the clock must not be supplied during operation including initialization.

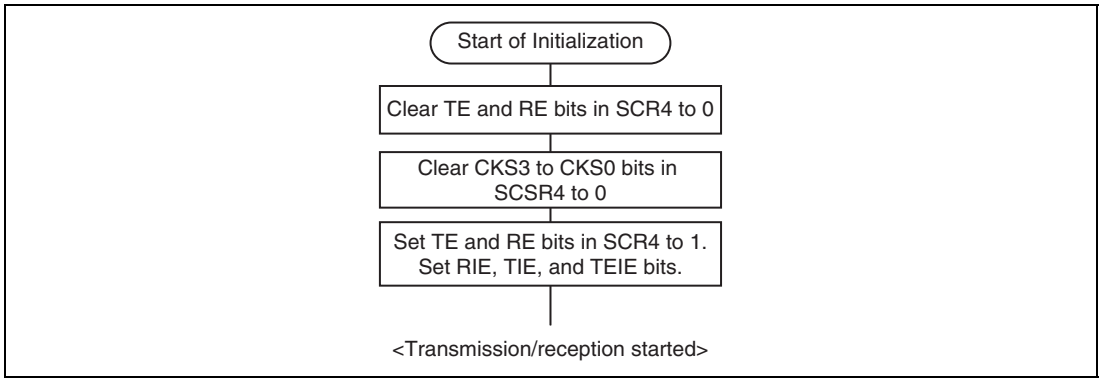


Figure 18.3 Flowchart Example of SCI4 Initialization

21.4.2 Relationship between LCD RAM and Display

The relationship between the LCD RAM and the display segments differs according to the duty cycle. LCD RAM maps for the different duty cycles are shown in figures 21.3 to 21.6.

After setting the registers required for display, data is written to the part corresponding to the duty using the same kind of instruction as for ordinary RAM, and display is started automatically when turned on. Word- or byte-access instructions can be used for RAM setting.

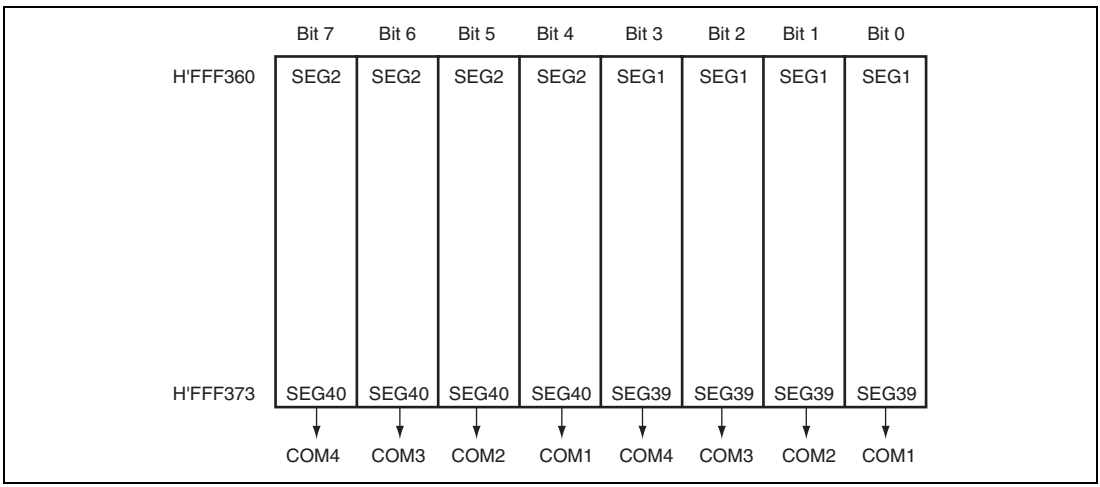


Figure 21.3 LCD RAM Map (1/4 Duty)

Figure 21.7 shows output waveforms for each duty cycle (A waveform).

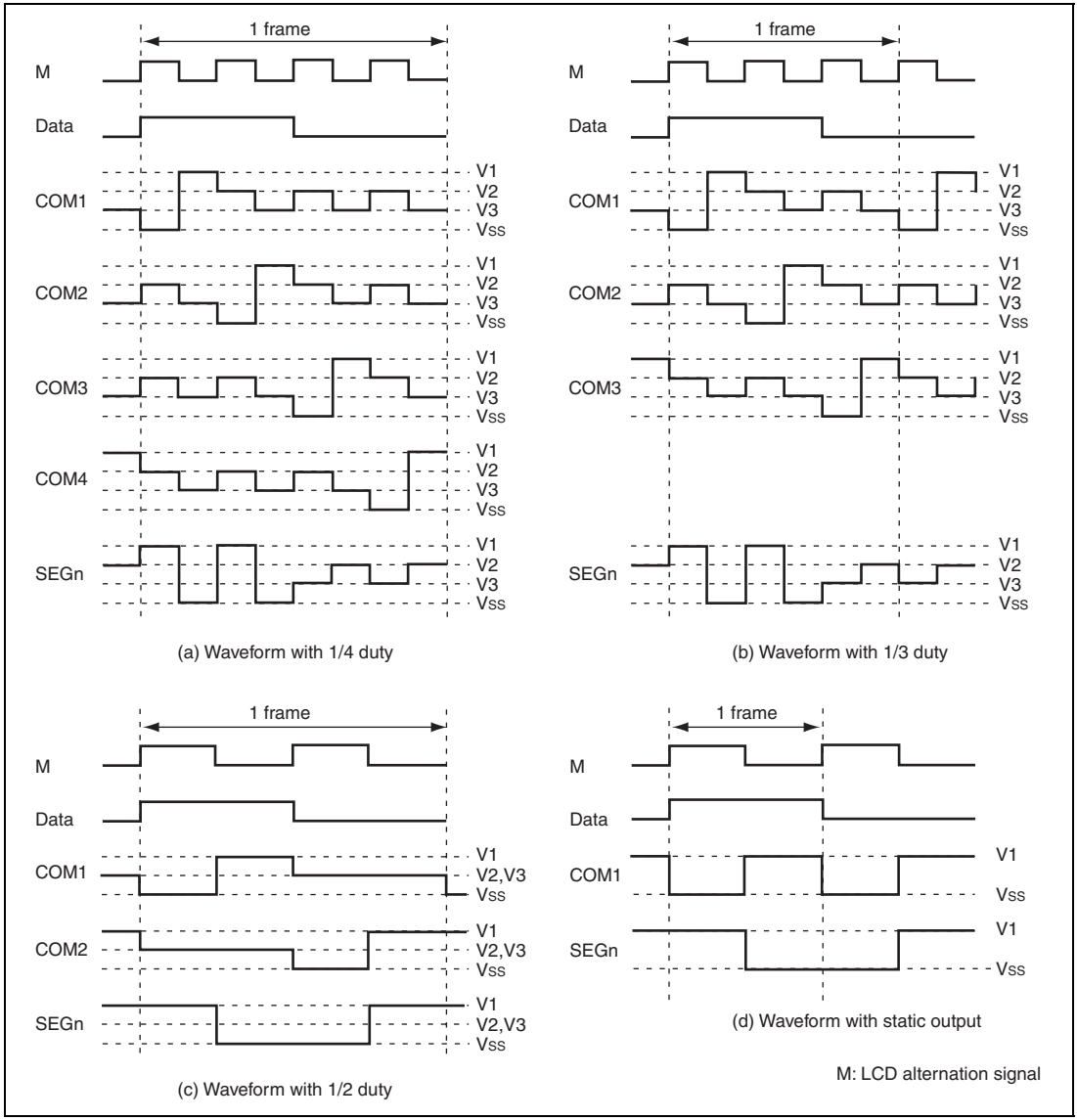


Figure 21.7 Output Waveforms for Each Duty Cycle (A Waveform)

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA	
		P90 to P93		—	—	15.0		
Allowable output low current (total)	ΣI_{OL}	Output pins except port 9		—	—	20.0	mA	
		Port 9		—	—	60.0		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	Vcc = 2.7 to 3.6 V	—	—	2.0	mA	
			Vcc = 1.8 to 3.6 V	—	—	0.2		
Allowable output high current (total)	$\Sigma - I_{OH}$	All output pins		—	—	10.0	mA	

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates On-chip WDT oscillator is off	V_{CC}	System clock oscillator: crystal resonator Subclock oscillator: Pin X1 = GND
Active (medium-speed) mode (I_{OPE2})				
Sleep mode	V_{CC}	Only on-chip timers operate On-chip WDT oscillator is off	V_{CC}	
Subactive mode	V_{CC}	Only CPU operates On-chip WDT oscillator is off	V_{CC}	System clock oscillator: crystal resonator Subclock oscillator: crystal resonator
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops On-chip WDT oscillator is off	V_{CC}	
Watch mode	V_{CC}	Only time base operates, CPU stops On-chip WDT oscillator is off	V_{CC}	
Standby mode	V_{CC}	CPU and timers both stop On-chip WDT oscillator is off 32KSTOP = 1	V_{CC}	System clock oscillator: crystal resonator Subclock oscillator: crystal resonator

Item	Symbol	Applicable Pins	Test Condition	Values Min.			Unit	Note
Input/output leakage current	$\lvert I_{IL} \rvert$	TEST, $\overline{NMI}$, OSC1, X1, P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, IRQAEC, PA0 to PA3, PC0 to PC7, PE0 to PE7, PF0 to PF3, P90 to P93	V_{IN} = 0.5 V to V_{CC} – 0.5 V	—	—	1.0	µA	
		PB0 to PB7	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	—	—	1.0		
Pull-up MOS current	$-I_p$	P10 to P16, P30, P36, P37, P50 to P57, P60 to P67	V_{CC} = 3 V, V_{IN} = 0 V	30	—	180	µA	
Input capacitance	C_{IN}	All input pins except power supply pin	f = 1 MHz, V_{IN} = 0 V, Ta = 25°C	—	—	15.0	pF	

Item	Symbol	Applicable Pins	Test Condition	Values Min.			Unit	Note
Subactive mode supply current	I_{SUB}	V_{CC}	V_{CC} = 1.8 V, LCD lighting, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$)	—	6.5	—	µA	Reference value *1 *2
			V_{CC} = 2.7 V, LCD lighting, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/8$)	—	5.5	—		Reference value *1 *2
			V_{CC} = 2.7 V, LCD lighting, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$)	—	11	17		*1 *2
Subsleep mode supply current	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, LCD lighting, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	5.0	8.5	µA	*1 *2
Watch mode supply current	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C 32-kHz crystal resonator used, LCD not used	—	0.5	—	µA	*1 *2
			V_{CC} = 2.7 V, 32-kHz crystal resonator used, LCD not used	—	1.5	5.0		Reference value *1 *2
Standby mode supply current	I_{STBY}	V_{CC}	V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.1	—	µA	Reference value *1 *2
			32-kHz crystal resonator not used	—	1.0	5.0		*1 *2

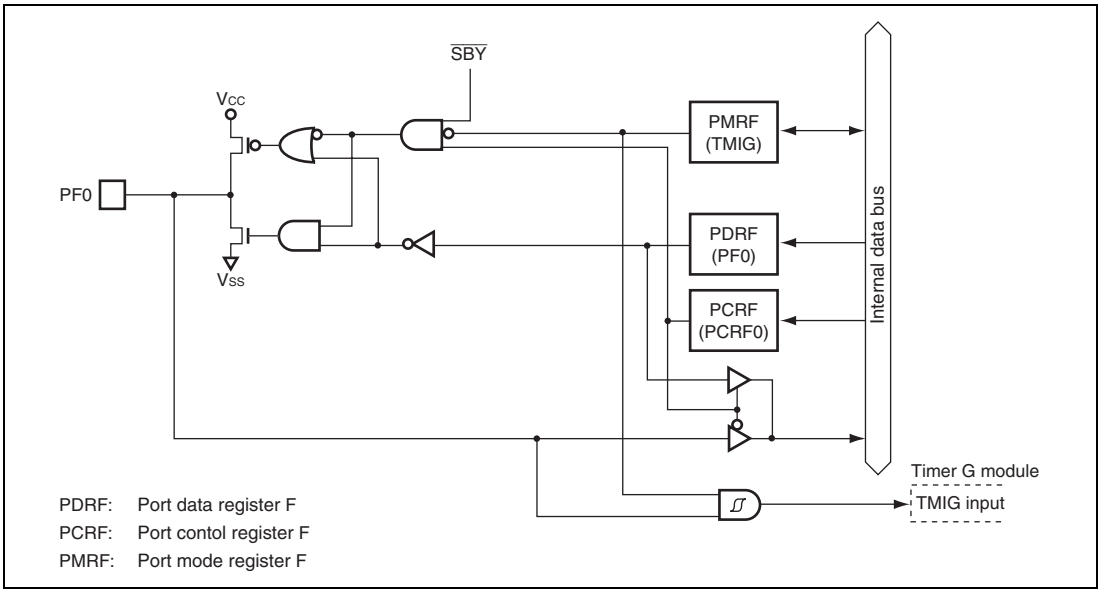
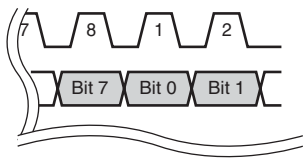
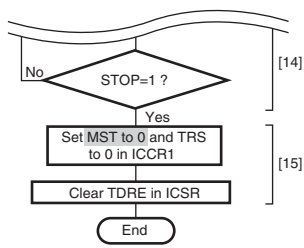


Figure B.13 (d) Port F Block Diagram (PF0)

Item	Page	Revisions (See Manual for Details)
21.4.3 3-V Constant-Voltage Power Supply Circuit	473	Modified … Before activating a step-up circuit, operate the LCD controller/driver, and set the duty cycle, pin function, display data, frame frequencies, etc. Insert a capacitance of 0.1 μF between the C1 pin and C2 pin, and connect a capacitance of 0.1 μF to each of V1, V2, and V3 pins.
	474	Modified Notes: : 4. The step-up circuit output voltage in the initial state is different in an individual device according to the manufacturing difference.
21.5 Usage Notes	477	Added
Section 22 I^2C Bus Interface 2 (IIC2) Figure 22.15 Receive Mode Operation Timing	506	Modified 
Figure 22.17 Sample Flowchart for Master Transmit Mode	508	Modified 
22.7.3 Restriction on Transfer Rate Setting in Multimaster Operation	514	Added
22.7.4 Restriction on the Use of Bit Manipulation Instructions for MST and TRS Setting in Multimaster Operation	515	Added
22.7.5 Usage Note on Master Receive Mode	515	Added