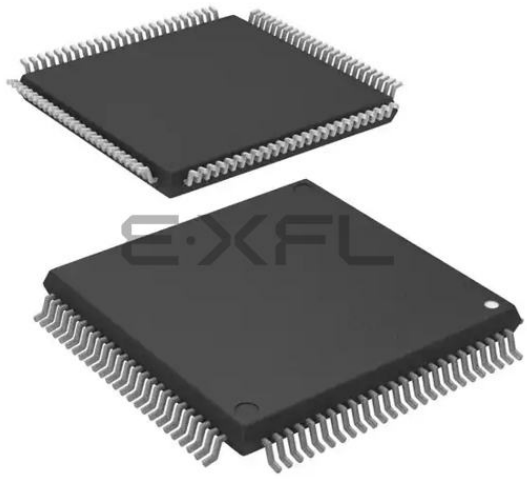

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38099fp4v

Figures

Type	Symbol	Pin No.	I/O	Functions
A/D converter	AN0 to AN7	74 to 67	Input	Analog data input pins for the A/D converter.
	$\overline{\text{ADTRG}}$	65	Input	External trigger input pin for the A/D converter.
I^2C bus interface 2 (IIC2)	SDA	95	I/O	IIC data I/O pin.
	SCL	94	I/O	IIC clock I/O pin.
LCD controller/ driver	COM1 to COM4	41 to 44	Output	LCD common output pins.
	SEG1 to SEG8	1 to 8	Output	LCD segment output pins.
	SEG9 to SEG16	9 to 16	Output	
	SEG17 to SEG24	17 to 24	Output	
	SEG25 to SEG32	25 to 32	Output	
	SEG33 to SEG40	33 to 40	Output	
I/O ports	P10 to P16	77 to 82, 91	I/O	7-bit I/O pins. Input or output can be designated for each bit by means of the port control register 1 (PCR1).
	P30 to P32, P36, P37	96 to 92	I/O	5-bit I/O pins. Input or output can be designated for each bit by means of the port control register 3 (PCR3).
	P40 to P42	50 to 52	I/O	3-bit I/O pins. Input or output can be designated for each bit by means of the port control register 4 (PCR4).
	P50 to P57	1 to 8	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 5 (PCR5).
	P60 to P67	9 to 16	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 6 (PCR6).

4.3.5 Interrupt Request Register 1 (IRR1)

IRR1 indicates the IRQ0, IRQ1, IRQ3, IRQ4, and IRQAEC interrupt request status.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
4	IRRI4	0	R/W	IRQ4 Interrupt Request Flag [Setting condition] The IRQ4 pin is set as the interrupt input pin and the specified edge is detected [Clearing condition] Writing of 0 to this bit
3	IRRI3	0	R/W	IRQ3 Interrupt Request Flag [Setting condition] The IRQ3 pin is set as the interrupt input pin and the specified edge is detected [Clearing condition] Writing of 0 to this bit
2	IRREC2	0	R/W	IRQAEC Interrupt Request Flag [Setting condition] The IRQAEC pin is set as the interrupt input pin and the specified edge is detected [Clearing condition] Writing of 0 to this bit
1	IRRI1	0	R/W	IRQ1 Interrupt Request Flag [Setting condition] The IRQ1 pin is set as the interrupt input pin and the specified edge is detected [Clearing condition] Writing of 0 to this bit

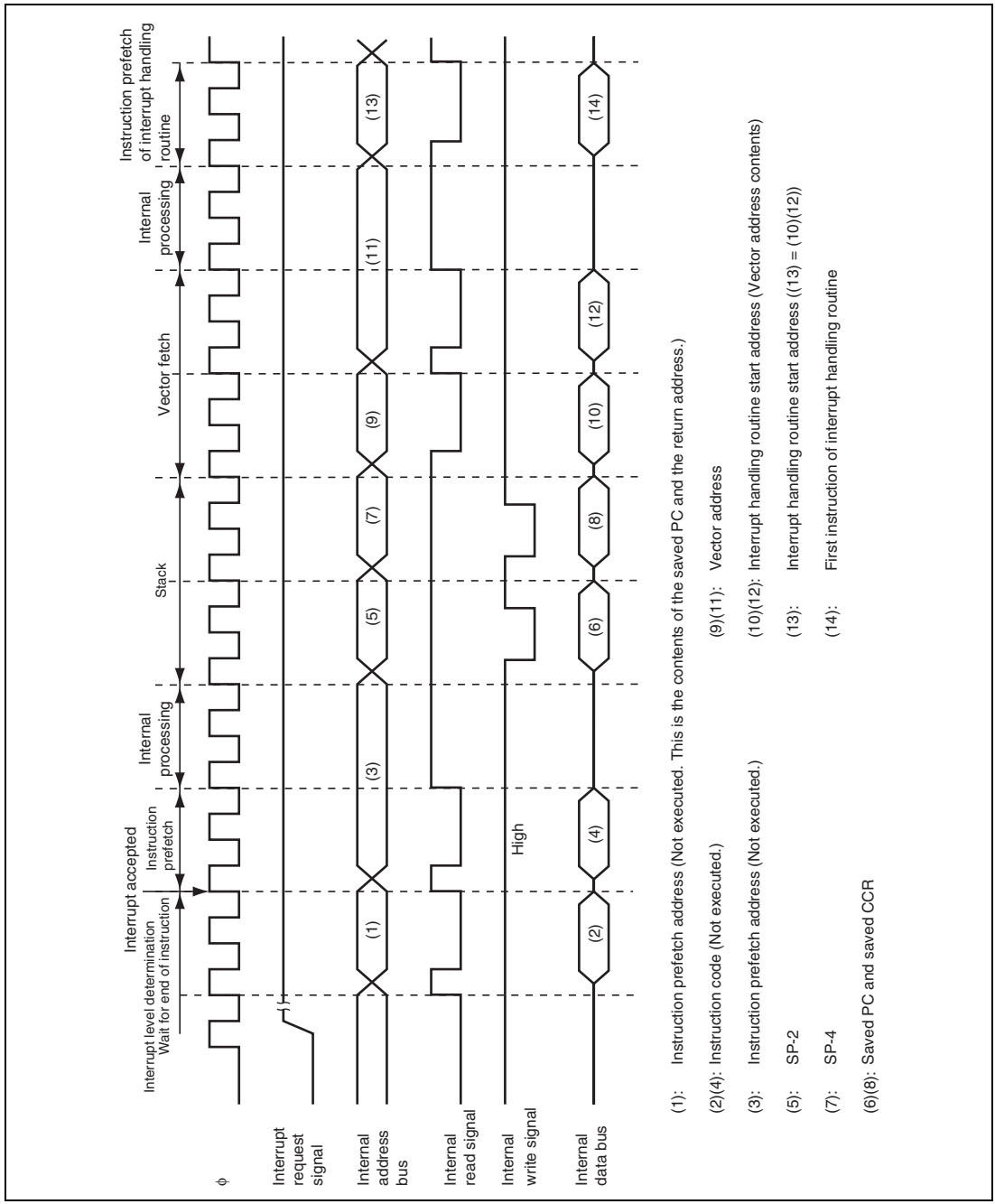


Figure 4.3 Interrupt Exception Handling Sequence

6.3.7 Notes on External Input Signal Changes before/after Direct Transition

(1) Direct transition from active (high-speed) mode to subactive mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on External Input Signal Changes before/after Standby Mode.

(2) Direct transition from active (medium-speed) mode to subactive mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on External Input Signal Changes before/after Standby Mode.

(3) Direct transition from subactive mode to active (high-speed) mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on External Input Signal Changes before/after Standby Mode.

(4) Direct transition from subactive mode to active (medium-speed) mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on External Input Signal Changes before/after Standby Mode.

6.4 Module Standby Function

The module-standby function can be set to any peripheral module. In module standby mode, the clock supply to modules stops to enter the power-down mode. Module standby mode enables each on-chip peripheral module to enter the standby state by clearing a bit that corresponds to each module in CKSTPR1 to CKSTPR3 and cancels the mode by setting the bit to 1 (see section 6.1.4, Clock Halt Registers 1 to 3 (CKSTPR1 to CKSTPR3)).

9.6 Port 7

Port 7 is an I/O pins; its pins can also be configured to function as LCD segment output pins. Figure 9.6 shows the pin configuration.

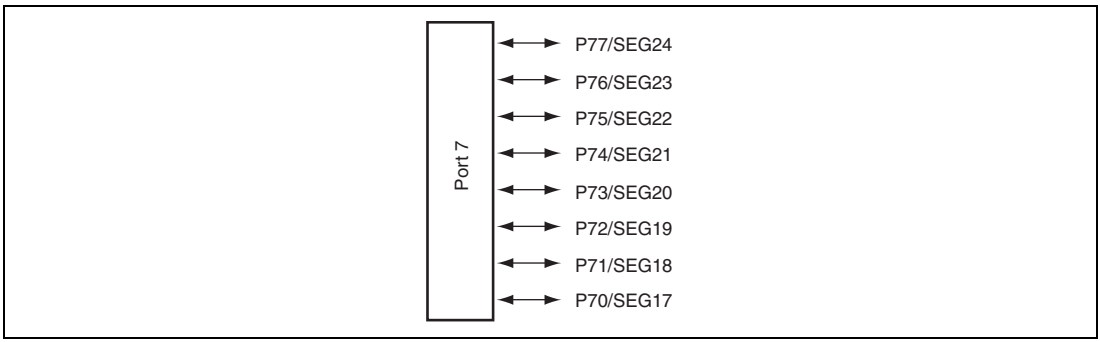


Figure 9.6 Port 7 Pin Configuration

Port 7 has the following registers.

- Port data register 7 (PDR7)
- Port control register 7 (PCR7)

9.6.1 Port Data Register 7 (PDR7)

PDR7 is a register that stores data of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	P77	0	R/W	If port 7 is read while PCR7 bits are set to 1, the values stored in PDR7 are read, regardless of the actual pin states. If port 7 is read while PCR7 bits are cleared to 0, the pin states are read.
6	P76	0	R/W	
5	P75	0	R/W	
4	P74	0	R/W	
3	P73	0	R/W	
2	P72	0	R/W	
1	P71	0	R/W	
0	P70	0	R/W	

10.3.1 Second Data Register/Free Running Counter Data Register (RSECDR)

RSECDR counts the BCD-coded second value. The setting range is decimal 00 to 59. It is an 8-bit read register used as a counter, when it operates as a free running counter. For more information on reading seconds, minutes, hours, and day-of-week, see section 10.4.3, Data Reading Procedure.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—/(0)*	R	RTC Busy This bit is set to 1 when the RTC is updating (operating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.
6	SC12	—/(0)*	R/W	Counting Ten's Position of Seconds
5	SC11	—/(0)*	R/W	Counts on 0 to 5 for 60-second counting.
4	SC10	—/(0)*	R/W	
3	SC03	—/(0)*	R/W	Counting One's Position of Seconds
2	SC02	—/(0)*	R/W	Counts on 0 to 9 once per second. When a carry is generated, 1 is added to the ten's position.
1	SC01	—/(0)*	R/W	
0	SC00	—/(0)*	R/W	

Note: * This is the initial value after a reset by the RST bit in RTCCR1.

14.5.3 Operation with Cascaded Connection

Operation as a 32-bit counter can be performed by cascading two 16-bit counter channels.

This function is enabled when the TPSC2 to TPSC0 bits in TCR are set to count on TCNT2 overflow for the channel 1 counter clock.

Table 14.11 shows the counter combination used in operation with the cascaded connection.

Table 14.11 Counter Combination in Operation with Cascaded Connection

Combination	Upper 16 bits	Lower 16 bits
Channel 1 and channel 2	TCNT1	TCNT2

(1) Setting Procedure for Operation with Cascaded Connection

Figure 14.15 shows the setting procedure for cascaded connection operation.

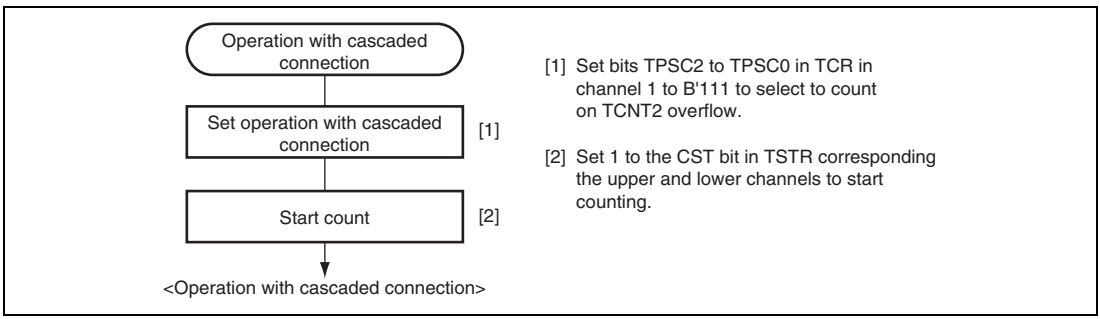


Figure 14.15 Setting Procedure for Operation with Cascaded Operation

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	—	All 1	—	Reserved These bits are always read as 1.

Notes: 1. Only 0 can be written to clear the flag.
2. Write operation is necessary because this bit controls data writing to other bit. This bit is always read as 1.
3. Writing is possible only when the write conditions are satisfied.

16.2.3 Timer Counter WD (TCWD)

TCWD is an 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00, the internal reset signal is generated and the WRST bit in TCSRWD1 is set to 1. TCWD is initialized to H'00.

16.4 Interrupt

During interval timer mode operation, an overflow generates an interval timer interrupt. The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSRWD2. The OVF flag must be cleared to 0 in the interrupt handling routine.

16.5 Usage Notes

16.5.1 Switching between Watchdog Timer Mode and Interval Timer Mode

If modes are switched between watchdog timer and interval timer, while the WDT is operating, an error may occur in the count value. Software must stop the watchdog timer (by clearing the WDON bit to 0) before switching modes.

16.5.2 Module Standby Mode Control

The WDCKSTP bit in CKSTPR2 is valid when the WDON bit in the timer control/status register WD1 (TCSRWD1) is cleared to 0. The WDCKSTP bit can be cleared to 0 while the WDON bit is set to 1 (while the watchdog timer is operating). However, the watchdog timer does not enter module standby mode but continues operating. When the WDON bit is cleared to 0 by software after the watchdog timer stops operating, the WDCKSTP bit is valid at the same time and the watchdog timer enters module standby mode.

16.5.3 Writing to Timer Counter WD (TCWD) with the On-Chip Watchdog Timer Oscillator Selected

When the timer counter WD (TCWD) is written to with the on-chip watchdog timer oscillator selected as the clock to drive the counter, updating of values read from TCWD requires up to (on-chip watchdog timer oscillator overflow time)/256. The watchdog timer does not overflow between writing of the new value to the register and updating of the read values.

17.4 Operation in Asynchronous Mode

Figure 17.2 shows the general format for asynchronous serial communication. Each frame consists of a start bit (low level), followed by data (in LSB-first order), a parity bit (high or low level), and finally stop bits (high level). In reception in asynchronous mode, synchronization is with falling edges of the start bits. The data is sampled on the 8th pulse of a clock signal with a frequency 16 times the bit rate, so that the transferred data is latched at the center of each bit. When the ABCS bit in SEMR is set to 1, data is sampled on the 4th pulse of a clock with a frequency 8 times the bit rate*. Internally, the SCI3 has independent transmitter and receiver units, which enables full duplex operation. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer. Table 17.9 shows the 16 data transfer formats that can be set in asynchronous mode. The format is selected by the settings in SMR as shown in table 17.10.

Note: Only supported by the SCI3_1 interface.

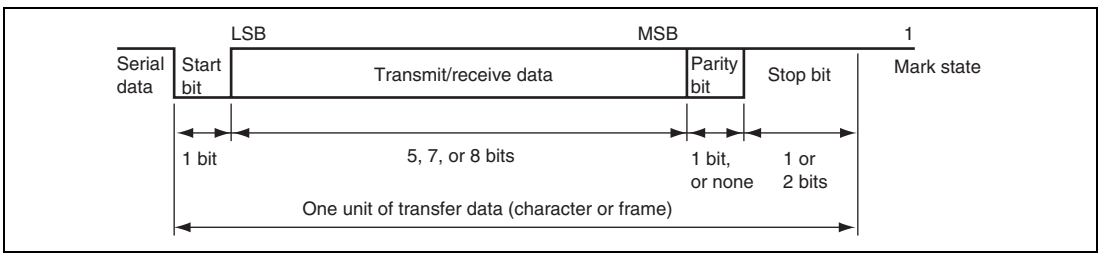


Figure 17.2 Data Format in Asynchronous Communication

17.7.1 Transmission

During transmission, the output signals from the SCI (UART frames) are converted to IR frames using the IrDA interface (see figure 17.20).

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in IrCR.

According to the standard, the high-level pulse width is defined to be 1.41 μs at minimum and (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 μs at maximum. For example, when the frequency of system clock ϕ is 10 MHz, being equal to or greater than 1.41 μs, the high-level pulse width at minimum can be specified as 1.6 μs.

For serial data of level 1, no pulses are output.

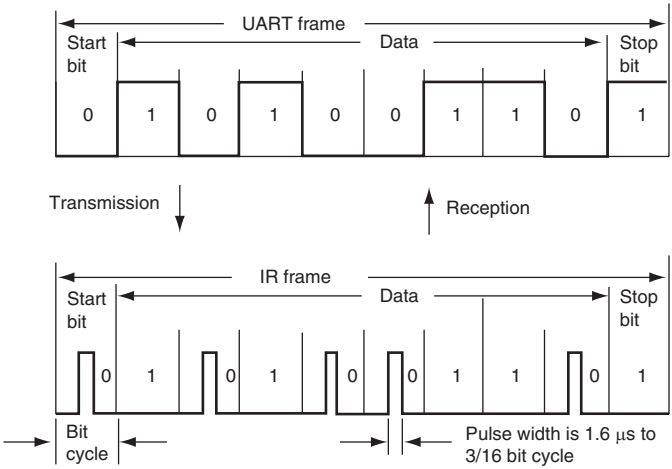


Figure 17.20 IrDA Transmission and Reception

20.6 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 20.6).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (see figure 20.7).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (see figure 20.7).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristics between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error.
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

23.2 Operation

23.2.1 Power-On Reset Circuit

The operation timing of the power-on reset circuit is shown in figure 23.2. As the power supply voltage rises, the capacitor, which is externally connected to the $\overline{RES}$ pin, is gradually charged through the on-chip pull-up resistor (Rp). The low level of the $\overline{RES}$ pin is sent to the LSI and the whole LSI is reset. When the level of the $\overline{RES}$ pin reaches to the predetermined level, a voltage detection circuit detects it. Then a 3-bit counter starts counting up. When the 3-bit counter counts ϕ for 8 times, an overflow signal is generated and an internal reset signal is negated.

The capacitance ($C_{\overline{RES}}$) which is connected to the $\overline{RES}$ pin can be computed using the following formula; where the $\overline{RES}$ rising time is t. For the on-chip resistor (Rp), see section 26, Electrical Characteristics. The power supply rising time (t_vtr) should be shorter than half the $\overline{RES}$ rising time (t). The $\overline{RES}$ rising time (t) is also should be longer than the oscillation stabilization time (trc).

$$C_{\overline{RES}} = \frac{t}{Rp} \quad (t > trc,\ t > t\_vtr \times 2)$$

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after charge on the $\overline{RES}$ pin is removed. To remove charge on the $\overline{RES}$ pin, it is recommended that the diode should be placed near Vcc. If the power supply voltage (Vcc) rises from the point above Vpor, a power-on reset may not occur.

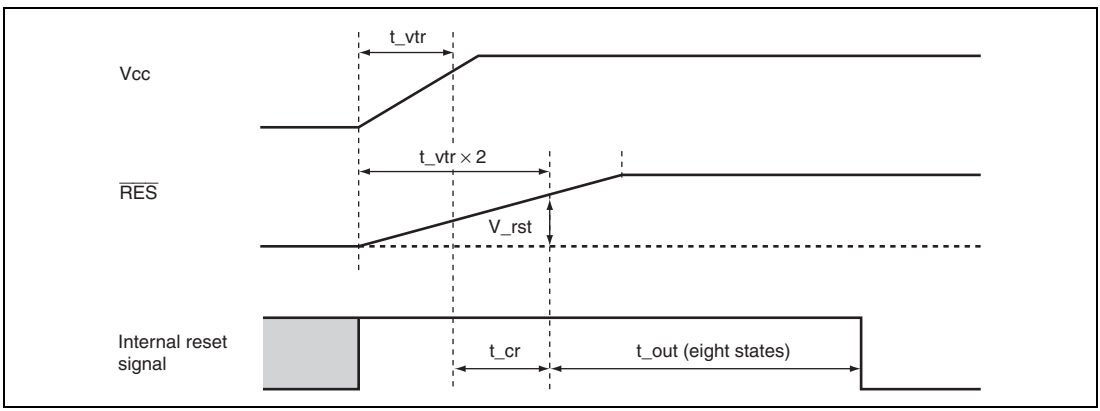


Figure 23.2 Power-On Reset Circuit Operation Timing

Item	Symbol	Applicable Pins	Test Condition	Values Min.			Unit	Note
Active mode supply current	I_{OPE1}	V_{CC}	Active (high-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.7	—	mA	Max. guideline = 1.1 × typ.*1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = R_{OSC}	—	2.2	—		Max. guideline = 1.1 × typ.*1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	2.6	—		Max. guideline = 1.1 × typ.*1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	6.0	9.0		*1 *2
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.1	—	mA	Max. guideline = 1.1 × typ.*1 *2
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.4	—		Max. guideline = 1.1 × typ.*1 *2
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	0.6	0.8		*1 *2
Sleep mode supply current	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.3	—	mA	Max. guideline = 1.1 × typ.*1 *2
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	1.2	—		Max. guideline = 1.1 × typ.*1 *2
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	2.5	4.0		*1 *2

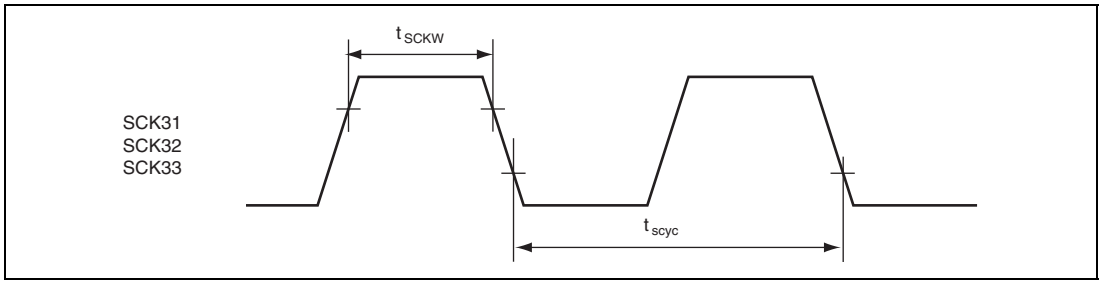
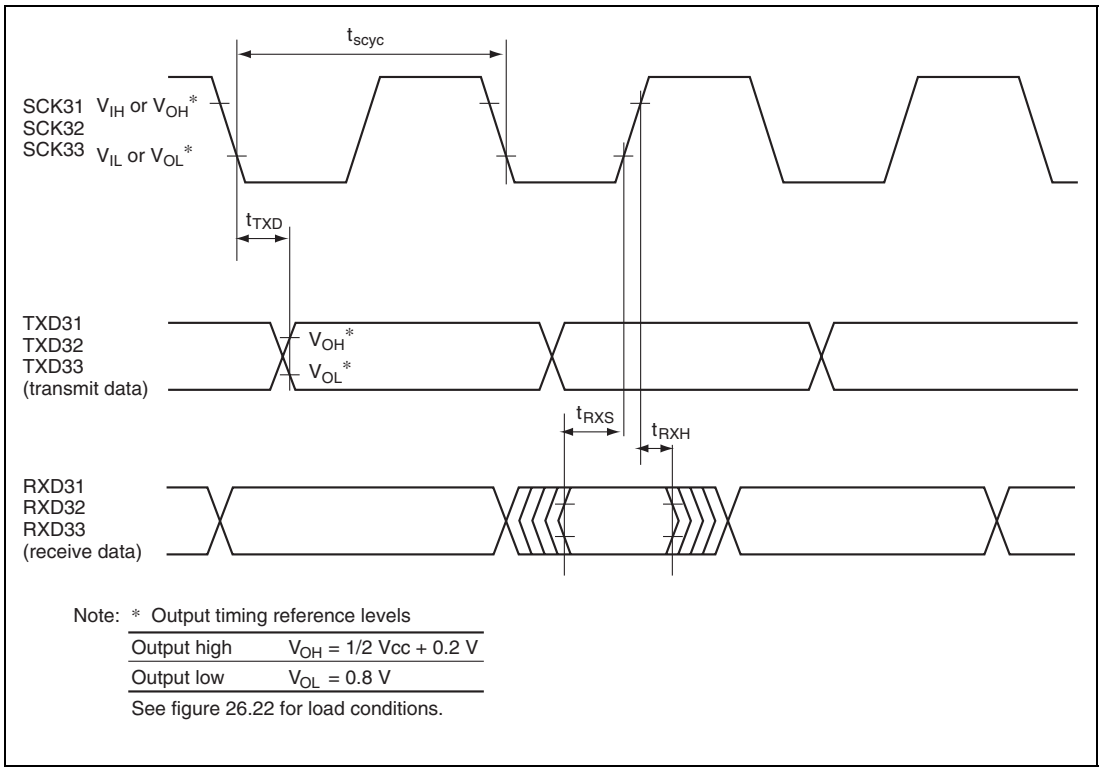


Figure 26.17 SCK3 Input Clock Timing



Note: * Output timing reference levels

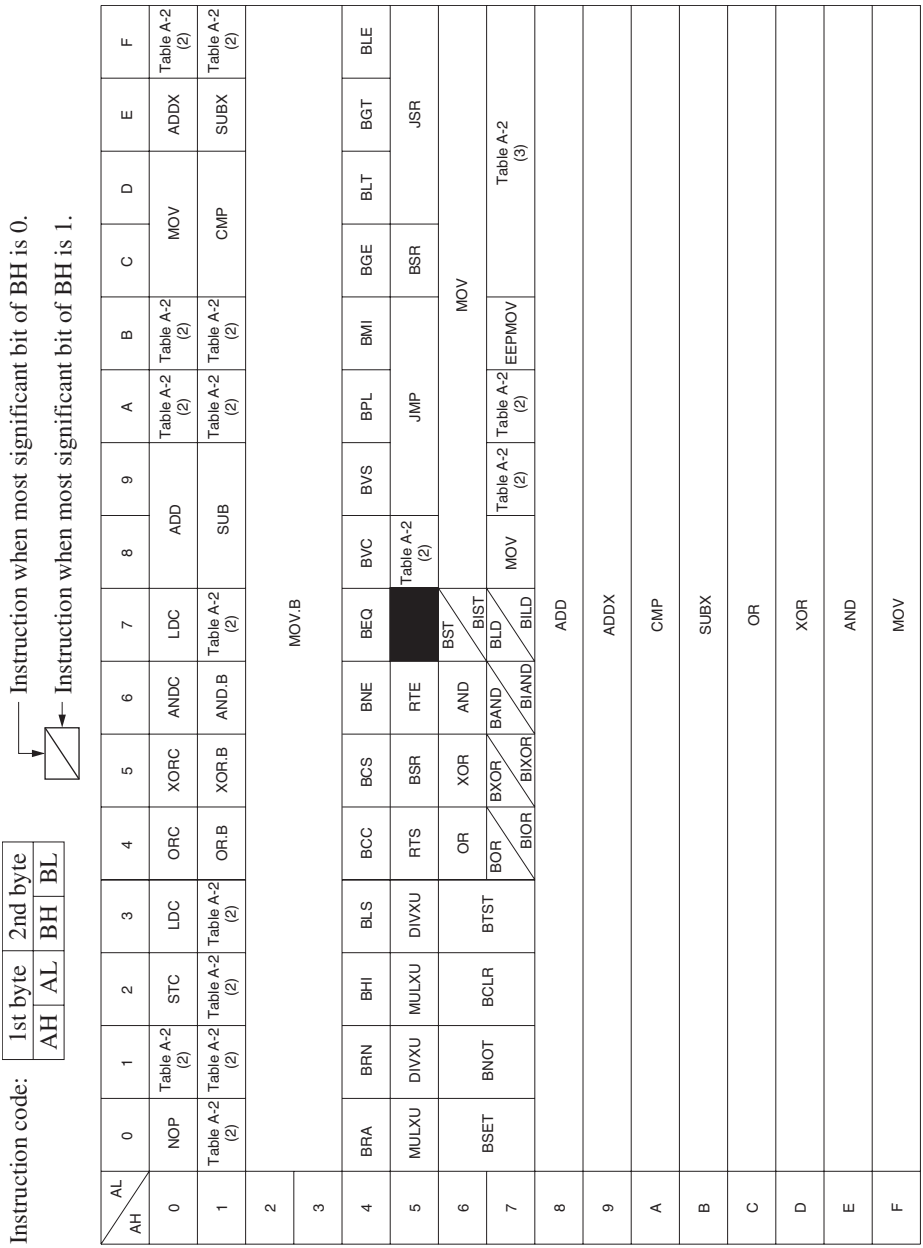
Output high	V_{OH} = 1/2 Vcc + 0.2 V
Output low	V_{OL} = 0.8 V

See figure 26.22 for load conditions.

Figure 26.18 SCI3 Input/Output Timing in Clock Synchronous Mode

A.2 Operation Code Map

Table A.2 Operation Code Map (1)



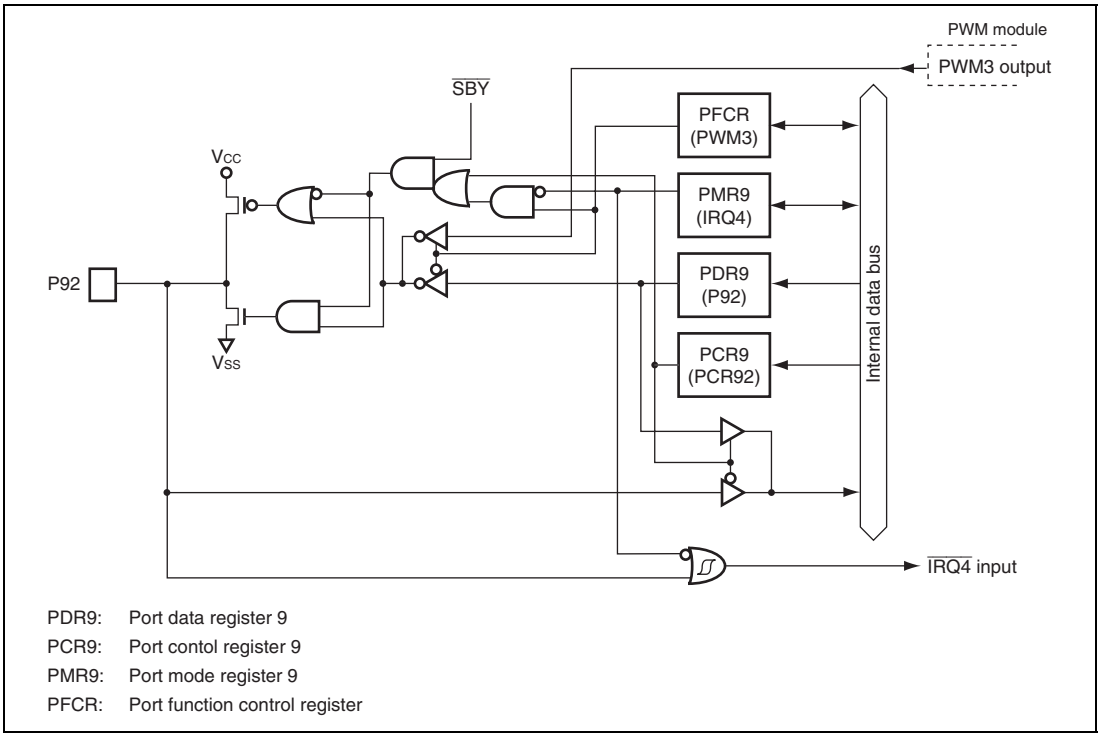


Figure B.8 (b) Port 9 Block Diagram (P92)

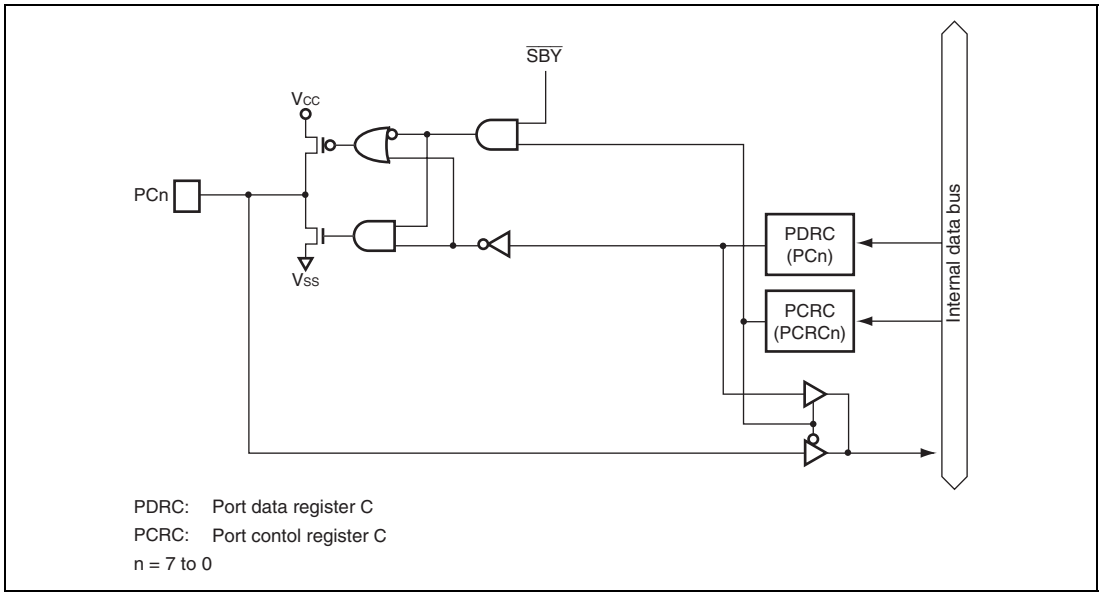


Figure B.11 Port C Block Diagram (PC7 to PC0)

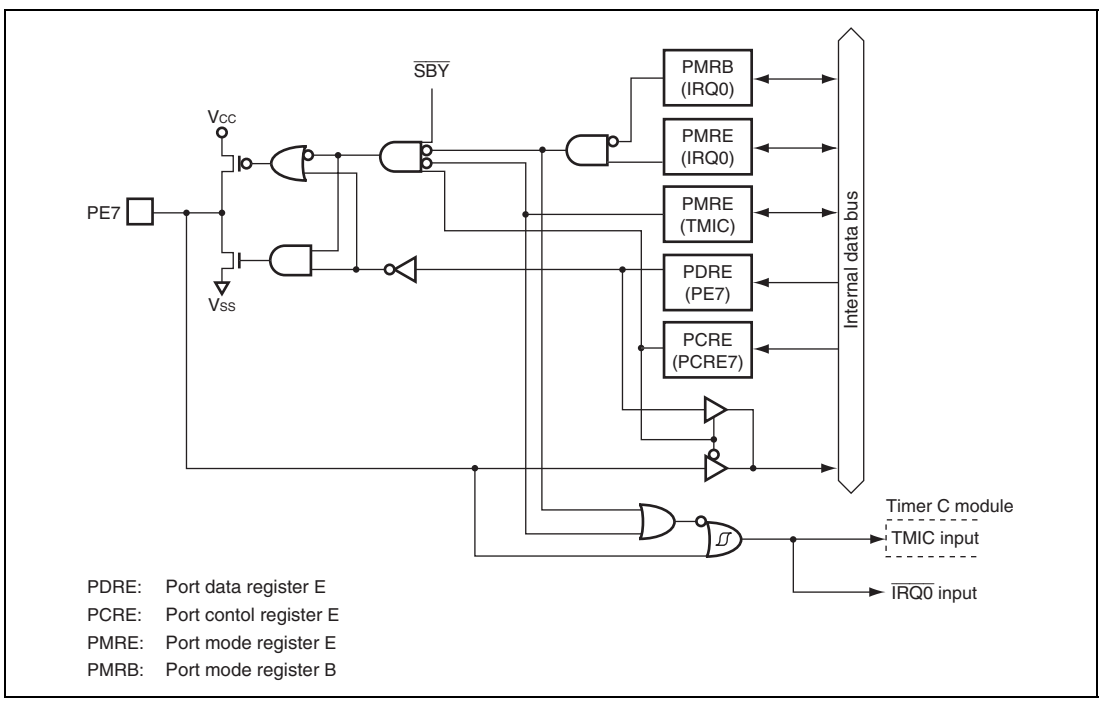


Figure B.12 (a) Port E Block Diagram (PE7)