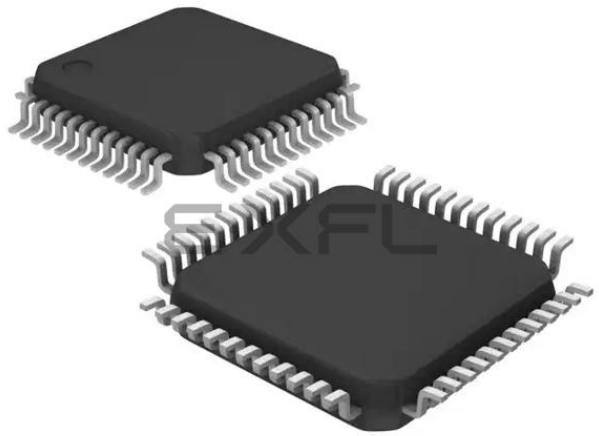

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5268tay

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with two trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 4. Peripheral clock gating bits (CLK_PCKENR1)

Control bit	Peripheral
PCKEN17	TIM1
PCKEN16	TIM3
PCKEN15	TIM2
PCKEN14	TIM4
PCKEN13	LINUART
PCKEN12	USART
PCKEN11	SPI
PCKEN10	I^2C

Detailed feature list:

- Full duplex, asynchronous communications
- NRZ standard format (mark/space)
- High-precision baud rate generator system
  - Common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits)
- Configurable stop bits: Support for 1 or 2 stop bits
- LIN master mode:
  - LIN break and delimiter generation
  - LIN break and delimiter detection with separate flag and interrupt source for readback checking.
- Transmitter clock output for synchronous communication
- Separate enable bits for transmitter and receiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - End of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Six interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Parity error
  - LIN break and delimiter detection
- Two interrupt vectors:
  - Transmitter interrupt
  - Receiver interrupt
- Reduced power consumption mode
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC positive reference voltage		-
23	19	13	9	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
24	20	14	10	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
25	21	-	-	-	V_{REF-}	S	-	-	-	-	-	-	-	ADC negative reference voltage		-
26	22	-	-	-	PF0/AIN10	I/O	**X**	X	-	-	O1	X	X	**Port F0**	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X	-	-	O1	X	X	**Port H4**	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X	-	-	O1	X	X	**Port H5**	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X	-	-	O1	X	X	**Port H6**	Timer 1 - inverted channel 2	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X	-	-	O1	X	X	**Port H7**	Timer 1 - inverted channel 2	-
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	-	-	O1	X	X	**Port E7**	Analog input 8	-
40	32	24			PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E6**	Analog input 9	-
41	33	25	17	17	PE5/SPI_NSS(2)	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/ slave select	-
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X	-	O1	X	X	**Port C0**	ADC trigger input	-
43	34	26	18	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
44	35	27	19	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
45	36	28	20	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
46	37	29	21	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
47	38	30	22	22	PC5/SPI_SCK(2)	I/O	**X**	X	X	-	O3	X	X	**Port C5**	SPI clock	-
48	39	31	-	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
49	40	32	-	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
50	41	33	23	-	PC6/SPI_MOSI (2)	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
51	42	34	24	-	PC7/SPI_MISO (2)	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
52	43	35	-	23	PG0/CAN_TX	I/O	**X**	X	-	-	O1	X	X	**Port G0**	CAN transmit	-
53	44	36	-	24	PG1/CAN_RX	I/O	**X**	X	-	-	O1	X	X	**Port G1**	CAN receive	-
54	45	-	-	-	PG2	I/O	**X**	X	-	-	O1	X	X	**Port G2**	-	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
78	62	46	30	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-
79	63	47	31	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
80	64	48	32	32	PD7/TLI(5)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. SPI and USTART are not available in STM8AF5286UC, refer to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* for the pin names.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to V_{DD} are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after reset release.
5. If this pin is configured as interrupt pin, it will trigger the TLI.

Table 14. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x40
0x00 5060 to 0x005061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215				
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5437	beCAN	CAN_PF	CAN paged register F	0xXX(3)
0x00 5438 to 0x00 57FF	Reserved area (968 bytes)			

1. Depends on the previous reset source.
2. Write only register.
3. If the bootloader is enabled, it is initialized to 0x00.

Table 15. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17(2)
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00

Table 19. Option byte description (continued)

Option byte no.	Description
OPT12	**TMU_KEY 5 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	**TMU_KEY 6 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	**TMU_KEY 7 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	**TMU_KEY 8 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	**BL[7:0]: Bootloader enable** If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

2. Guaranteed by design.
3. Guaranteed by characterization results, not tested in production.

Figure 23. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

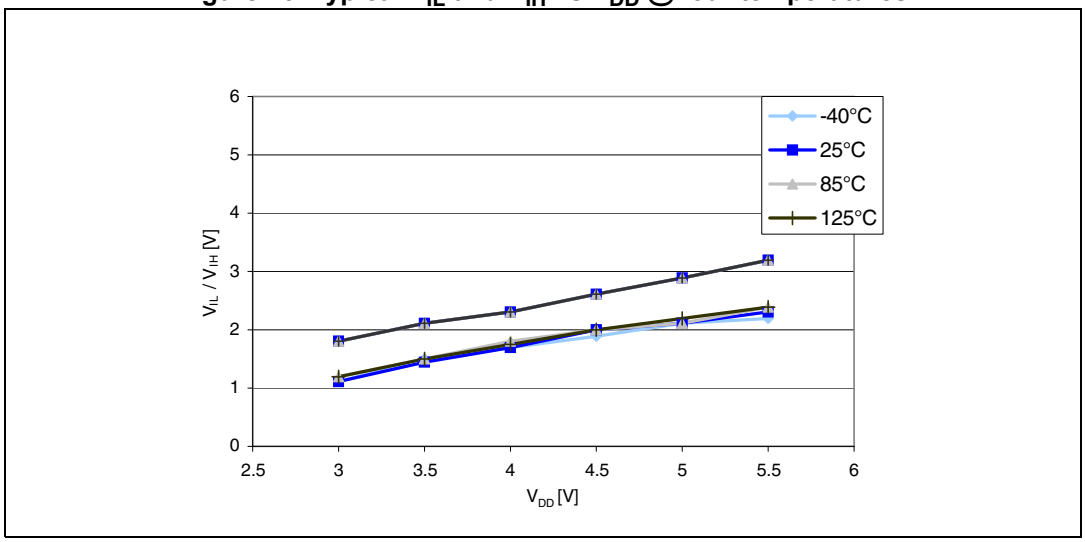
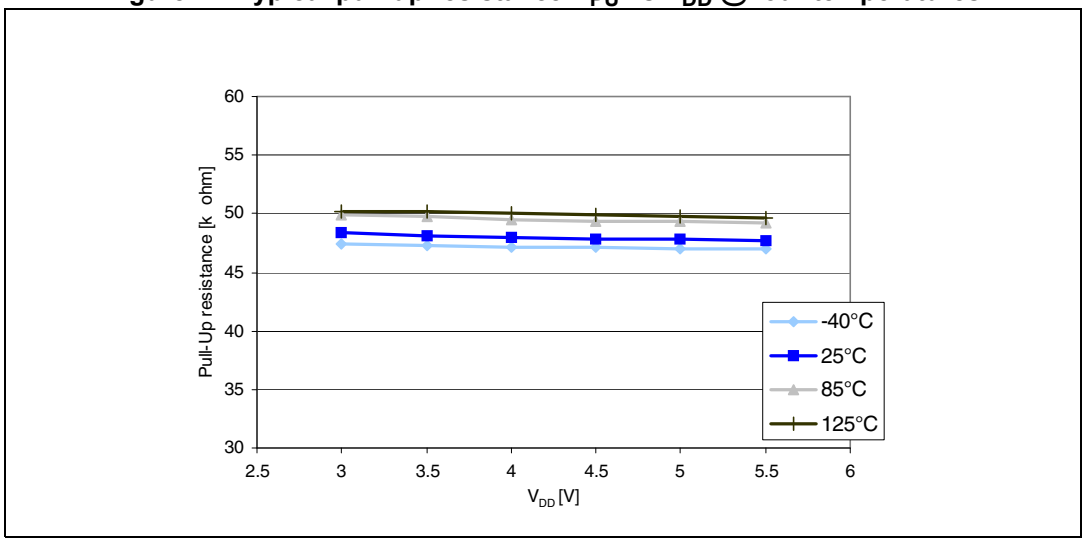


Figure 24. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST high-level input voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST low-level output voltage(1)	I_{OL} = 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Figure 36. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

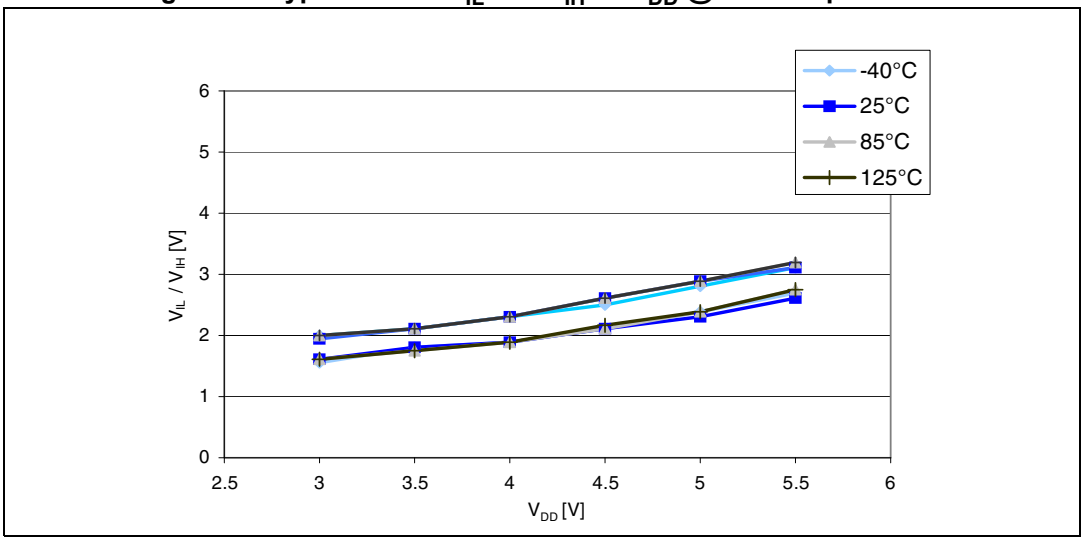


Figure 37. Typical NRST pull-up resistance R_{PU} vs V_{DD}

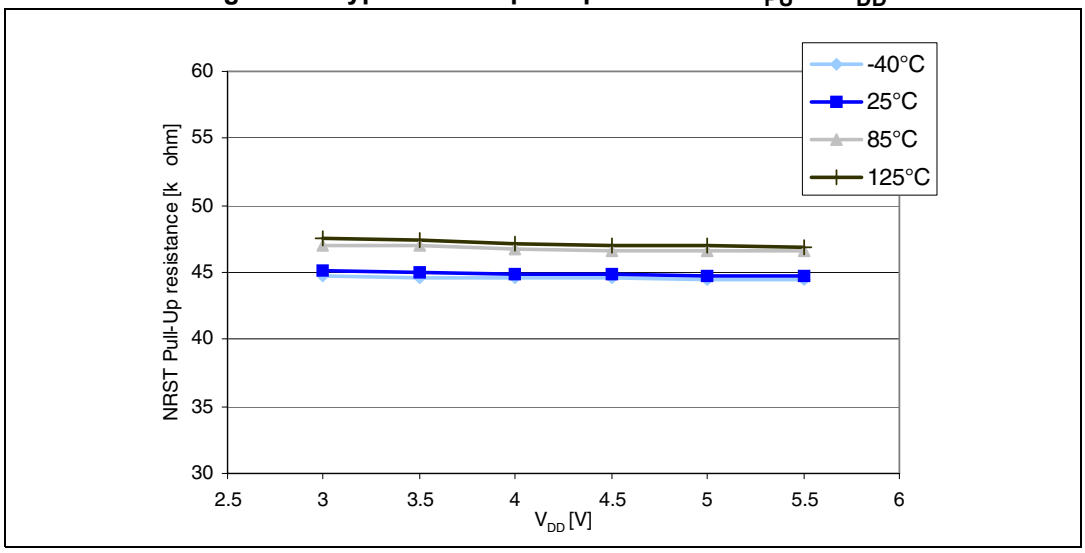
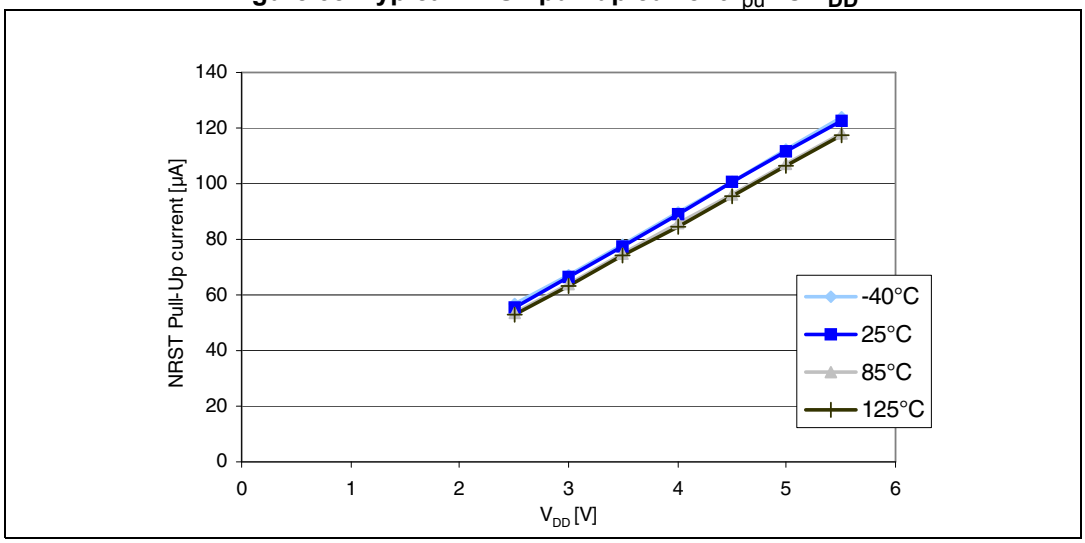


Figure 38. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 39* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 39: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 10 nF.

10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

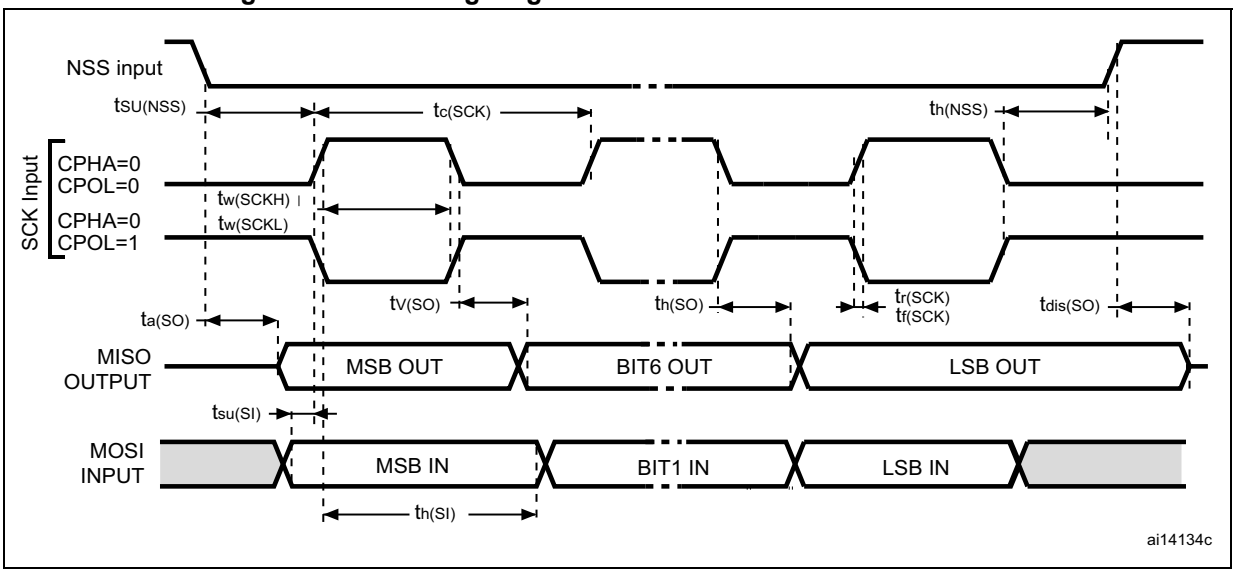
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

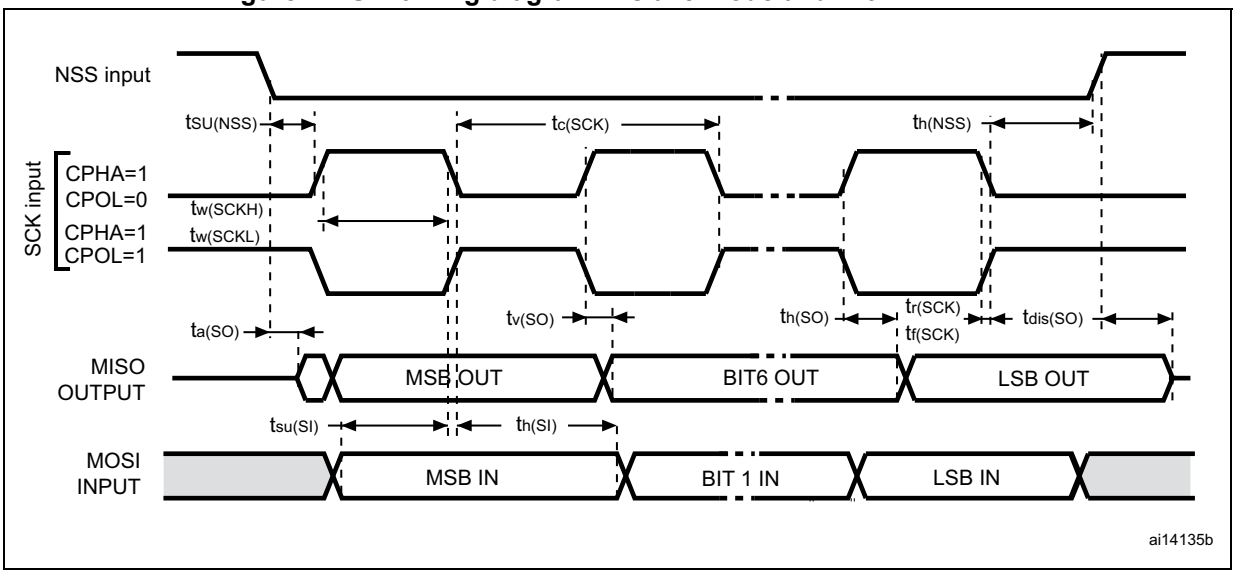
1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 40. SPI timing diagram in slave mode and with CPHA = 0



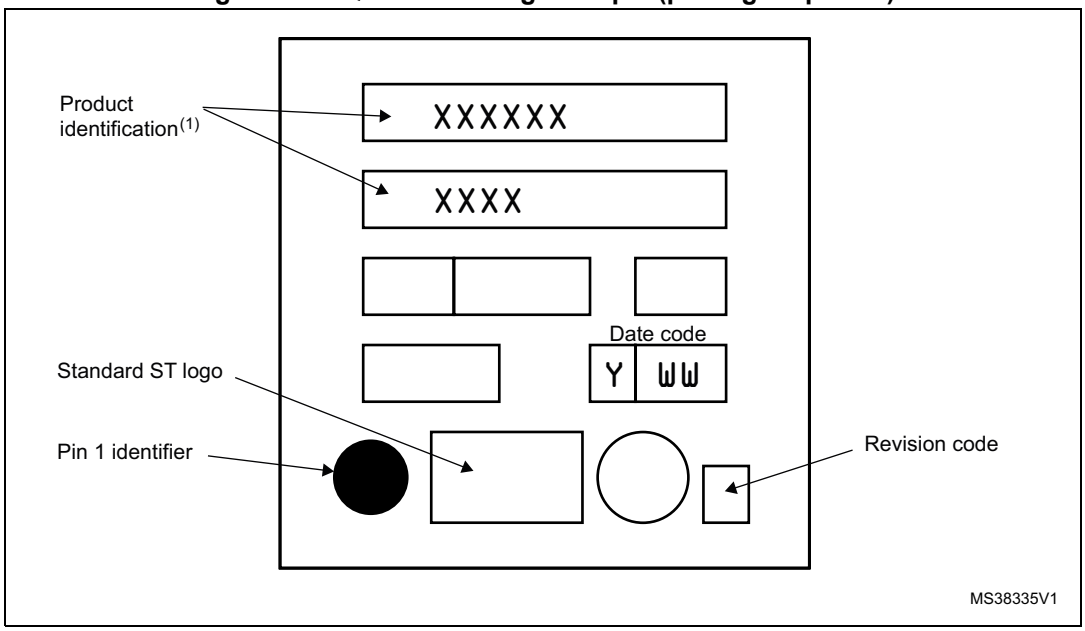
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 53. LQFP48 marking example (package top view)



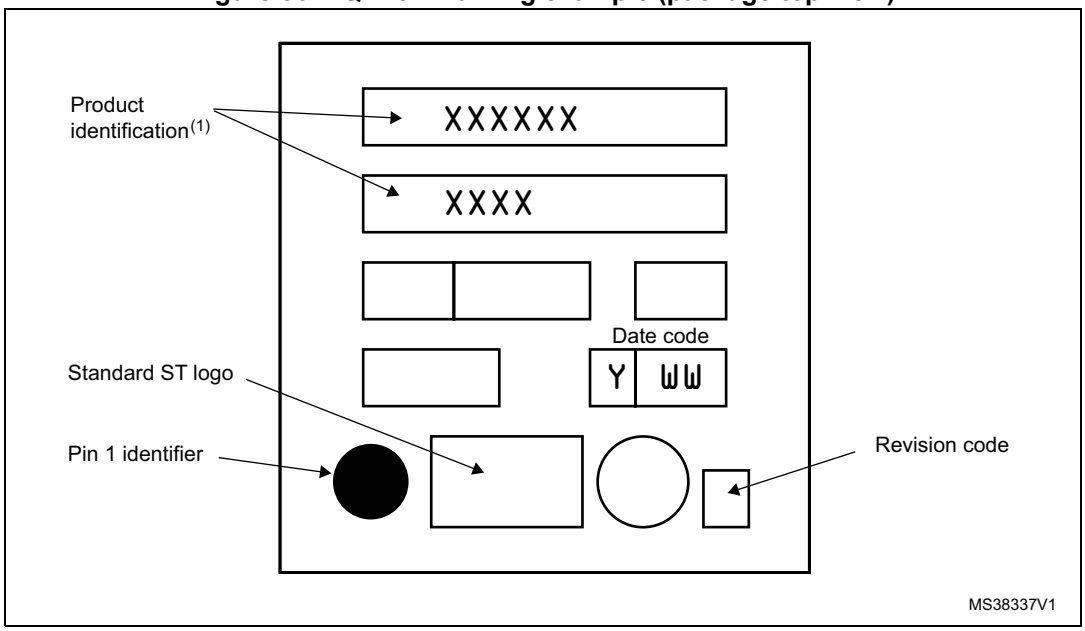
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of high density Flash program memory. Updated the number of I/Os for devices in 80-, 64-, and 48-pin packages in *Table: STM8AF52xx product line-up with CAN, Table: STM8AF62xx product line-up without CAN, Table: STM8AF/H/P51xx product line-up with CAN,* and *Table: STM8AF/H/P61xx product line-up without CAN.* Added TMU brief description in *Section 5.4: Flash program and data EEPROM*, updated TMU_MAXATT description in *Table 19: Option byte description*, and TMU_MAWATT reset value in *Table 18: Option bytes.* Updated clock sources in *Section 5.5.1: Features*. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)*. Added calibration using TIM3 in *Section 5.7.2: Auto-wakeup counter.* Added *Table 8: ADC naming* and *Table 9: Communication peripheral naming correspondence*. Updated SPI data rate to $f_{MASTER}/2$ in *Section 5.9.3: Serial peripheral interface (SPI)*. Added reset state in *Table 10: Legend/abbreviation for the pin description table.* *Table: STM8A microcontroller family pin description:* modified footnotes related to PD1/SWIM, corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. *Section: Register map:* Removed CAN register CLK_CANCCR. Removed I2C_PECR register. Added *footnote* for Px_IDR registers in *Table 13: I/O port hardware register map*. Updated register reset values for Px_IDR and PD_CR1 registers. Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, TMU, clock controller, interrupt controller, timers, communication interfaces, and ADC, by *TTable 14: General hardware register map.* Added debug module register map Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off, updated *Section 5.6: Low-power operating modes,* and *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated.* $I_{DD(FAH)}$ and $I_{DD(SAH)}$ renamed $I_{DD(AH)}$; $t_{WU(FAH)}$ and $t_{WU(SAH)}$ renamed $t_{WU(AH)}$.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-Jul-2012	9 (continued)	*Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* updated conditions for $I_{DD(RUN)}$. *Table 38: I/O static characteristics:* added new condition and new max values for rise and fall time; updated footnote 2. *Section 10.3.7: Reset pin characteristics:* updated text below *Figure 38: Typical NRST pull-up current Ipu vs VDD* *Figure 39: Recommended reset pin protection:* updated unit of capacitor. *Table 41: SPI characteristics:* updated SCK high and low time conditions and values. *Figure 42: SPI timing diagram - master mode:* replaced 'SCK input' signals with 'SCK output' signals. Updated *Table 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data* Replaced *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* Added *Figure 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint* *and* *Figure 55: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* Updated *Figure 57: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline* Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1* *Section 13.2.2: C and assembly toolchains:* added www.iar.com.
31-Mar-2014	10	Updated: – *Table 1: Device summary*, – *Table: STM8AF52xx product line-up with CAN*, – *Table: STM8AF/H/P51xx product line-up with CAN*, – *Table: STM8AF/H/P61xx product line-up without CAN*, – *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*, – The maximum speed in *Section 5.9.3: Serial peripheral interface (SPI)*, – t_{TEMP} Reset release delay /VDD rising typical and max values in *Table 25: Operating conditions at power-up/power-down*, – The symbol $t_{IFP(NRST)}$ with $t_{INFP(NRST)}$ in *Table 39: NRST pin characteristics*, – The address and comment for Reset in *Table 17: STM8A interrupt table*.