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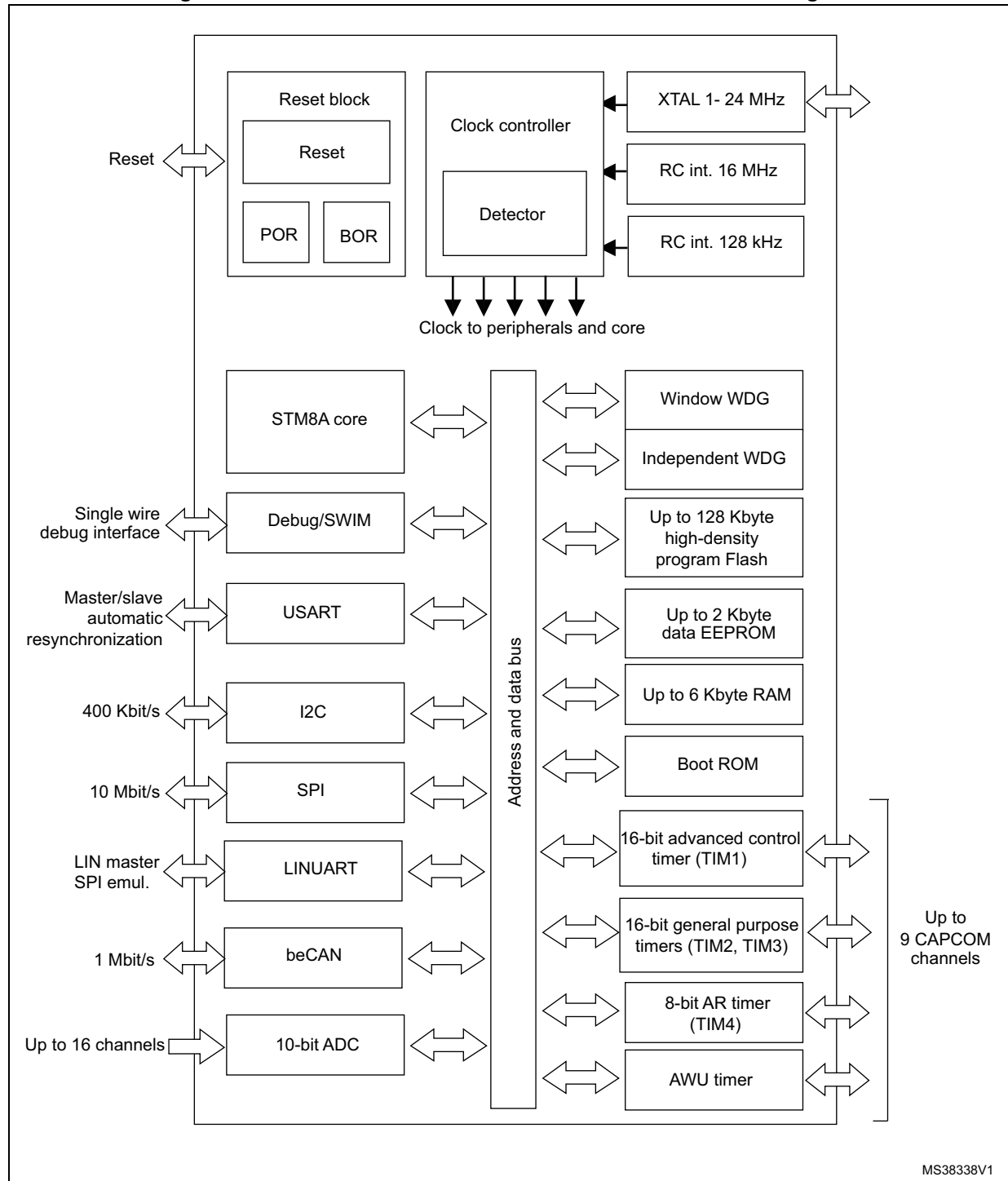
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5269tay

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 4. Peripheral clock gating bits (CLK_PCKENR1)

Control bit	Peripheral
PCKEN17	TIM1
PCKEN16	TIM3
PCKEN15	TIM2
PCKEN14	TIM4
PCKEN13	LINUART
PCKEN12	USART
PCKEN11	SPI
PCKEN10	I ² C

5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{\text{MASTER}}/2$ for master, 8 Mbit/s or $f_{\text{MASTER}}/2$ for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
 - CRC value can be transmitted as last byte in Tx mode
 - CRC error checking for last received byte

5.9.4 Inter integrated circuit (I²C) interface

The devices covered by this datasheet contain one I²C interface. The interface is available on all the supported packages.

- I²C master features:
 - Clock generation
 - Start and stop generation
- I²C slave features:
 - Programmable I²C address detection
 - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
 - Standard speed (up to 100 kHz),
 - Fast speed (up to 400 kHz)
- Status flags:
 - Transmitter/receiver mode flag
 - End-of-byte transmission flag
 - I²C busy flag
- Error flags:
 - Arbitration lost condition for master mode
 - Acknowledgement failure after address/data transmission
 - Detection of misplaced start or stop condition
 - Overrun/underrun if clock stretching is disabled

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I²C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

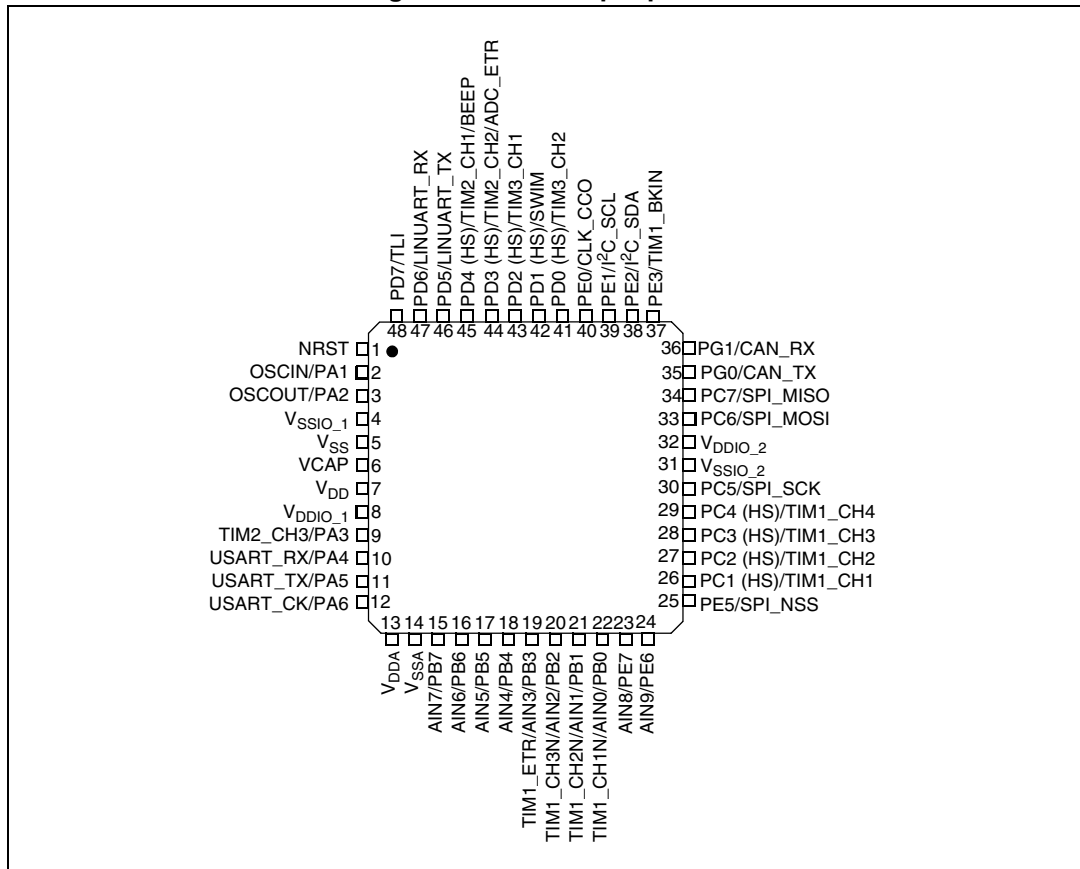
The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:

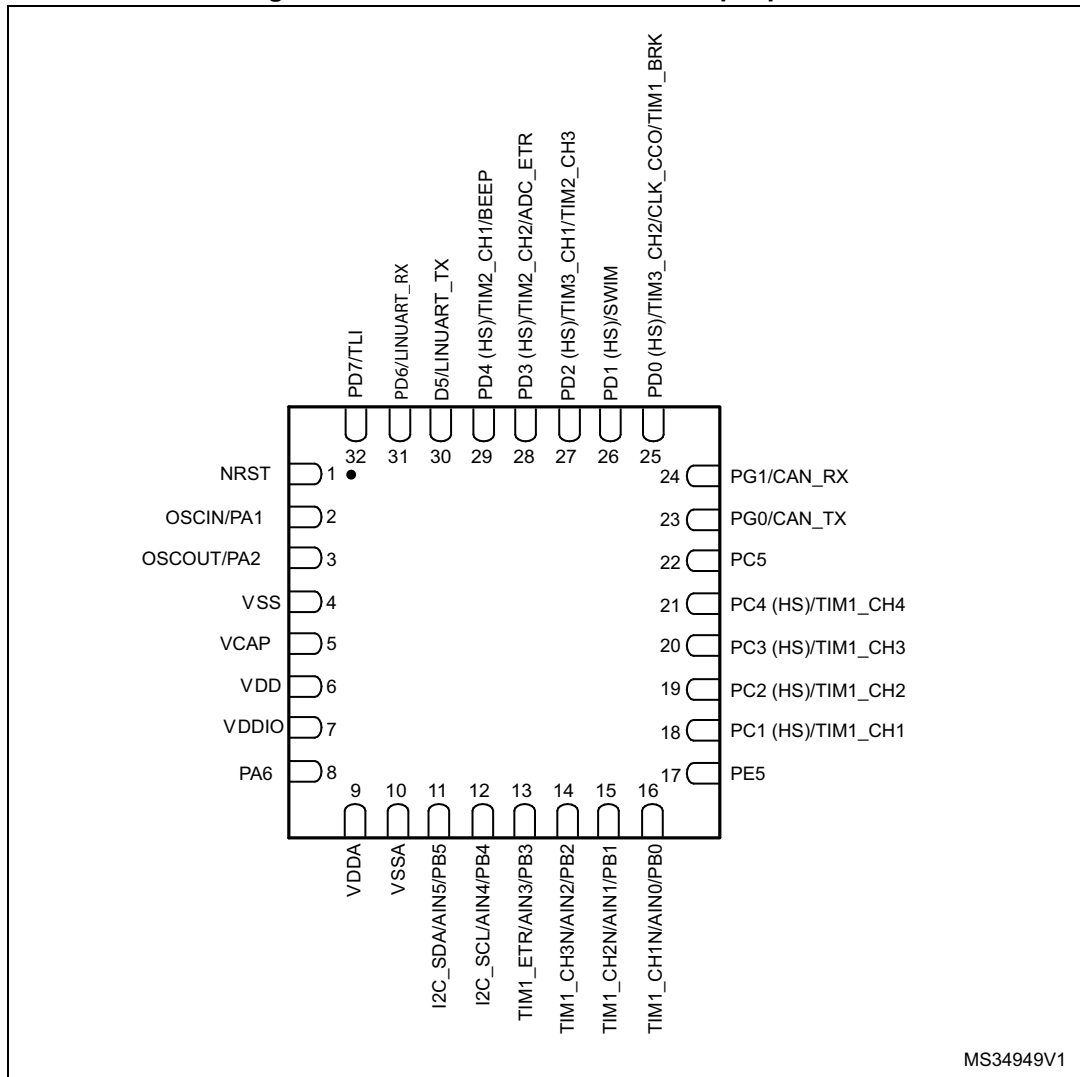
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Figure 5. LQFP 48-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Figure 7. STM8AF52x6 VFQFPN32 32-pin pinout



1. The following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7. As a consequence, they must be put into one of the following configurations by software:
 - configured as input with internal pull-up/down resistor,
 - configured as output push-pull low.
2. HS stands for high sink capability.

7 Memory and register map

7.1 Memory map

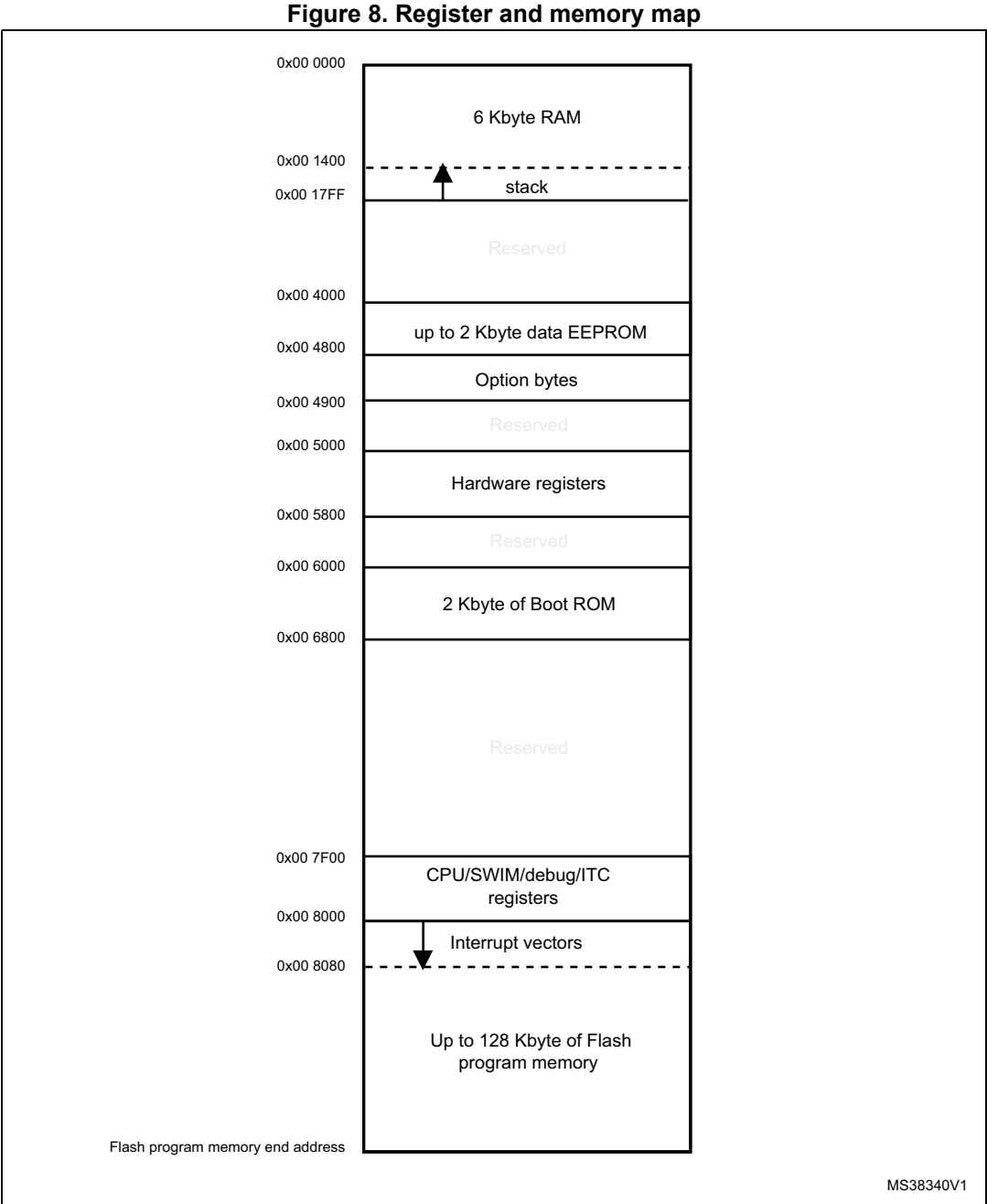


Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215				
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = -40\text{ }^{\circ}\text{C}$, $T_A = 25\text{ }^{\circ}\text{C}$, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

Figure 9. Pin loading conditions

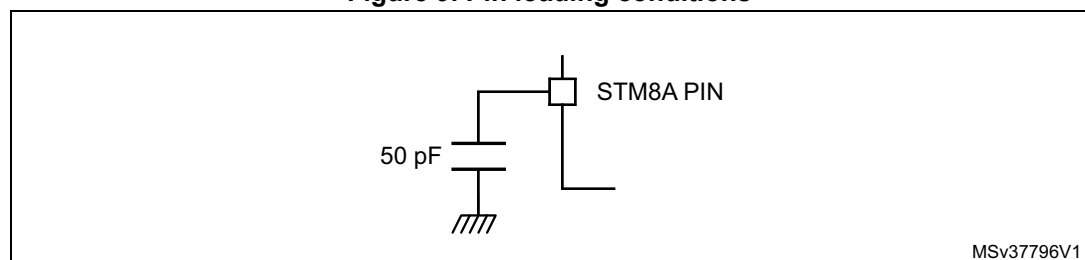


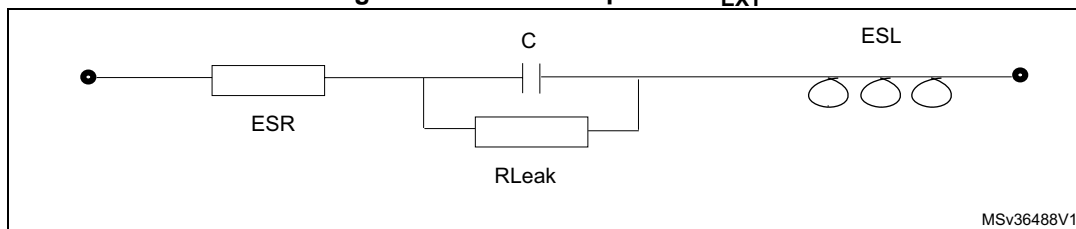
Table 25. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2 ⁽¹⁾	-	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	-	2 ⁽¹⁾	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	1.7	ms
	Reset generation delay	V_{DD} falling	-	3	-	μs
V_{IT+}	Power-on reset threshold ⁽²⁾ (3)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70 ⁽¹⁾	-	mV

1. Guaranteed by design, not tested in production.
2. If V_{DD} is below 3 V, the code execution is guaranteed above the V_{IT-} and V_{IT+} thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1 μF requires $Q=1 \mu\text{F} \times 1.8 \text{ V} = 1.8 \mu\text{C}$.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in [Table 24](#). Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT} 

1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in [Figure 9 on page 59](#) and [Figure 10 on page 60](#).

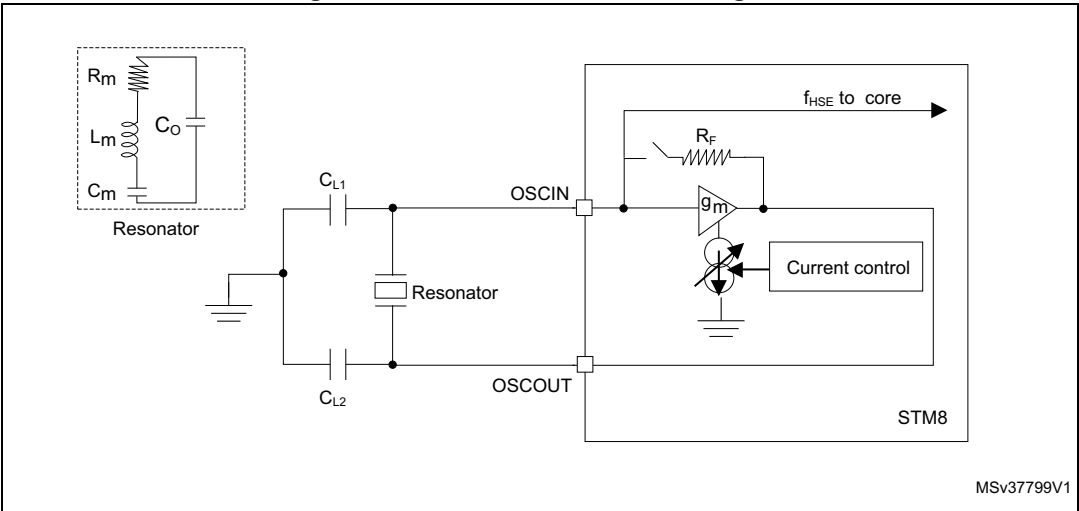
If not explicitly stated, general conditions of temperature and voltage apply.

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	220	-	$k\Omega$
$C_{L1}/C_{L2}^{(1)}$	Recommended load capacitance	-	-	-	20	pF
g_m	Oscillator trans conductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(2)}$	Startup time	V_{DD} is stabilized	-	2.8	-	ms

1. The oscillator needs two load capacitors, C_{L1} and C_{L2} , to act as load for the crystal. The total load capacitance (C_{Load}) is $(C_{L1} * C_{L2}) / (C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1}/2$. Some oscillators have built-in load capacitors, C_{L1} and C_{L2} .
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 24 MHz oscillation is reached. It can vary with the crystal type that is used.

Figure 20. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

The crystal characteristics have to be checked with the following formula:

Equation 1

$$g_m \gg g_{mcrit}$$

where g_{mcrit} can be calculated with the crystal parameters as follows:

Equation 2

$$g_{mcrit} = (2 \times \pi \times f_{HSE})^2 \times R_m (2C_o + C)^2$$

- R_m : Notional resistance (see crystal specification)
- L_m : Notional inductance (see crystal specification)
- C_m : Notional capacitance (see crystal specification)
- C_o : Shunt capacitance (see crystal specification)
- $C_{L1} = C_{L2} = C$: Grounded external capacitance

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

High-speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} = 3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 150\text{ }^{\circ}\text{C}$	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2 ⁽¹⁾	μs

1. Guaranteed by characterization results, not tested in production.

Figure 21. Typical HSI frequency vs V_{DD}

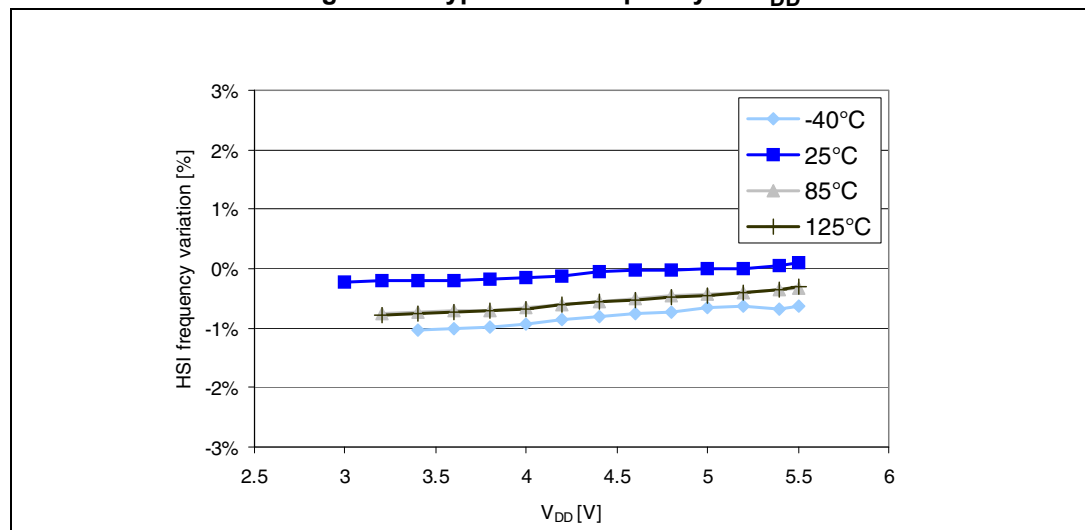


Table 37. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance ⁽¹⁾ (erase/write cycles)	$T_A = 25\text{ °C}$	300 k	-	cycles
		$T_A = -40\text{ °C to }125\text{ °C}$	100 k ⁽²⁾	-	
t_{RET}	Data retention time	$T_A = 25\text{ °C}$	40 ⁽²⁾⁽³⁾	-	years
		$T_A = 55\text{ °C}$	20 ⁽²⁾⁽³⁾	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	-	-0.3 V		$0.3 \times V_{DD}$	V
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		$V_{DD} + 0.3 \text{ V}$	
V_{hys}	Hysteresis ⁽¹⁾		-	$0.1 \times V_{DD}$	-	
V_{OH}	High-level output voltage	Standard I/O, $V_{DD} = 5 \text{ V}$, $I = 3 \text{ mA}$	$V_{DD} - 0.5 \text{ V}$	-	-	V
		Standard I/O, $V_{DD} = 3 \text{ V}$, $I = 1.5 \text{ mA}$	$V_{DD} - 0.4 \text{ V}$	-	-	
V_{OL}	Low-level output voltage	High sink and true open drain I/O, $V_{DD} = 5 \text{ V}$ $I = 8 \text{ mA}$	-	-	0.5	V
		Standard I/O, $V_{DD} = 5 \text{ V}$ $I = 3 \text{ mA}$	-	-	0.6	
		Standard I/O, $V_{DD} = 3 \text{ V}$ $I = 1.5 \text{ mA}$	-	-	0.4	
R_{pu}	Pull-up resistor	$V_{DD} = 5 \text{ V}$, $V_{IN} = V_{SS}$	35	50	65	k Ω
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35 ⁽²⁾	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125 ⁽²⁾	
		Fast I/Os Load = 20 pF	-	-	20 ⁽²⁾	
		Standard and high sink I/Os Load = 20 pF	-	-	50 ⁽²⁾	
I_{lkg}	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA
$I_{lkg \text{ ana}}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ $-40^\circ\text{C} < T_A < 125^\circ\text{C}$	-	-	± 250	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ $-40^\circ\text{C} < T_A < 150^\circ\text{C}$	-	-	± 500	
$I_{lkg(inj)}$	Leakage current in adjacent I/O ⁽³⁾	Injection current $\pm 4 \text{ mA}$	-	-	± 1 ⁽³⁾	μA
I_{DDIO}	Total current on either V_{DDIO} or V_{SSIO}	Including injection currents	-	-	60	mA

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

10.3.10 I²C interface characteristicsTable 42. I²C characteristics

Symbol	Parameter	Standard mode I ² C		Fast mode I ² C ⁽¹⁾		Unit
		Min ⁽²⁾	Max ⁽²⁾	Min ⁽²⁾	Max ⁽²⁾	
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	-	μs
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	
t _{su(SDA)}	SDA setup time	250	-	100	-	ns
t _{h(SDA)}	SDA data hold time	0 ⁽³⁾	-	0 ⁽⁴⁾	900 ⁽³⁾	
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time (V _{DD} 3 V to 5.5 V)	-	1000	-	300	
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time (V _{DD} 3 V to 5.5 V)	-	300	-	300	
t _{h(STA)}	START condition hold time	4.0	-	0.6	-	μs
t _{su(STA)}	Repeated START condition setup time	4.7	-	0.6	-	
t _{su(STO)}	STOP condition setup time	4.0	-	0.6	-	μs
t _{w(STO:STA)}	STOP to START condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER} must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-4	4/A

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

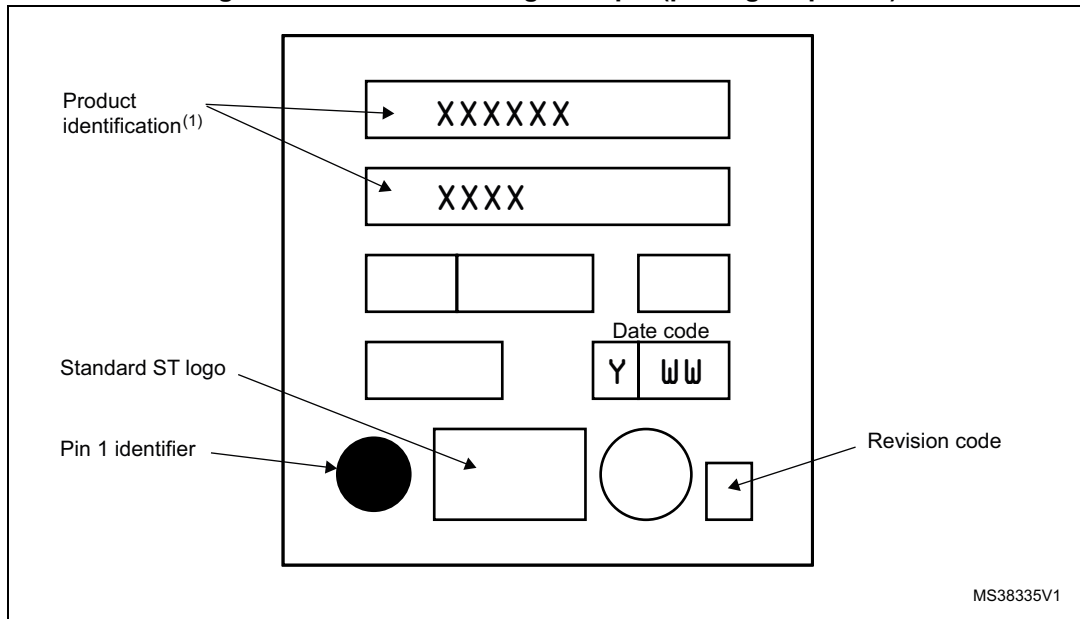
Symbol	Parameter	Conditions	Class ⁽¹⁾
LU	Static latch-up class	$T_A = 25\text{ °C}$	A
		$T_A = 85\text{ °C}$	
		$T_A = 125\text{ °C}$	
		$T_A = 150\text{ °C}$	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

Technical drawing of a square microchip package. The package is square with a side length of 16.7. The drawing shows the top and bottom views. The top view shows a central square area with a side length of 14.3. The bottom view shows a central square area with a side length of 12.75. The package has 60 pins on the top edge, 41 pins on the right edge, 21 pins on the bottom edge, and 1 pin on the left edge. The pin numbers are: 60, 41, 21, 1, 1, 20, 21, 41, 60. The package is labeled with the number 15. The drawing includes dimensions for the package size (16.7), the central area (14.3, 12.75), and the pin pitch (0.65, 0.4, 1.2).

1S_FP

Figure 53. LQFP48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Oct-2016	14	<p>Updated:</p> <ul style="list-style-type: none"> – Title of Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout, (previously STM8AF5286UC VFQFPN32 32-pin pinout) – Footnotes of Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme 1 – Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description replaced “STM8AF5286UC VQFPN32” with “STM8AF52x6 VQFPN32” at header row – Section 10.2: Absolute maximum ratings – Section : Device marking on page 93 – Section : Device marking on page 96 – Section : Device marking on page 99 – Section : Device marking on page 104 – Section : Device marking on page 108 <p>Added:</p> <ul style="list-style-type: none"> – Footnote on Figure 47: LQFP80 marking example (package top view), Figure 50: LQFP64 marking example (package top view), Figure 56: LQFP32 marking example (package top view), Figure 59: VFQFPN32 marking example (package top view).
10-Nov-2016	15	<p>Updated header row and PA6/USART_CK pin row on Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description.</p>