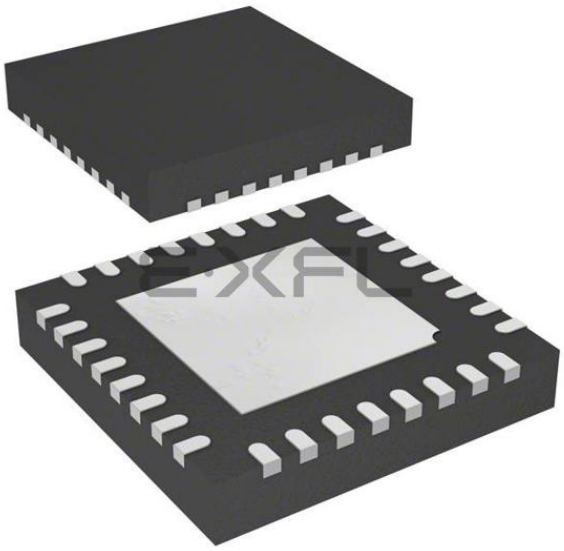

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5286ucy

List of tables

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram

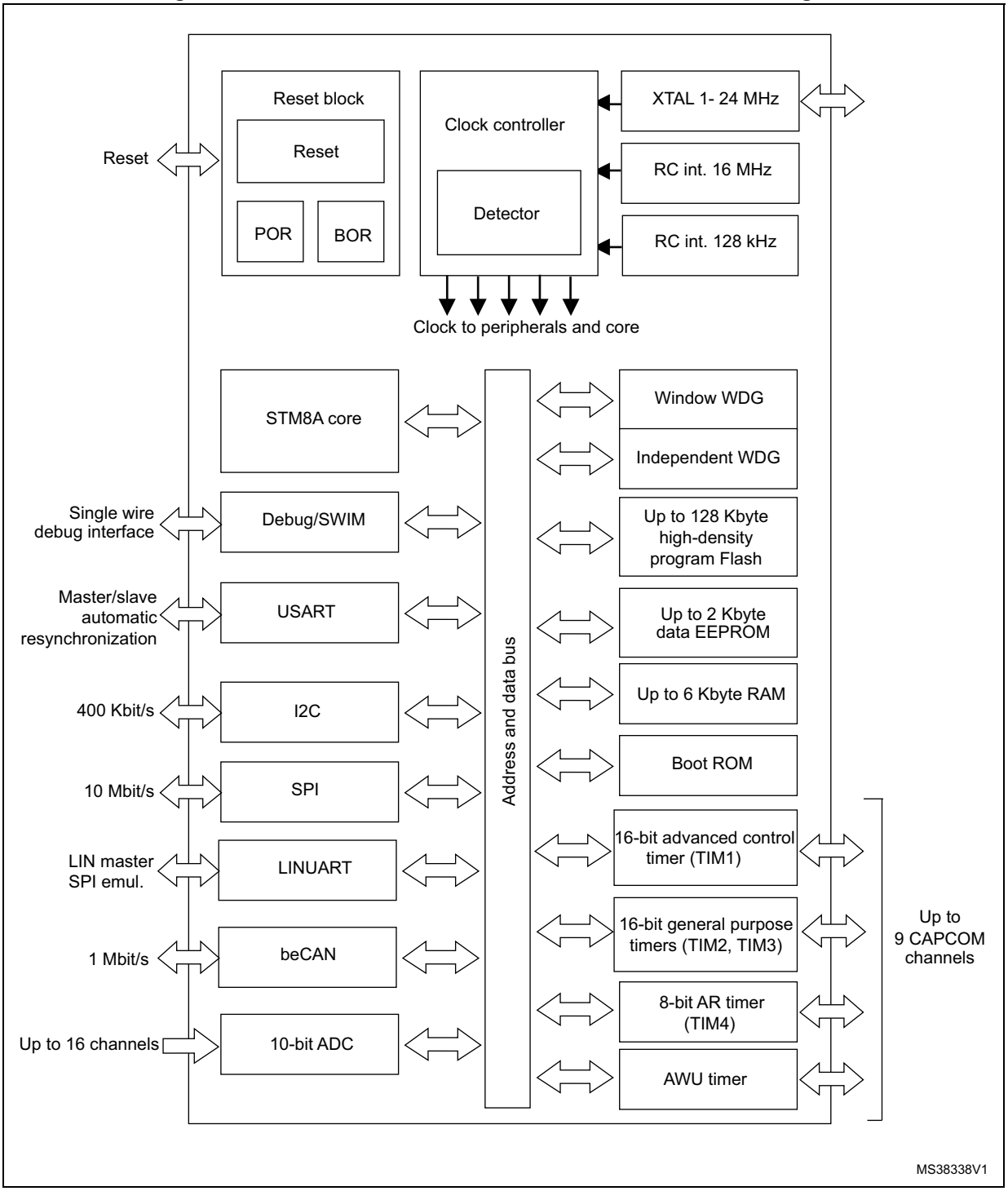


Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
78	62	46	30	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-
79	63	47	31	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
80	64	48	32	32	PD7/TLI(5)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. SPI and USTART are not available in STM8AF5286UC, refer to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* for the pin names.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to V_{DD} are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after reset release.
5. If this pin is configured as interrupt pin, it will trigger the TLI.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 18: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be changed in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 18. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
0x00 4801	User boot code (UBC)	OPT1	UBC[7:0]								0x00
0x00 4802		NOPT1	NUBC[7:0]								0xFF
0x00 4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x00 4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x00 4805	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	0x00
0x00 4806		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	0xFF
0x00 4807	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	0x00
0x00 4808		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	0xFF
0x00 4809	HSE clock startup	OPT5	HSECNT[7:0]								0x00
0x00 480A		NOPT5	NHSECNT[7:0]								0xFF

Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

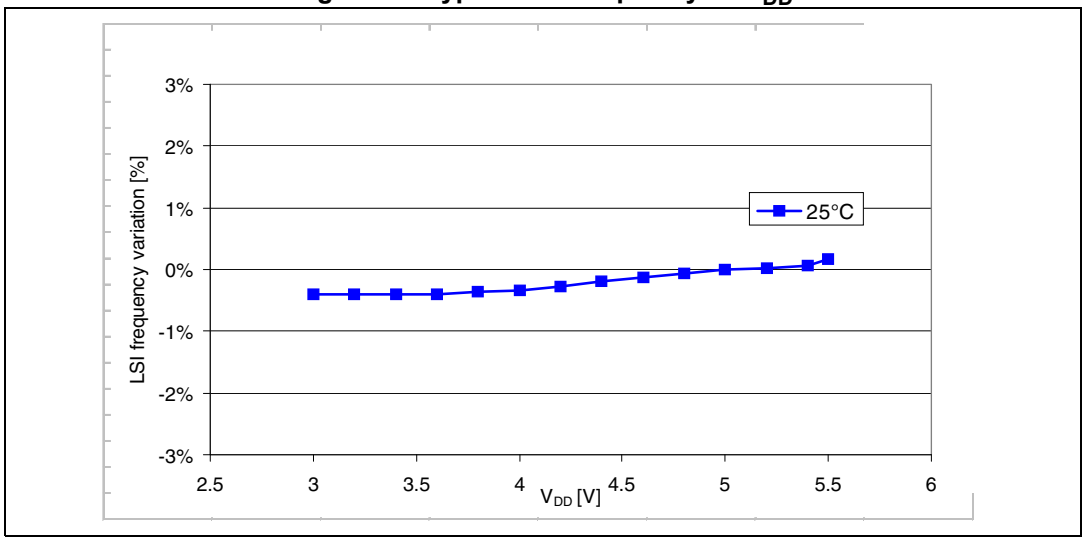


Table 37. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Figure 37. Typical NRST pull-up resistance R_{PU} vs V_{DD}

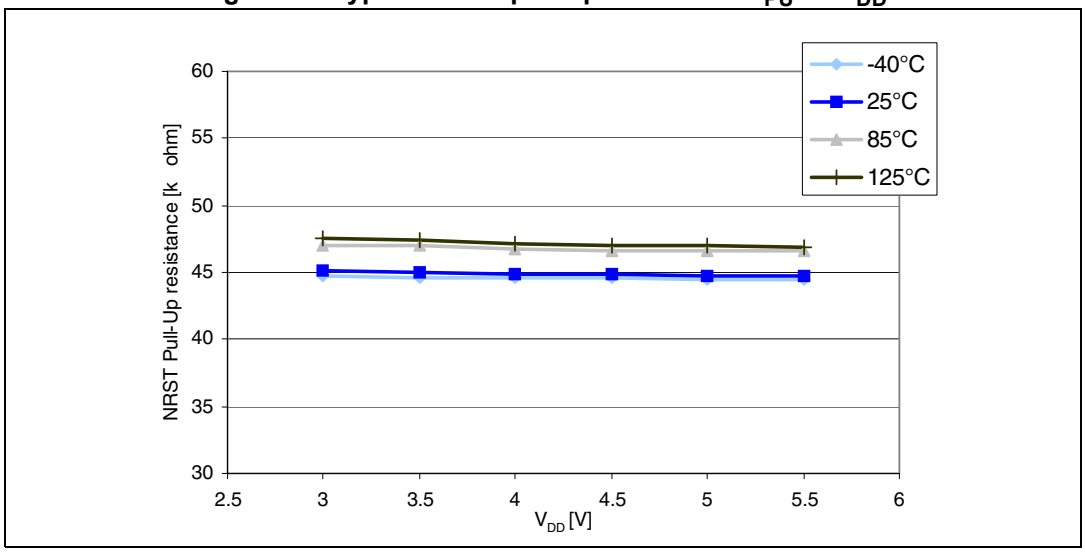
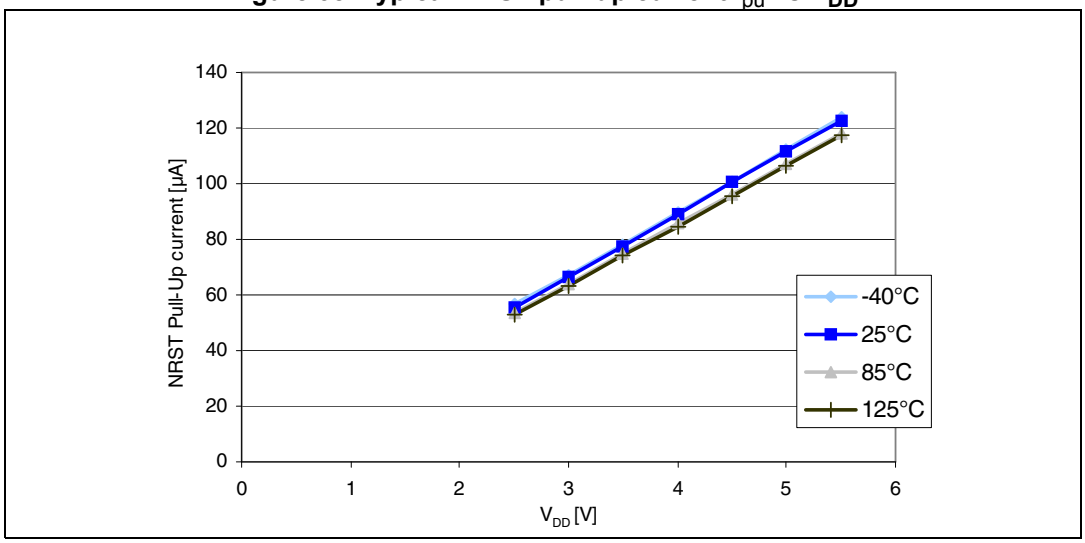


Figure 38. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 39* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 39: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 10 nF.

10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

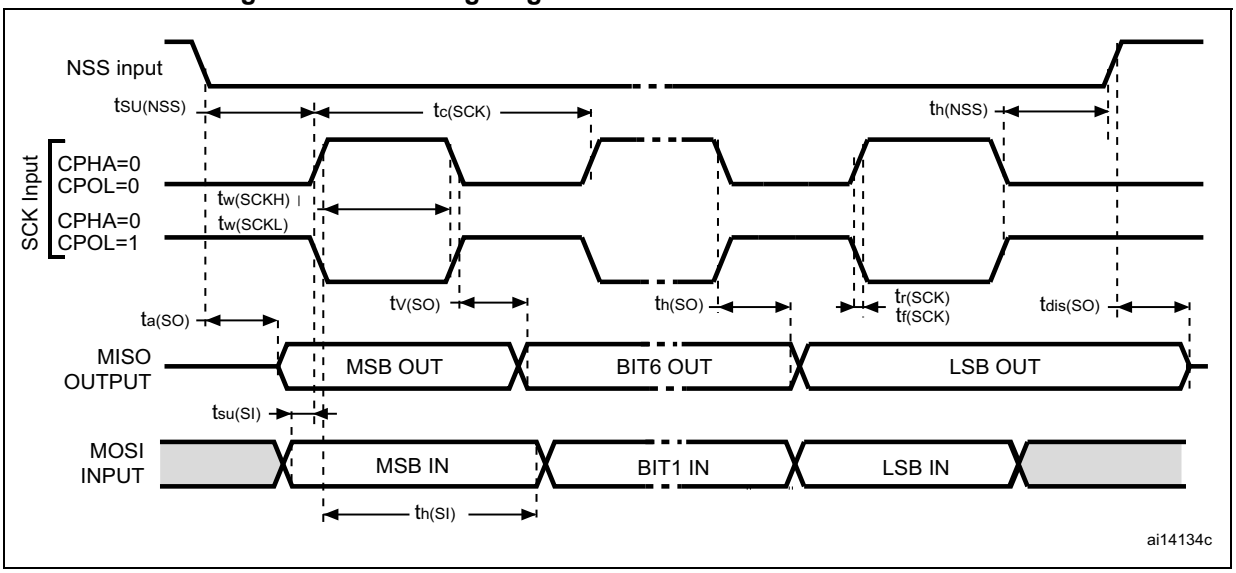
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

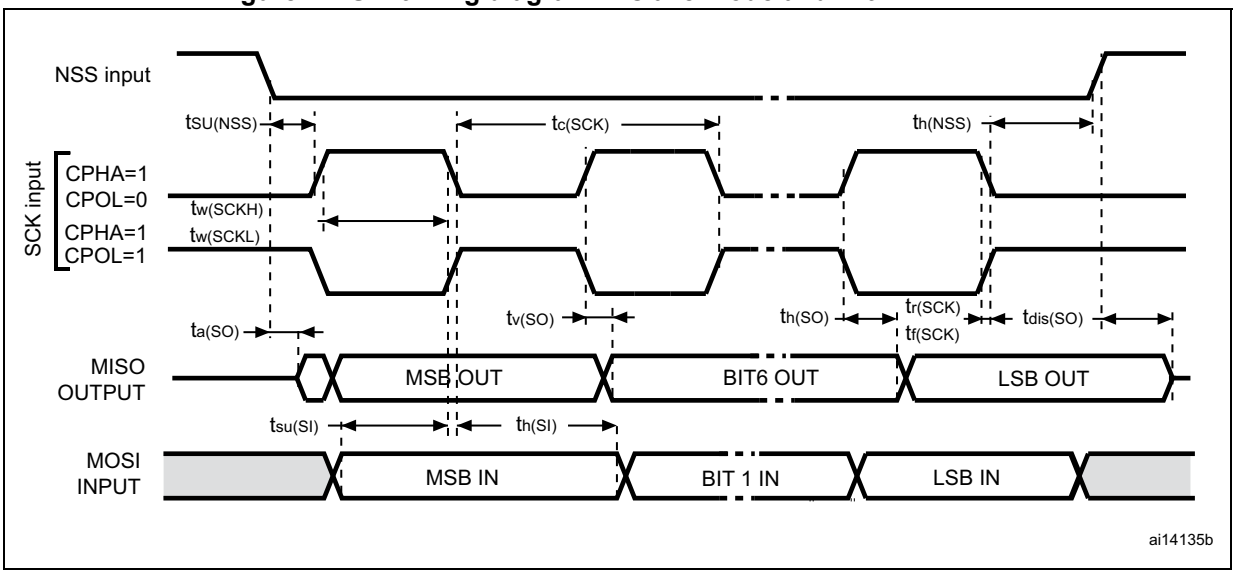
1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 40. SPI timing diagram in slave mode and with CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

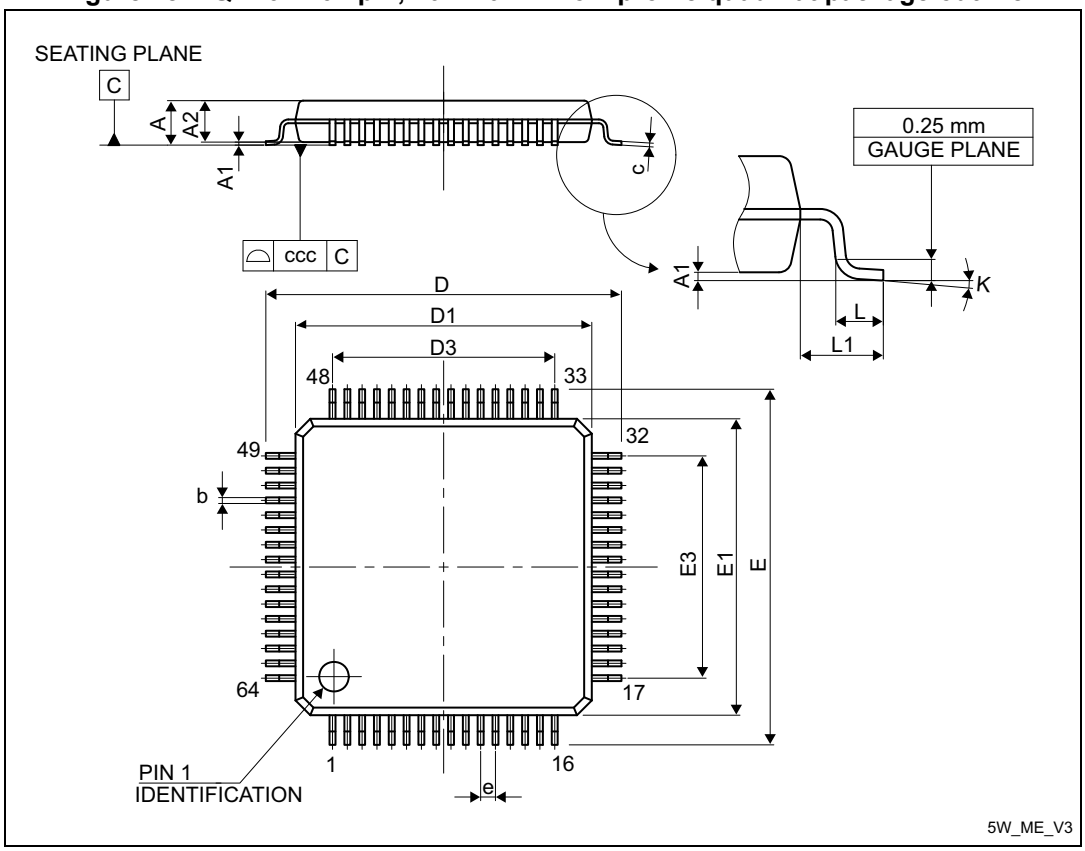
Table 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.2 LQFP64 package information

Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

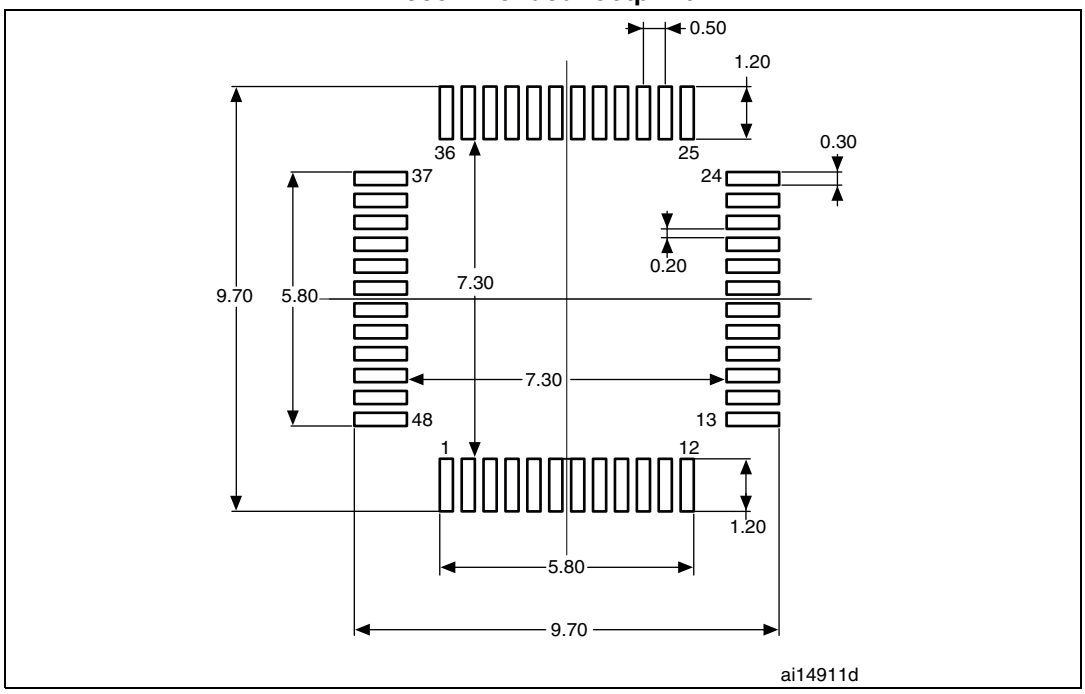


1. Drawing is not to scale.

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

13 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

13.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

13.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high-speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	Added 'H' products to the datasheet (Flash no EEPROM). *Section : Features* on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1. *Table 1: Device summary*: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166. *Section 1: Introduction*, *Section 5: Product overview*, *Section 9: Option bytes*, *Section 6.2: Alternate function remapping*, *Table 21: Current characteristics:* Updated reference documentation: RM0009, PM0047, and UM0470. *Section 2: Description*: added information about peak performance. *Section 3: Product line-up*: Removed *STM8A common features* table. *Table 4: Peripheral clock gating bits (CLK_PCKENR1):* Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T. *Table 5: Peripheral clock gating bits (CLK_PCKENR2)*: Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T. *Section 5: Product overview*: Made minor content changes and improved readability and layout. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: Major modification, TMU included. *Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI)*: User trimming updated. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: LSI as CPU clock added. *Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE)*, *Section 5.5.5: External clock input*: Maximum frequency conditional 32 Kbyte/128 Kbyte. *Section 5.8: Analog to digital converter (ADC)*: Scan for 128 Kbyte removed. *Section 5.9: Communication interfaces*, *Section 5.9.3: Serial peripheral interface (SPI)*: SPI 10 Mb/s. *Figure 3: LQFP 80-pin pinout*, *Figure 4: LQFP 64-pin pinout*, *Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout*: Amended footnote 1. *Table 12: Memory model 128K:* HS output changed from 20 mA to 8 mA. *Section 7: Memory and register map*: Corrected *Table 8: Register and memory map*; removed address list; added *Table 14: General hardware register map*. *Section 10.3.2: Supply current characteristics* Note on typical/WC values added.

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Apr-2010	6	Updated title on cover page. Modified cover page header to clarify the part numbers covered by the datasheets. Updated footnote on *Table 1: Device summary* to add 'P' order codes. Changed definition of 'P' order codes. 'Q' order codes (FASTROM and EEPROM) removed. Reorganized the content of *Section 5: Product overview*. *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* updated PD7/TLI alternate function, removed caution note for PD6/ LINUART_RX, and added note to PA1/OSCIN. Renamed *Section 7: Memory and register map*, and merged content with *Section: Register map*. Updated *Figure 8: Register and memory map*. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table 18: Option bytes*. Updated AFR4 definition in *Table 19: Option byte description*. Added C_{EXT} in *Table 24: General operating conditions*, and *Section 10.3.1: VCAP external capacitor*. Updated t_{VDD} in *Table 25: Operating conditions at power-up/power-down*. Moved *Table 30: Typical peripheral current consumption VDD = 5.0 V* to *Section : Current consumption for on-chip peripherals*. Removed $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*. Updated *Section 12: Ordering information* to the devices supported by the datasheet. Updated *Section 13: STM8 development tools*.
08-Jul-2010	7	Added STM8AF5168 and STM8AF518A part number in *Figure 4*, and STM8AF618A in *Figure 5*. Added STM8AF52xx, STM8AF6269, STM8AF628x, and STM8AF62Ax. Updated D temperature range to -40 to 150°C. Updated number of I/Os on cover page. Added *Table 23: Operating lifetime*. Restored $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*. *Table 24: General operating conditions*: updated V_{CAP} information. ESL parameter, and range D maximum junction temperature (T_J). Added STM8AF52xx and STM8AF62xx, and footnote in *Section 12: Ordering information*. Updated *Section 13: STM8 development tools*: added *Table: Product evolution summary*, and split the beCAN time triggered communication mode limitation in two sections.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8 (continued)	Removed note 1 in *Table 24: General operating conditions* and note 1 below *Figure 11: fCPUmax versus VDD*. Removed note 3 in *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C*. Removed note 2 in *Table 31: HSE external clock characteristics* and *Table 35: Flash program memory/data EEPROM memory* Removed note 1 in *Table 37: Data memory*. Modified T_{WE} maximum value in *Table 36: Flash program memory* and *Table 37: Data memory*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table 39: NRST pin characteristics*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 39: Recommended reset pin protection,* and updated external capacitor value. Updated *Note 1* in *Table 40: TIM 1, 2, 3, and 4 electrical specifications.* Updated *Note 1* in *Table 41: SPI characteristics.* Moved know limitations to separate errata sheet. Added “not recommended for new design” note to device family 51, memory size 7 and 9, and temperature range B, in *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added Raisonance compiler in *Section 13.2: Software tools.*
18-Jul-2012	9	Updated wildcards of document part numbers. Added VFQFPN package. Added STM8AF62A6 part number. *Table 1: Device summary* updated footnote *1* and added footnote *2*. *Table: STM8AF52xx product line-up with CAN* and *Table: STM8AF62xx product line-up without CAN*: added “P” version for all order codes; updated size of data EEPROM for 64K devices to 2K instead of 1.5K; updated RAM. *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram*: updated POR, BOR and WDG; removed PDR; added legend. *Section 5.4: Flash program and data EEPROM*: removed non relevant bullet points and added a sentence about the factory program. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)* and updated *Table 5: Peripheral clock gating bits (CLK_PCKENR2)* *Section : ADC features*: updated ADC input range. *Table 12: Memory model 128K:* updated RAM size, RAM end addresses, and stack roll-over addresses; updated footnote *1* *Table 18: Option bytes:* updated factory default setting for NOPT17; updated footnotes. *Table 20: Voltage characteristics:* updated V_{DDX} - V_{DD} to V_{DDX} - V_{SS}. *Table 24: General operating conditions:* updated V_{CAP}.