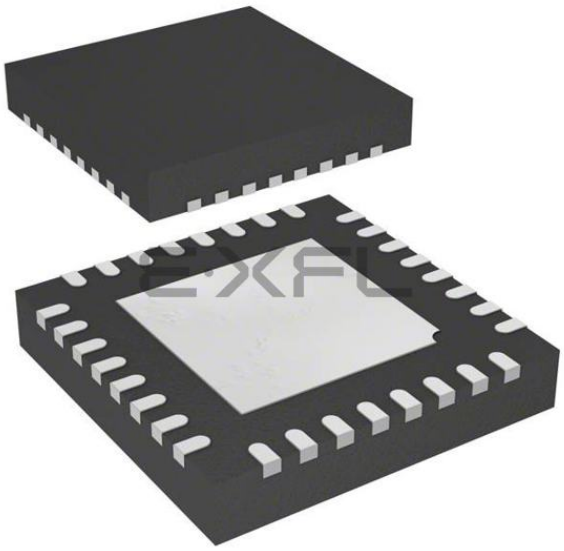

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5286udx

3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P5289		64 K						
STM8AF/P5269		32 K		1 K				
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K		1K				
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I²C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I²C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P6289		64 K		2 K				
STM8AF/P6269		32 K		1 K				
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P6288		64 K						
STM8AF/P6286	LQFP32 (7x7)				7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P62A6	VFQFPN32 (5x5)	128 K						

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with two trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

Table 5. Peripheral clock gating bits (CLK_PCKENR2)

Control bit	Peripheral
PCKEN27	CAN
PCKEN26	Reserved
PCKEN25	Reserved
PCKEN24	Reserved
PCKEN23	ADC
PCKEN22	AWU
PCKEN21	Reserved
PCKEN20	Reserved

5.6 Low-power operating modes

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- Wait mode

  In this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.

- Active-halt mode with regulator on

  In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.

- Active-halt mode with regulator off

  This mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.

- Halt mode

  CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see *Table 8*).

Table 8. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC2

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 9*).

Table 9. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
USART	UART1
LINUART	UART3

5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ for master, 8 Mbit/s or f_{MASTER} /2 for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

5.9.4 Inter integrated circuit (I^2C) interface

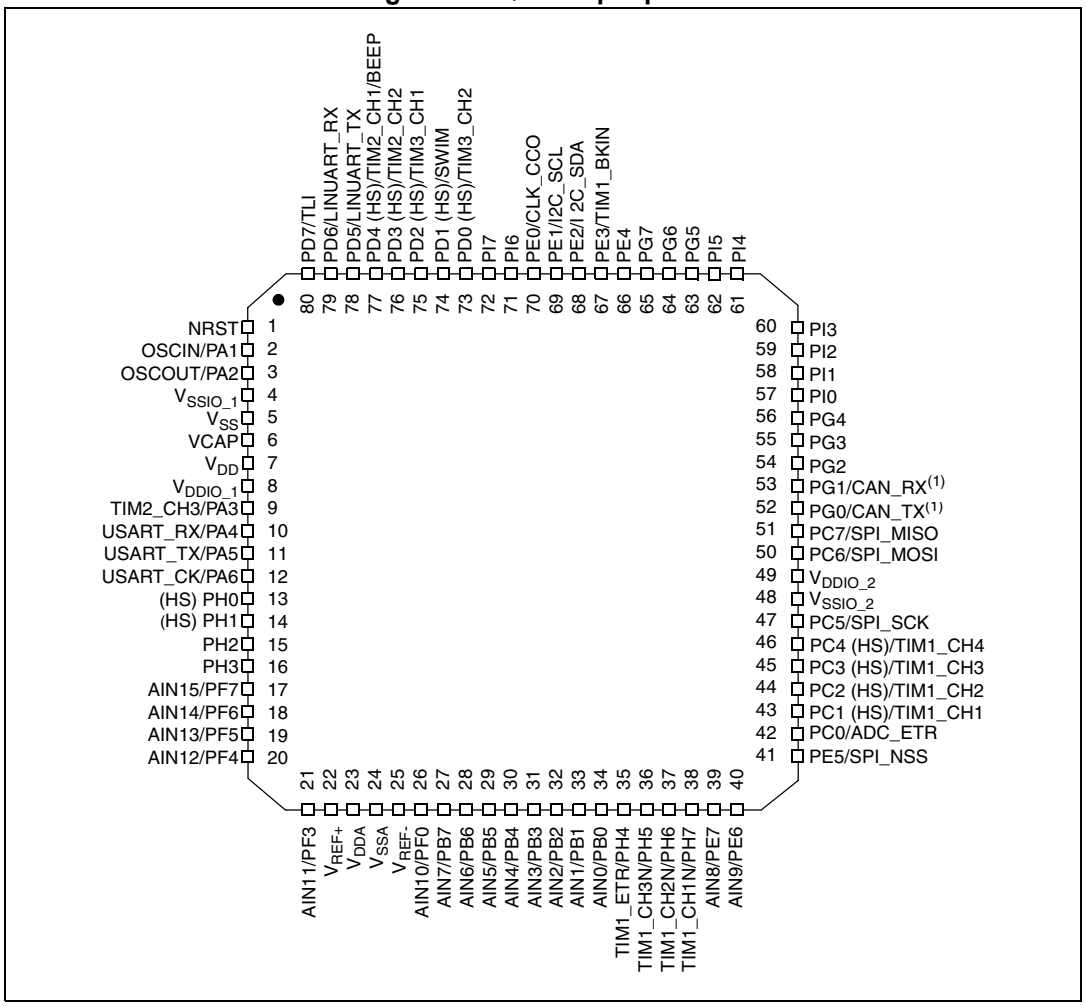
The devices covered by this datasheet contain one I^2C interface. The interface is available on all the supported packages.

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. (HS) stands for high sink capability.

Table 12. Memory model 128K

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
128 K	0x00 27FFF	6 K	0x00 17FF	0x00 1400
64 K	0x00 17FFF			
32 K	0x00 0FFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 13. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215				
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	-	-0.3 V		0.3 x V_{DD}	V
V_{IH}	High-level input voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	0.1 x V_{DD}	-	
V_{OH}	High-level output voltage	Standard I/0, V_{DD} = 5 V, I = 3 mA	V_{DD} - 0.5 V	-	-	
		Standard I/0, V_{DD} = 3 V, I = 1.5 mA	V_{DD} - 0.4 V	-	-	
V_{OL}	Low-level output voltage	High sink and true open drain I/0, V_{DD} = 5 V I = 8 mA	-	-	0.5	V
		Standard I/0, V_{DD} = 5 V I = 3 mA	-	-	0.6	
		Standard I/0, V_{DD} = 3 V I = 1.5 mA	-	-	0.4	
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	35	50	65	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
		Fast I/Os Load = 20 pF	-	-	20(2)	
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
$I_{lkg\ ana}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 125 °C	-	-	±250	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 150 °C	-	-	±500	
$I_{lkg(inj)}$	Leakage current in adjacent I/O(3)	Injection current ±4 mA	-	-	±1(3)	µA
I_{DDIO}	Total current on either V_{DDIO} or V_{SSIO}	Including injection currents	-	-	60	mA

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

10.3.10 I²C interface characteristics

Table 42. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} 3 V to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} 3 V to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

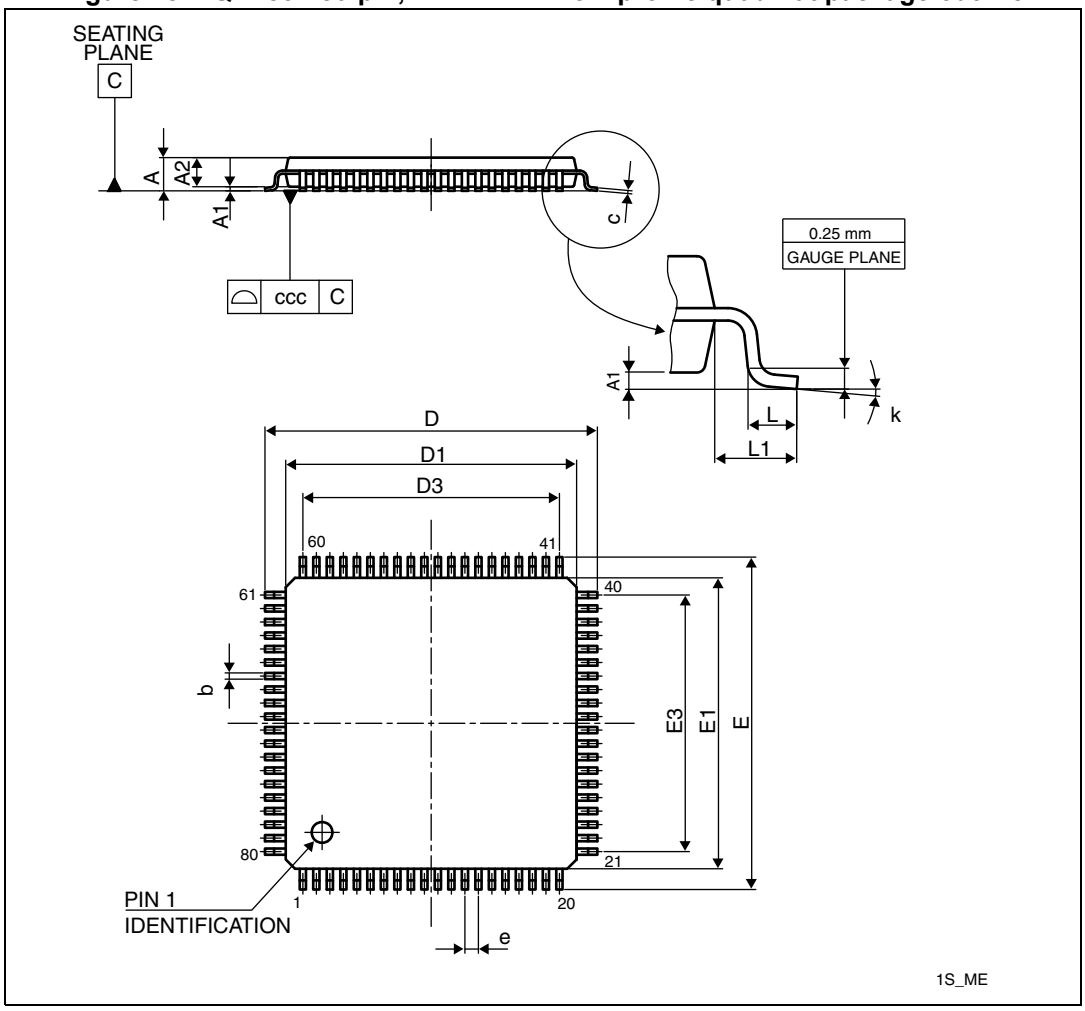
1. Guaranteed by characterization results, not tested in production

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

11.1 LQFP80 package information

Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



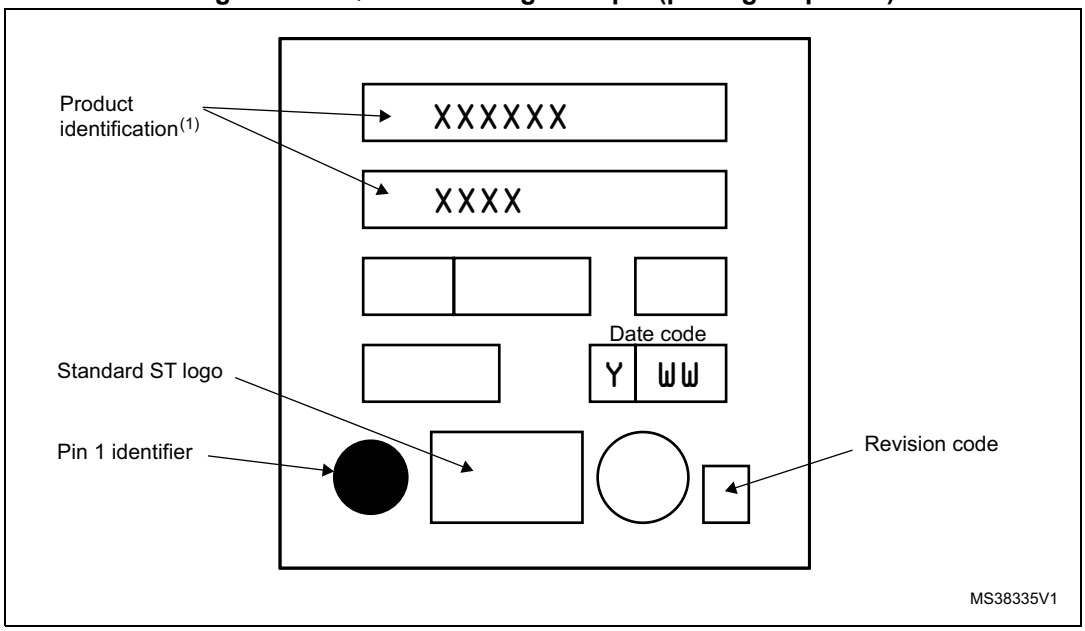
1. Drawing is not to scale.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. LQFP48 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	Added 'H' products to the datasheet (Flash no EEPROM). *Section : Features* on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1. *Table 1: Device summary*: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166. *Section 1: Introduction*, *Section 5: Product overview*, *Section 9: Option bytes*, *Section 6.2: Alternate function remapping*, *Table 21: Current characteristics:* Updated reference documentation: RM0009, PM0047, and UM0470. *Section 2: Description*: added information about peak performance. *Section 3: Product line-up*: Removed *STM8A common features* table. *Table 4: Peripheral clock gating bits (CLK_PCKENR1):* Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T. *Table 5: Peripheral clock gating bits (CLK_PCKENR2)*: Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T. *Section 5: Product overview*: Made minor content changes and improved readability and layout. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: Major modification, TMU included. *Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI)*: User trimming updated. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: LSI as CPU clock added. *Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE)*, *Section 5.5.5: External clock input*: Maximum frequency conditional 32 Kbyte/128 Kbyte. *Section 5.8: Analog to digital converter (ADC)*: Scan for 128 Kbyte removed. *Section 5.9: Communication interfaces*, *Section 5.9.3: Serial peripheral interface (SPI)*: SPI 10 Mb/s. *Figure 3: LQFP 80-pin pinout*, *Figure 4: LQFP 64-pin pinout*, *Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout*: Amended footnote 1. *Table 12: Memory model 128K:* HS output changed from 20 mA to 8 mA. *Section 7: Memory and register map*: Corrected *Table 8: Register and memory map*; removed address list; added *Table 14: General hardware register map*. *Section 10.3.2: Supply current characteristics* Note on typical/WC values added.

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	Replaced the salestype 'STM8H61xx' with 'STM8AH61xx on the first page. Added 'part numbers' to heading rows of *Table 1: Device summary*. Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD. *Table 18*: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]' *Section 9*: Updated introductory text concerning option bytes which do not need to be saved in a complementary form. *Table 18*: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively. *Table 21*: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'. Updated 80-pin package information in line with POA 0062342-revD in *Figure 45* and *Table 53*.
01-Jul-2009	4	Added 'STM8AH61xx' and 'STM8AH51xx to document header. Updated *: Features on page 1* (memories, timers, operating temperature, ADC and I/Os). Updated *Table 1: Device summary* Updated Kbyte value of program memory in *Section: Introduction* Changed the first two lines from the top in *Section: Description*. Updated *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram* Updated *Section 5: Product overview* In *Figure 5: LQFP 48-pin pinout*, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively. *Section 6: Pinouts and pin description:* deleted the text below the *Table 10: Legend/abbreviation for the pin description table* *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description:* 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote. Updated *Figure 8: Register and memory map*. *Table 12: Memory model 128K:* updated footnote Deleted the *Table: Stack and RAM partitioning* *Table 17: STM8A interrupt table*: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote Updated *Section 7: Memory and register map* Updated *Table: Data memory, Table: I/O static characteristics,* and *Table 39: NRST pin characteristics*. *Section 10.1.1: Minimum and maximum values:* added ambient temperature T_A = -40 °C Updated *Table 20: Voltage characteristics*. Updated *Table 21: Current characteristics*. Updated *Table 22: Thermal characteristics*. Updated *Table 24: General operating conditions*.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8 (continued)	Removed note 1 in *Table 24: General operating conditions* and note 1 below *Figure 11: fCPUmax versus VDD*. Removed note 3 in *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C*. Removed note 2 in *Table 31: HSE external clock characteristics* and *Table 35: Flash program memory/data EEPROM memory* Removed note 1 in *Table 37: Data memory*. Modified T_{WE} maximum value in *Table 36: Flash program memory* and *Table 37: Data memory*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table 39: NRST pin characteristics*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 39: Recommended reset pin protection,* and updated external capacitor value. Updated *Note 1* in *Table 40: TIM 1, 2, 3, and 4 electrical specifications.* Updated *Note 1* in *Table 41: SPI characteristics.* Moved know limitations to separate errata sheet. Added “not recommended for new design” note to device family 51, memory size 7 and 9, and temperature range B, in *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added Raisonance compiler in *Section 13.2: Software tools.*
18-Jul-2012	9	Updated wildcards of document part numbers. Added VFQFPN package. Added STM8AF62A6 part number. *Table 1: Device summary* updated footnote *1* and added footnote *2*. *Table: STM8AF52xx product line-up with CAN* and *Table: STM8AF62xx product line-up without CAN*: added “P” version for all order codes; updated size of data EEPROM for 64K devices to 2K instead of 1.5K; updated RAM. *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram*: updated POR, BOR and WDG; removed PDR; added legend. *Section 5.4: Flash program and data EEPROM*: removed non relevant bullet points and added a sentence about the factory program. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)* and updated *Table 5: Peripheral clock gating bits (CLK_PCKENR2)* *Section : ADC features*: updated ADC input range. *Table 12: Memory model 128K:* updated RAM size, RAM end addresses, and stack roll-over addresses; updated footnote *1* *Table 18: Option bytes:* updated factory default setting for NOPT17; updated footnotes. *Table 20: Voltage characteristics:* updated V_{DDX} - V_{DD} to V_{DDX} - V_{SS}. *Table 24: General operating conditions:* updated V_{CAP}.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-Jul-2012	9 (continued)	*Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* updated conditions for $I_{DD(RUN)}$. *Table 38: I/O static characteristics:* added new condition and new max values for rise and fall time; updated footnote 2. *Section 10.3.7: Reset pin characteristics:* updated text below *Figure 38: Typical NRST pull-up current Ipu vs VDD* *Figure 39: Recommended reset pin protection:* updated unit of capacitor. *Table 41: SPI characteristics:* updated SCK high and low time conditions and values. *Figure 42: SPI timing diagram - master mode:* replaced 'SCK input' signals with 'SCK output' signals. Updated *Table 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data* Replaced *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* Added *Figure 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint* *and* *Figure 55: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* Updated *Figure 57: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline* Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1* *Section 13.2.2: C and assembly toolchains:* added www.iar.com.
31-Mar-2014	10	Updated: – *Table 1: Device summary*, – *Table: STM8AF52xx product line-up with CAN*, – *Table: STM8AF/H/P51xx product line-up with CAN*, – *Table: STM8AF/H/P61xx product line-up without CAN*, – *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*, – The maximum speed in *Section 5.9.3: Serial peripheral interface (SPI)*, – t_{TEMP} Reset release delay /VDD rising typical and max values in *Table 25: Operating conditions at power-up/power-down*, – The symbol $t_{IFP(NRST)}$ with $t_{INFP(NRST)}$ in *Table 39: NRST pin characteristics*, – The address and comment for Reset in *Table 17: STM8A interrupt table*.

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Oct-2016	14	Updated: – Title of *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout*, (previously STM8AF5286UC VFQFPN32 32-pin pinout) – Footnotes of *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1* – *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* replaced “STM8AF5286UC VQFPN32” with “STM8AF52x6 VQFPN32” at header row – *Section 10.2: Absolute maximum ratings* – *Section : Device marking on page 93* – *Section : Device marking on page 96* – *Section : Device marking on page 99* – *Section : Device marking on page 104* – *Section : Device marking on page 108* Added: – Footnote on *Figure 47: LQFP80 marking example (package top view)*, *Figure 50: LQFP64 marking example (package top view)*, *Figure 56: LQFP32 marking example (package top view)*, *Figure 59: VFQFPN32 marking example (package top view)*.
10-Nov-2016	15	Updated header row and PA6/USART_CK pin row on *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*.