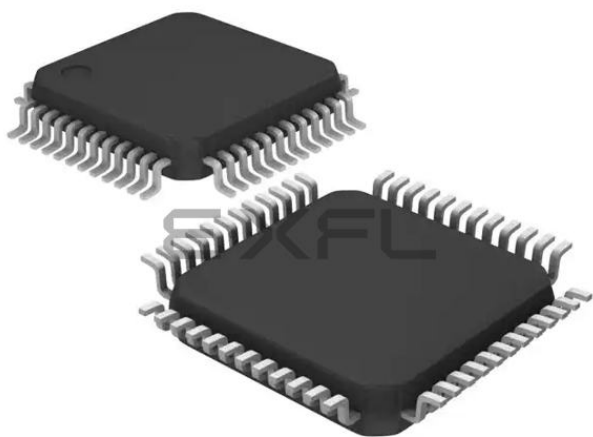




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Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5288tax

3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	128 K	52/36						
STM8AF/P5289	64 K							
STM8AF/P5269	32 K							
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K						
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I²C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins		
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I ² C	68/37		
STM8AF/P628A		64 K								
STM8AF/P62A9	128 K	2 K								
STM8AF/P6289	64 K			1 K						
STM8AF/P6269	32 K									
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I ² C	38/35
STM8AF/P6288										
STM8AF/P6286	LQFP32 (7x7)	64 K			7					
STM8AF/P62A6	VFQFPN32 (5x5)	128 K								

5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see [Table 8](#)).

Table 8. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC2

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{\text{SSA}} \leq V_{\text{IN}} \leq V_{\text{DDA}}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see [Table 9](#)).

Table 9. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
USART	UART1
LINUART	UART3

5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

- Interrupt:
 - Successful address/data communication
 - Error condition
 - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

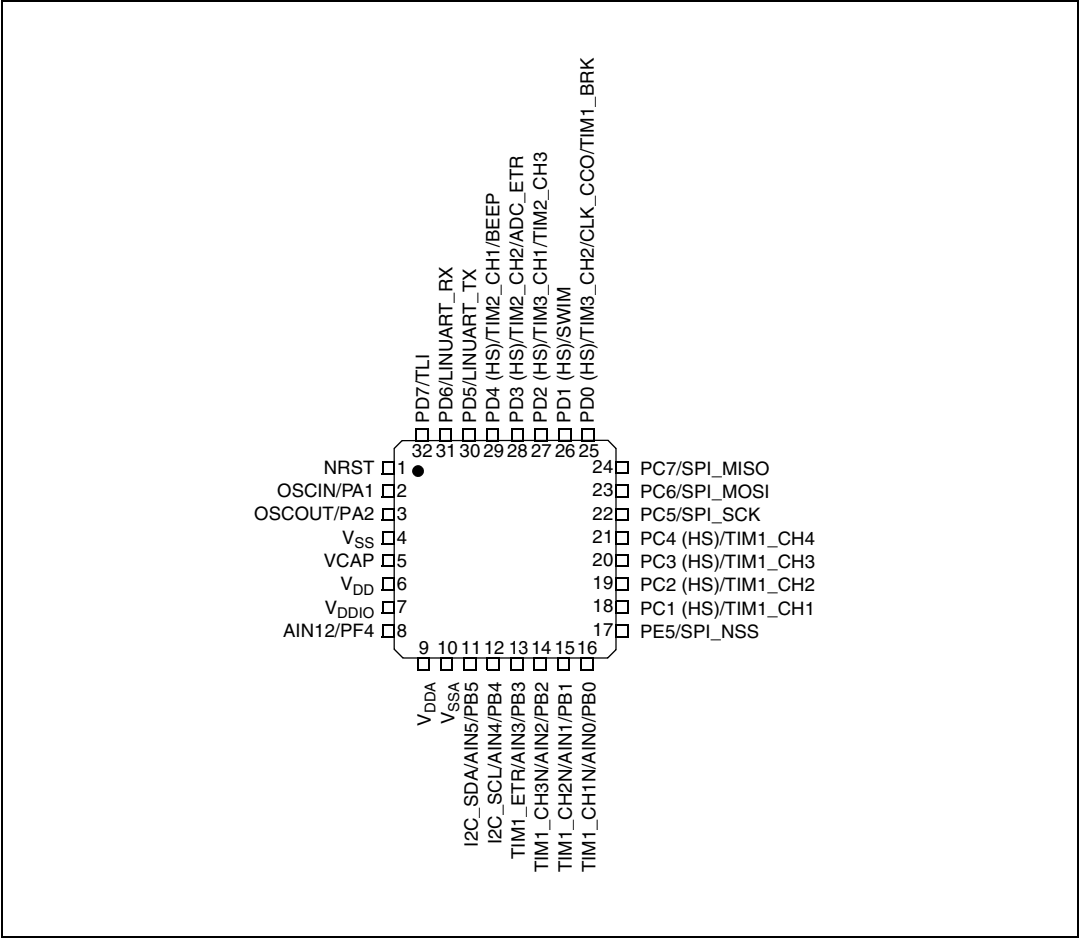
Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
 - Mask mode permitting ID range filtering
 - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout



1. HS stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input				Output			Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VQFPN32	STM8AF52xx6 VQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
55	46	-	-	-	PG3	I/O	X	X	-	-	O1	X	X	Port G3	-	-
56	47	-	-	-	PG4	I/O	X	X	-	-	O1	X	X	Port G4	-	-
57	48	-	-	-	PI0	I/O	X	X	-	-	O1	X	X	Port I0	-	-
58	-	-	-	-	PI1	I/O	X	X	-	-	O1	X	X	Port I1	-	-
59	-	-	-	-	PI2	I/O	X	X	-	-	O1	X	X	Port I2	-	-
60	-	-	-	-	PI3	I/O	X	X	-	-	O1	X	X	Port I3	-	-
61	-	-	-	-	PI4	I/O	X	X	-	-	O1	X	X	Port I4	-	-
62	-	-	-	-	PI5	I/O	X	X	-	-	O1	X	X	Port I5	-	-
63	49	-	-	-	PG5	I/O	X	X	-	-	O1	X	X	Port G5	-	-
64	50	-	-	-	PG6	I/O	X	X	-	-	O1	X	X	Port G6	-	-
65	51	-	-	-	PG7	I/O	X	X	-	-	O1	X	X	Port G7	-	-
66	52	-	-	-	PE4	I/O	X	X	X	-	O1	X	X	Port E4	-	-
67	53	37	-	-	PE3/TIM1_BKIN	I/O	X	X	X	-	O1	X	X	Port E3	Timer 1 - break input	-
68	54	38	-	-	PE2/I ² C_SDA	I/O	X	-	X	-	O1	T ⁽³⁾	-	Port E2	I ² C data	-
69	55	39	-	-	PE1/I ² C_SCL	I/O	X	-	X	-	O1	T ⁽³⁾	-	Port E1	I ² C clock	-
70	56	40	-	-	PE0/CLK_CCO	I/O	X	X	X	-	O3	X	X	Port E0	Configurable clock output	-
71	-	-	-	-	PI6	I/O	X	X	-	-	O1	X	X	Port I6	-	-
72	-	-	-	-	PI7	I/O	X	X	-	-	O1	X	X	Port I7	-	-
73	57	41	25	25	PD0/TIM3_CH2	I/O	X	X	X	HS	O3	X	X	Port D0	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	26	PD1/SWIM ⁽⁴⁾	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
75	59	43	27	27	PD2/TIM3_CH1	I/O	X	X	X	HS	O3	X	X	Port D2	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	28	28	PD3/TIM2_CH2	I/O	X	X	X	HS	O3	X	X	Port D3	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	29	PD4/TIM2_CH1/ BEEP	I/O	X	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1	BEEP output [AFR7]

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART	UART1_SR	USART status register	0xC0
0x00 5231		UART1_DR	USART data register	0xFF
0x00 5232		UART1_BRR1	USART baud rate register 1	0x00
0x00 5233		UART1_BRR2	USART baud rate register 2	0x00
0x00 5234		UART1_CR1	USART control register 1	0x00
0x00 5235		UART1_CR2	USART control register 2	0x00
0x00 5236		UART1_CR3	USART control register 3	0x00
0x00 5237		UART1_CR4	USART control register 4	0x00
0x00 5238		UART1_CR5	USART control register 5	0x00
0x00 5239		UART1_GTR	USART guard time register	0x00
0x00 523A		UART1_PSCR	USART prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	LINUART	UART3_SR	LINUART status register	0xC0
0x00 5241		UART3_DR	LINUART data register	0xFF
0x00 5242		UART3_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART3_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART3_CR1	LINUART control register 1	0x00
0x00 5245		UART3_CR2	LINUART control register 2	0x00
0x00 5246		UART3_CR3	LINUART control register 3	0x00
0x00 5247		UART3_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			

8 Interrupt table

Table 17. STM8A interrupt table⁽¹⁾

Priority	Source block	Description	Interrupt vector address	Wakeup from Halt	Comments
-	Reset	Reset	0x00 8000	Yes	-
-	TRAP	SW interrupt	0x00 8004	-	-
0	TLI	External top level interrupt	0x00 8008	-	-
1	AWU	Auto-wakeup from Halt	0x00 800C	Yes	-
2	Clock controller	Main clock controller	0x00 8010	-	-
3	MISC	External interrupt E0	0x00 8014	Yes	Port A interrupts
4	MISC	External interrupt E1	0x00 8018	Yes	Port B interrupts
5	MISC	External interrupt E2	0x00 801C	Yes	Port C interrupts
6	MISC	External interrupt E3	0x00 8020	Yes	Port D interrupts
7	MISC	External interrupt E4	0x00 8024	Yes	Port E interrupts
8	CAN	CAN interrupt Rx	0x00 8028	Yes	-
9	CAN	CAN interrupt TX/ER/SC	0x00 802C	-	-
10	SPI	End of transfer	0x00 8030	Yes	-
11	Timer 1	Update/overflow/ trigger/break	0x00 8034	-	-
12	Timer 1	Capture/compare	0x00 8038	-	-
13	Timer 2	Update/overflow	0x00 803C	-	-
14	Timer 2	Capture/compare	0x00 8040	-	-
15	Timer 3	Update/overflow	0x00 8044	-	-
16	Timer 3	Capture/compare	0x00 8048	-	-
17	USART	Tx complete	0x00 804C	-	-
18	USART	Receive data full reg.	0x00 8050	-	-
19	I ² C	I ² C interrupts	0x00 8054	Yes	-
20	LINUART	Tx complete/error	0x00 8058	-	-
21	LINUART	Receive data full reg.	0x00 805C	-	-
22	ADC	End of conversion	0x00 8060	-	-
23	Timer 4	Update/overflow	0x00 8064	-	-
24	EEPROM	End of programming/ write in not allowed area	0x00 8068	-	-

1. All unused interrupts must be initialized with 'IRET' for robust programming.

Table 18. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 480B	TMU	OPT6	TMU[3:0]								0x00
0x00 480C		NOPT6	NTMU[3:0]								0xFF
0x00 480D	Flash wait states	OPT7	Reserved						WAIT STATE	0x00	
0x00 480E		NOPT7	Reserved						NWAIT STATE	0xFF	
0x00 480F	Reserved										
0x00 4810	TMU	OPT8	TMU_KEY 1 [7:0]								0x00
0x00 4811		OPT9	TMU_KEY 2 [7:0]								0x00
0x00 4812		OPT10	TMU_KEY 3 [7:0]								0x00
0x00 4813		OPT11	TMU_KEY 4 [7:0]								0x00
0x00 4814		OPT12	TMU_KEY 5 [7:0]								0x00
0x00 4815		OPT13	TMU_KEY 6 [7:0]								0x00
0x00 4816		OPT14	TMU_KEY 7 [7:0]								0x00
0x00 4817		OPT15	TMU_KEY 8 [7:0]								0x00
0x00 4818		OPT16	TMU_MAXATT [7:0]								0xC7
0x00 4819 to 487D	Reserved										
0x00 487E	Boot-loader ⁽¹⁾	OPT17	BL [7:0]								0x00
0x00 487F		NOPT 17	NBL [7:0]								0xFF

1. This option consists of two bytes that must have a complementary value in order to be valid. If the option is invalid, it has no effect on EMC reset.

Table 19. Option byte description

Option byte no.	Description
OPT0	ROP[7:0]: Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) <i>Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</i>
OPT1	UBC[7:0]: User boot code area 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0xFF: Pages 4 to 255 defined as UBC, memory write-protected <i>Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.</i>
OPT2	AFR7: Alternate function remapping option 7 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP AFR6: Alternate function remapping option 6 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I ² C_SDA, port B4 alternate function = I ² C_SCL. AFR5: Alternate function remapping option 5 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. AFR4: Alternate function remapping option 4 0: Port D7 alternate function = TLI 1: Reserved AFR3: Alternate function remapping option 3 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN AFR2: Alternate function remapping option 2 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO <i>Note: AFR2 option has priority over AFR3 if both are activated</i> AFR1: Alternate function remapping option 1 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. AFR0: Alternate function remapping option 0 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Current consumption curves

Figure 13 to Figure 18 show typical current consumption measured with code executing in RAM.

Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = on

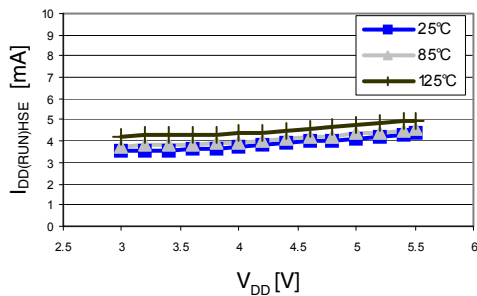


Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU}
@ $V_{DD} = 5.0$ V, peripherals = on

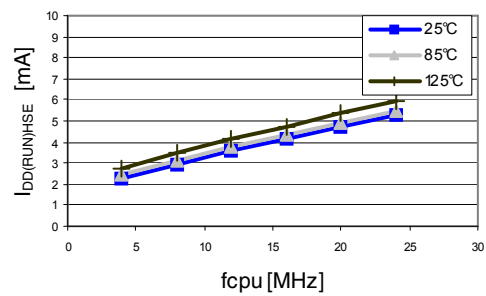


Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = off

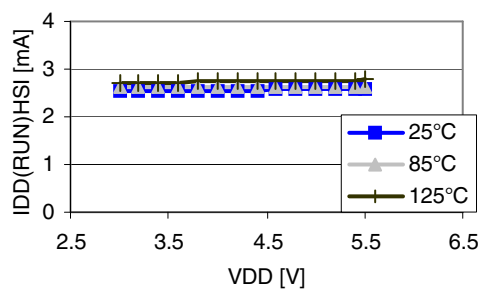


Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = on

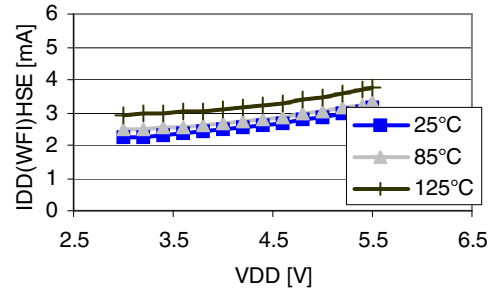


Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU}
@ $V_{DD} = 5.0$ V, peripherals = on

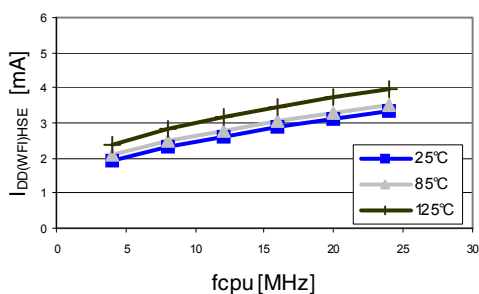
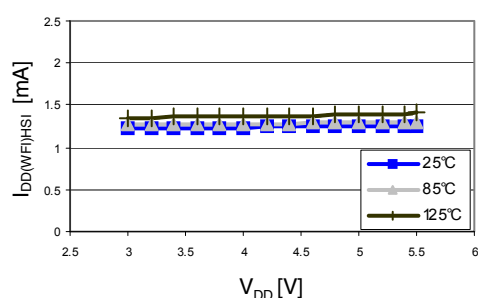


Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = off



10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

High-speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} = 3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 150\text{ }^{\circ}\text{C}$	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2 ⁽¹⁾	μs

1. Guaranteed by characterization results, not tested in production.

Figure 21. Typical HSI frequency vs V_{DD}

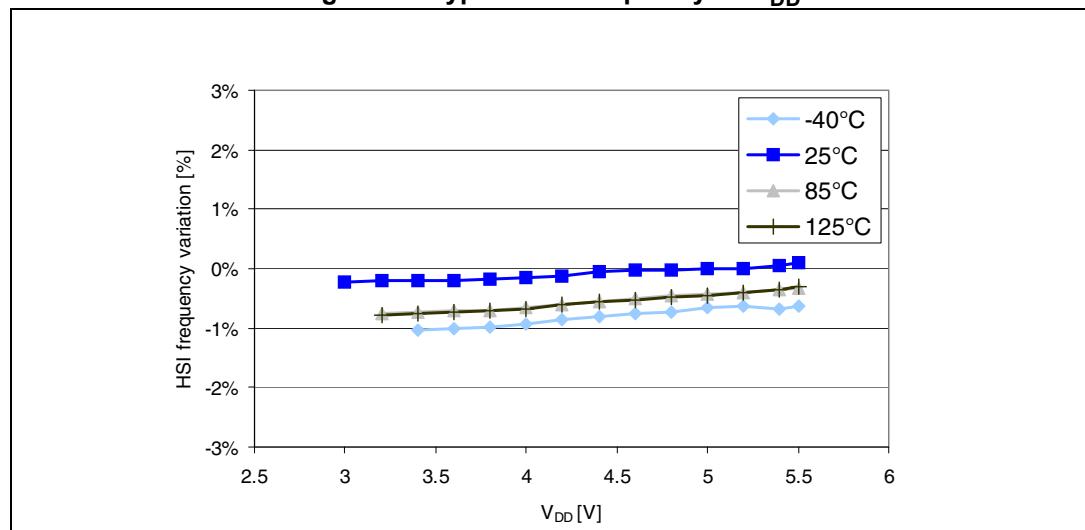
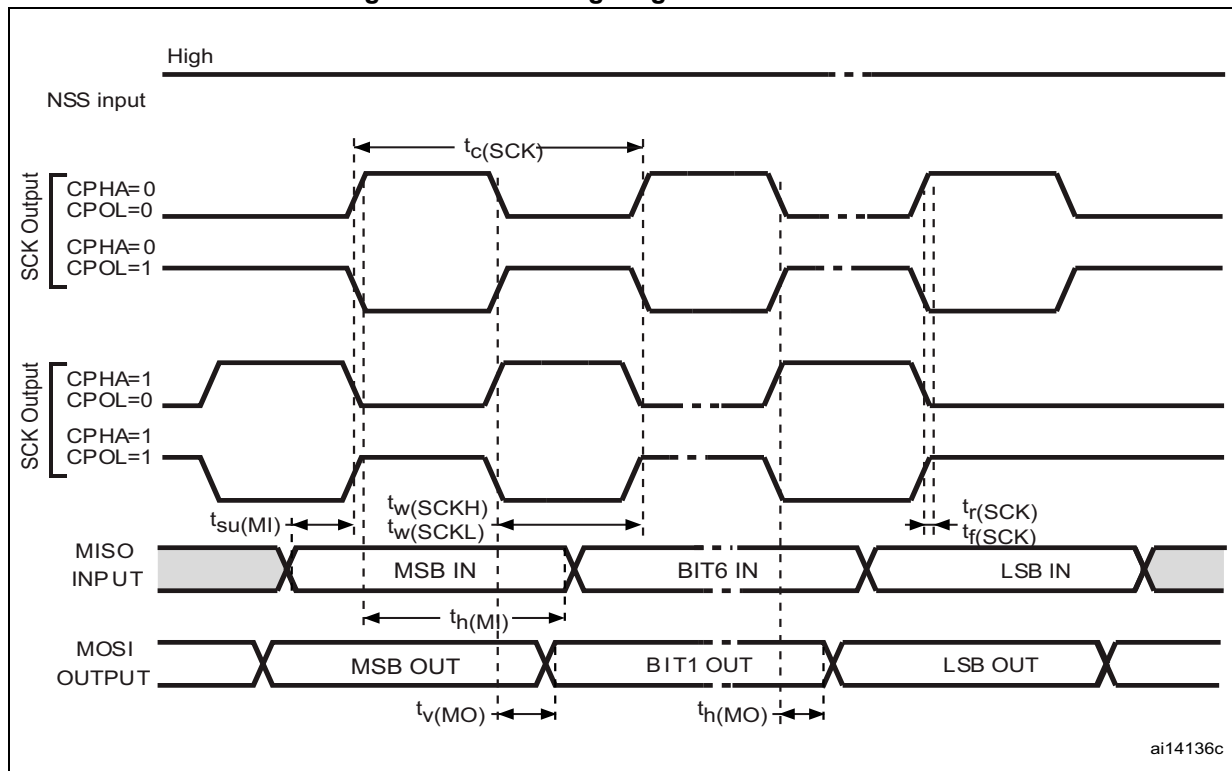


Figure 42. SPI timing diagram - master mode



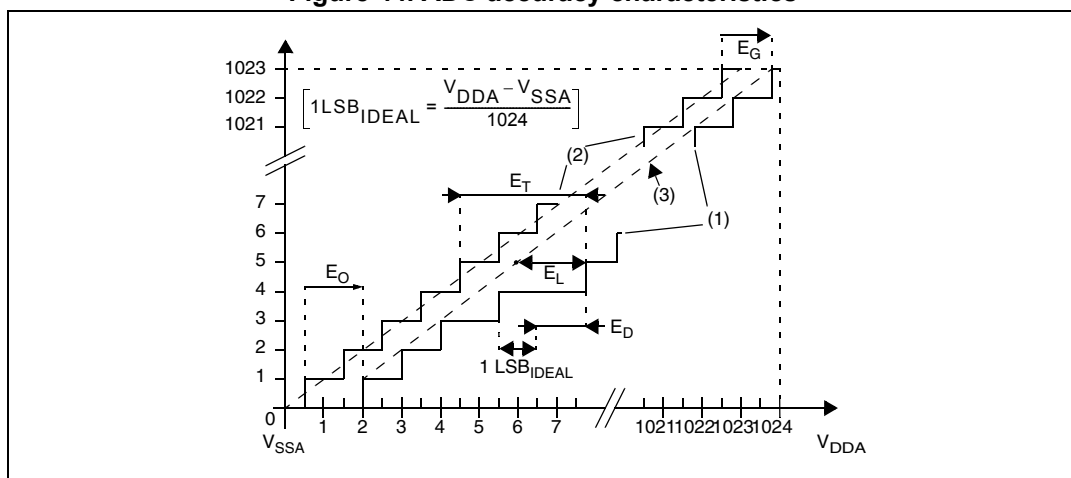
1. Measurement points are at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Table 44. ADC accuracy for $V_{DDA} = 5\text{ V}$

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$ E_T $	Total unadjusted error ⁽²⁾	$f_{\text{ADC}} = 2\text{ MHz}$	1.4	3 ⁽³⁾	LSB
$ E_O $	Offset error ⁽²⁾		0.8	3	
$ E_G $	Gain error ⁽²⁾		0.1	2	
$ E_D $	Differential linearity error ⁽²⁾		0.9	1	
$ E_L $	Integral linearity error ⁽²⁾		0.7	1.5	
$ E_T $	Total unadjusted error ⁽²⁾	$f_{\text{ADC}} = 4\text{ MHz}$	1.9 ⁽⁴⁾	4 ⁽⁴⁾	
$ E_O $	Offset error ⁽²⁾		1.3 ⁽⁴⁾	4 ⁽⁴⁾	
$ E_G $	Gain error ⁽²⁾		0.6 ⁽⁴⁾	3 ⁽⁴⁾	
$ E_D $	Differential linearity error ⁽²⁾		1.5 ⁽⁴⁾	2 ⁽⁴⁾	
$ E_L $	Integral linearity error ⁽²⁾		1.2 ⁽⁴⁾	1.5 ⁽⁴⁾	

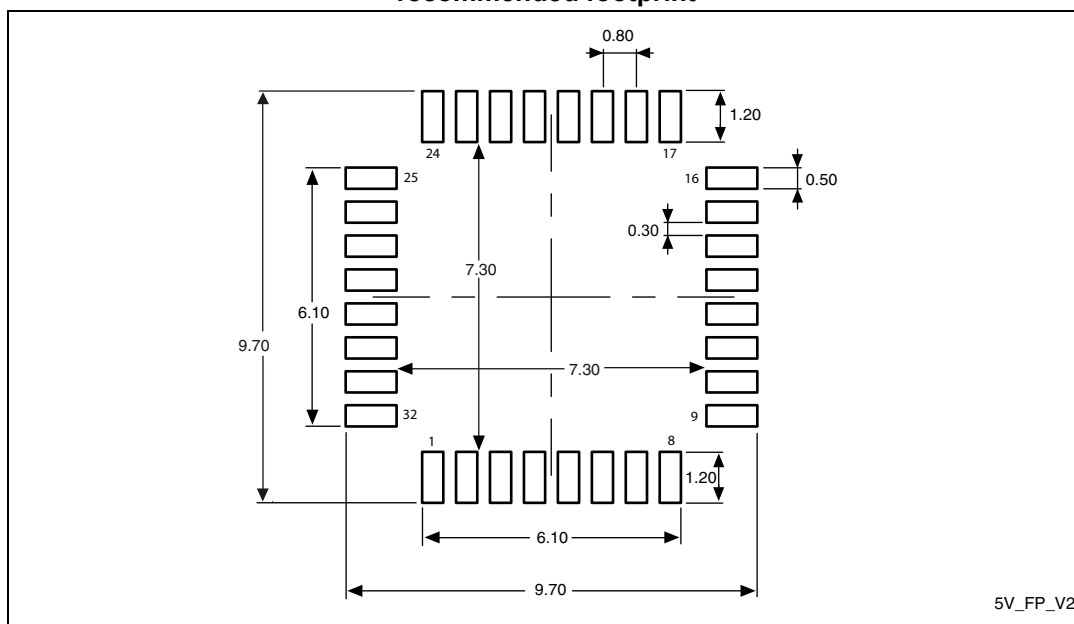
1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{\text{INJ(PIN)}}$ and $\Sigma I_{\text{INJ(PIN)}}$ in [Section 10.3.6](#) does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



1. Example of an actual transfer curve
 2. The ideal transfer curve
 3. End point correlation line
- E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset error: Deviation between the first actual transition and the first ideal one.
 E_G = Gain error: Deviation between the last ideal transition and the last actual one.
 E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
 E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

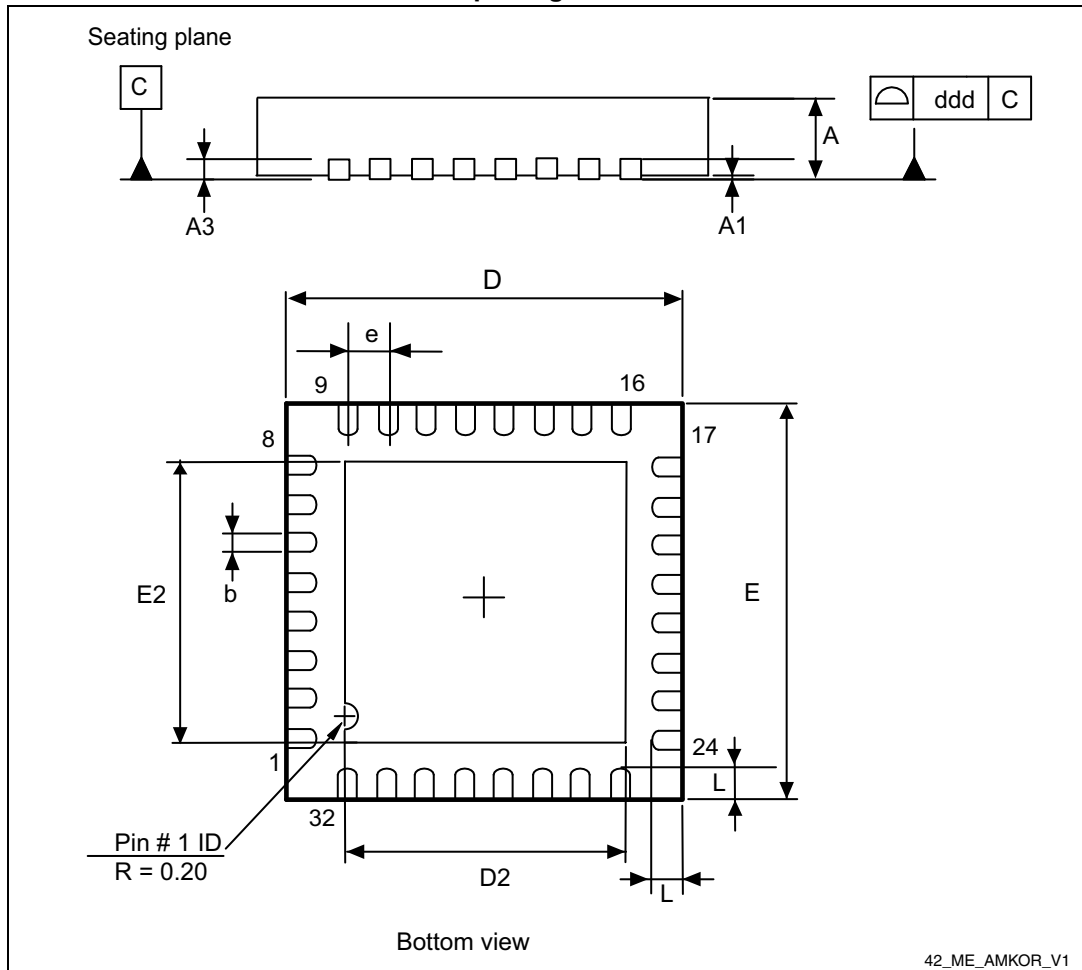
Figure 55. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.5 VFQFPN32 package information

Figure 57. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



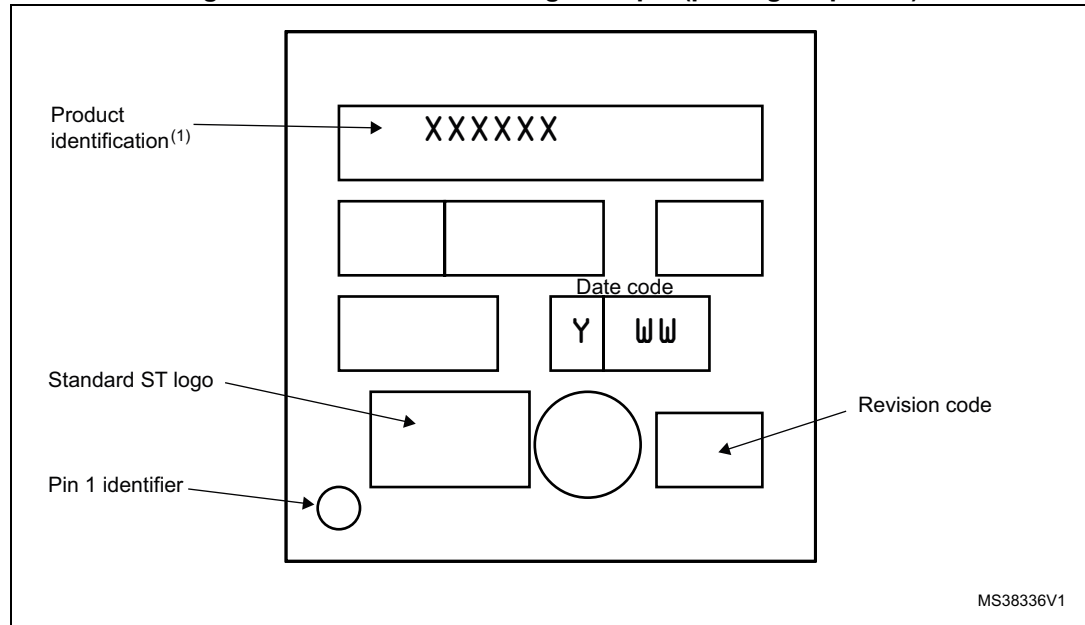
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. VFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

11.6 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in [Table 24: General operating conditions](#) is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} \cdot I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \cdot I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low- and high-level in the application.

Table 54. Thermal characteristics⁽¹⁾

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	25	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12 Ordering information

Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme¹

Example:	STM8A ²	F	62	A	A	T	D	XXX ³	Y
Product class	8-bit automotive microcontroller								
Program memory type	F = Flash + EEPROM P = FASTROM								
Device family	52 = Silicon rev U and rev T, CAN/LIN 62 = Silicon rev U and rev T, LIN only								
Program memory size	6 = 32 Kbyte 8 = 64 Kbyte A = 128 Kbyte								
Pin count	6 = 32 pins 8 = 48 pins 9 = 64 pins A = 80 pins								
Package type	T = LQFP U = VFQFPN								
Temperature range	A = -40 to 85 °C C = -40 to 125 °C D = -40 to 150 °C								
Packing	Y = Tray U = Tube X = Tape and reel compliant with EIA 481-C								

1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.