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Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5288tay

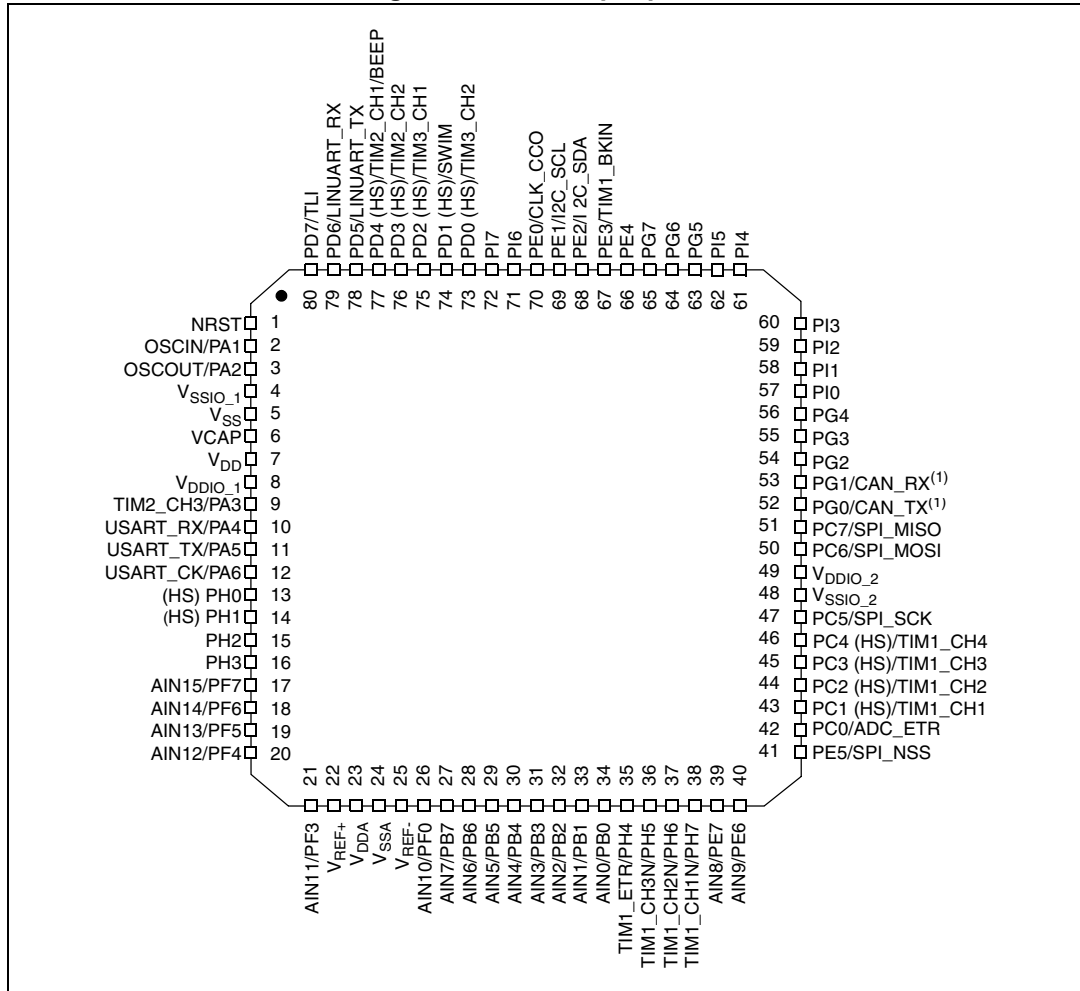
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6 Pinouts and pin description

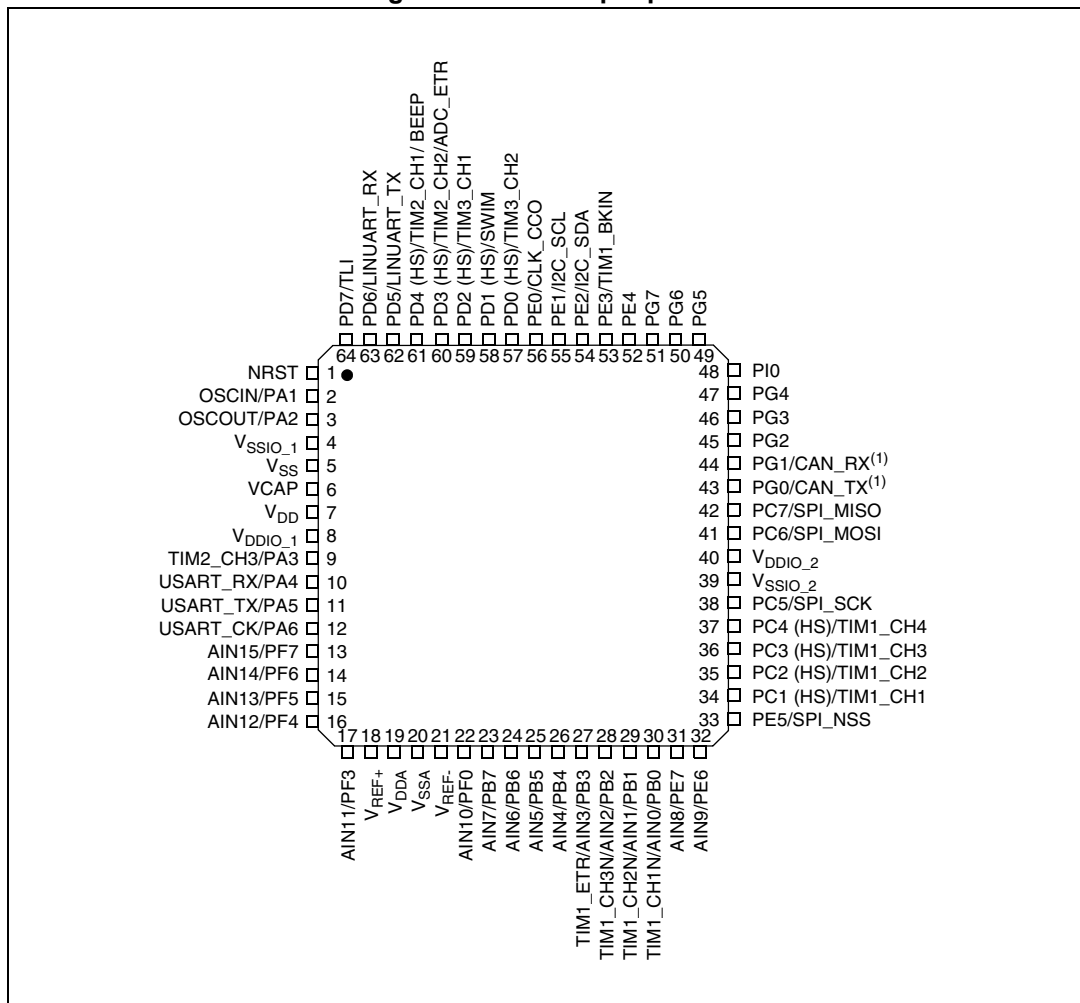
6.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. (HS) stands for high sink capability.

Figure 4. LQFP 64-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Table 10. Legend/abbreviation for the pin description table

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = high sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description

Pin number					Pin name	Type	Input				Output			Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52xx6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O	-	X	-	-	-	-	-	Reset		-
2	2	2	2	2	PA1/OSCIN ⁽¹⁾	I/O	X	X	-	-	O1	X	X	Port A1	Resonator/crystal in	-
3	3	3	3	3	PA2/OSCOOUT	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/crystal out	-
4	4	4	-	-	V _{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	5	5	4	4	V _{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	6	6	5	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	7	7	6	6	V _{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	8	7	7	V _{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
9	9	9	-	-	PA3/TIM2_CH3	I/O	X	X	X	-	O1	X	X	Port A3	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	10	10	-	-	PA4/USART_RX	I/O	X	X	X	-	O3	X	X	Port A4	USART receive	-
11	11	11	-	-	PA5/USART_TX	I/O	X	X	X	-	O3	X	X	Port A5	USART transmit	-
12	12	12	-	8	PA6/USART_CK ⁽²⁾	I/O	X	X	X	-	O3	X	X	Port A6	USART synchro nous clock	-
13	-	-	-	-	PH0	I/O	X	X	-	HS	O3	X	X	Port H0	-	-
14	-	-	-	-	PH1	I/O	X	X	-	HS	O3	X	X	Port H1	-	-
15	-	-	-	-	PH2	I/O	X	X	-	-	O1	X	X	Port H2	-	-
16	-	-	-	-	PH3	I/O	X	X	-	-	O1	X	X	Port H3	-	-
17	13	-	-	-	PF7/AIN15	I/O	X	X	-	-	O1	X	X	Port F7	Analog input 15	-
18	14	-	-	-	PF6/AIN14	I/O	X	X	-	-	O1	X	X	Port F6	Analog input 14	-
19	15	-	-	-	PF5/AIN13	I/O	X	X	-	-	O1	X	X	Port F5	Analog input 13	-
20	16	-	8	-	PF4/AIN12	I/O	X	X	-	-	O1	X	X	Port F4	Analog input 12	-
21	17	-	-	-	PF3/AIN11	I/O	X	X	-	-	O1	X	X	Port F3	Analog input 11	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VQFPN32	STM8AF52x6 VQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V _{REF+}	S	-	-	-	-	-	-	ADC positive reference voltage		-	
23	19	13	9	9	V _{DDA}	S	-	-	-	-	-	-	Analog power supply		-	
24	20	14	10	10	V _{SSA}	S	-	-	-	-	-	-	Analog ground		-	
25	21	-	-	-	V _{REF-}	S	-	-	-	-	-	-	ADC negative reference voltage		-	
26	22	-	-	-	PF0/AIN10	I/O	X	X	-	-	O1	X	X	Port F0	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	X	X	X	-	O1	X	X	Port B7	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	X	X	X	-	O1	X	X	Port B6	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	X	X	X	-	O1	X	X	Port B5	Analog input 5	I ² C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	X	X	X	-	O1	X	X	Port B4	Analog input 4	I ² C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	X	X	X	-	O1	X	X	Port B3	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	X	X	X	-	O1	X	X	Port B2	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	X	X	X	-	O1	X	X	Port B1	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	X	X	X	-	O1	X	X	Port B0	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	X	X	-	-	O1	X	X	Port H4	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	X	X	-	-	O1	X	X	Port H5	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	X	X	-	-	O1	X	X	Port H6	Timer 1 - inverted channel 2	-

Table 12. Memory model 128K

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
128 K	0x00 27FFF	6 K	0x00 17FF	0x00 1400
64 K	0x00 17FFF			
32 K	0x00 0FFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 13. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX ⁽¹⁾
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX ⁽¹⁾
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX ⁽¹⁾
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX ⁽¹⁾
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 13. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX ⁽¹⁾
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX ⁽¹⁾
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX ⁽¹⁾
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX ⁽¹⁾
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX ⁽¹⁾
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

1. Depends on the external circuitry.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			

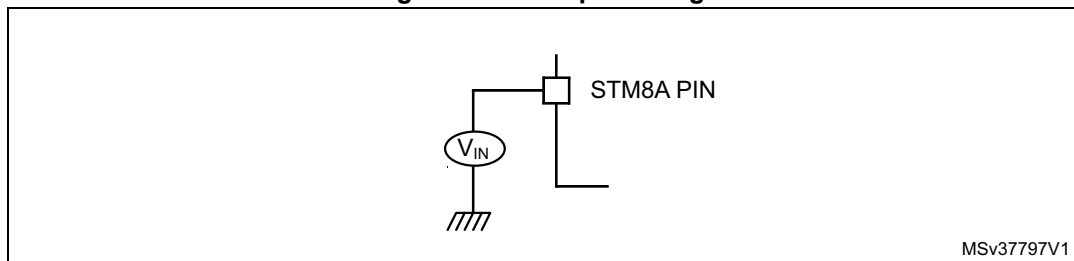
Table 19. Option byte description (continued)

Option byte no.	Description
OPT3	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on Halt 0: No reset generated on Halt if WWDG active 1: Reset generated on Halt if WWDG active
OPT4	EXTCLK: External clock selection 0: External crystal connected to OSCIN/OSCOU 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	HSECNT[7:0]: HSE crystal oscillator stabilization time This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of 0xE1, 0xD2, 0xB4, and 0x00.
OPT6	TMU[3:0]: Enable temporary memory unprotection 0101: TMU disabled (permanent ROP). Any other value: TMU enabled.
OPT7	WAIT STATE: Wait state configuration This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 0: No wait state 1: One wait state
OPT8	TMU_KEY 1 [7:0]: Temporary unprotection key 0 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT9	TMU_KEY 2 [7:0]: Temporary unprotection key 1 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT10	TMU_KEY 3 [7:0]: Temporary unprotection key 2 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT11	TMU_KEY 4 [7:0]: Temporary unprotection key 3 Temporary unprotection key: Must be different from 0x00 or 0xFF

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 10](#).

Figure 10. Pin input voltage



10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 20: Voltage characteristics](#), [Table 21: Current characteristics](#) and [Table 22: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability. The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 20. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V _{DDx} - V _{SS}	Supply voltage (including V _{DDA} and V _{DDIO}) ⁽¹⁾	-0.3	6.5	V
V _{IN}	Input voltage on true open drain pins (PE1, PE2) ⁽²⁾	V _{SS} - 0.3	6.5	
	Input voltage on any other pin ⁽²⁾	V _{SS} - 0.3	V _{DD} + 0.3	
V _{DDx} - V _{DD}	Variations between different power pins	-	50	mV
V _{SSx} - V _{SS}	Variations between all the different ground pins	-	50	
V _{ESD}	Electrostatic discharge voltage	see <i>Absolute maximum ratings (electrical sensitivity) on page 88</i>		

1. All power (V_{DD} , V_{DDIO} , V_{DDA}) and ground (V_{SS} , V_{SSIO} , V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

10.3 Operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	1 wait state $T_A = -40\text{ }^{\circ}\text{C to }150\text{ }^{\circ}\text{C}$	16	24	MHz
		0 wait state $T_A = -40\text{ }^{\circ}\text{C to }150\text{ }^{\circ}\text{C}$	0	16	
$V_{\text{DD}}/V_{\text{DDIO}}$	Standard operating voltage	-	3.0	5.5	V
$V_{\text{CAP}}^{(1)}$	C_{EXT} : capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz ⁽²⁾	-	0.3	Ω
	ESL of external capacitor		-	15	nH
T_A	Ambient temperature	Suffix A	- 40	85	$^{\circ}\text{C}$
		Suffix C		125	
		Suffix D		150	
T_J	Junction temperature range	Suffix A	- 40	90	
		Suffix C		130	
		Suffix D		155	

- Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
- This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.

Figure 11. f_{CPUmax} versus V_{DD}

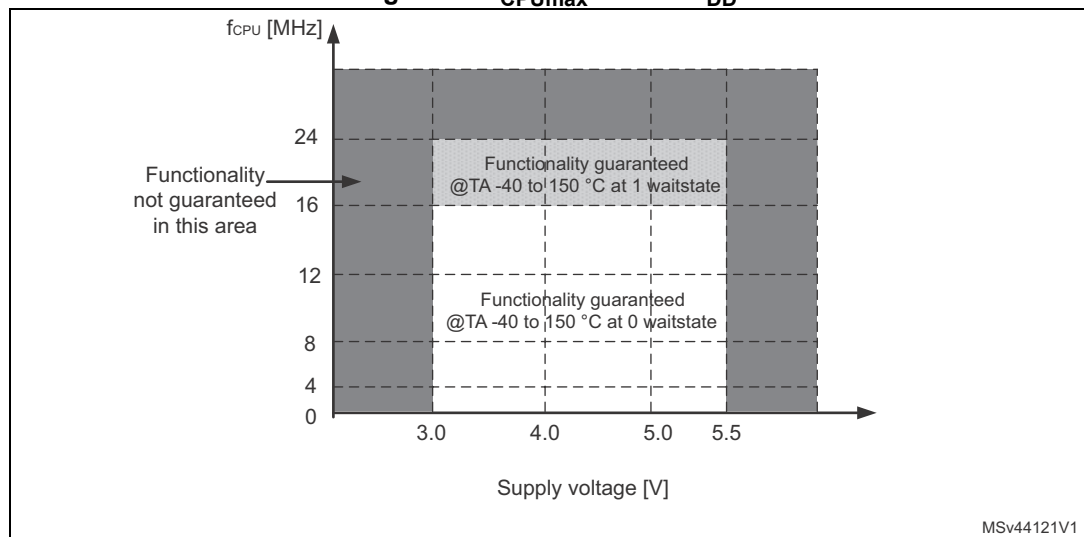


Table 27. Total current consumption in Halt and Active-halt modes. General conditions for V_{DD} applied. $T_A = -40\text{ }^{\circ}\text{C}$ to $55\text{ }^{\circ}\text{C}$ unless otherwise stated

Symbol	Parameter	Conditions			Typ	Max	Unit
		Main voltage regulator (MVR) ⁽¹⁾	Flash mode ⁽²⁾	Clock source and temperature condition			
$I_{DD(H)}$	Supply current in Halt mode	Off	Power-down	Clocks stopped	5	35 ⁽³⁾	μA
				Clocks stopped, $T_A = 25\text{ }^{\circ}\text{C}$	5	25	
$I_{DD(AH)}$	Supply current in Active-halt mode with regulator on	On	Power-down	External clock 16 MHz $f_{\text{MASTER}} = 125\text{ kHz}$	770	900 ⁽³⁾	
				LSI clock 128 kHz	150	230 ⁽³⁾	
	Supply current in Active-halt mode with regulator off	Off	Power-down	LSI clock 128 kHz	25	42 ⁽³⁾	
				LSI clock 128 kHz, $T_A = 25\text{ }^{\circ}\text{C}$	25	30	
$t_{WU(AH)}$	Wakeup time from Active-halt mode with regulator on	On	Operating mode	$T_A = -40\text{ to }150\text{ }^{\circ}\text{C}$	10	30 ⁽³⁾	μs
	Wakeup time from Active-halt mode with regulator off	Off			50	80 ⁽³⁾	

1. Configured by the REGAH bit in the CLK_ICR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.
3. Guaranteed by characterization results, not tested in production.

Current consumption for on-chip peripherals

Table 28. Oscillator current consumption

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(OSC)}$	HSE oscillator current consumption ⁽²⁾	Quartz or ceramic resonator, CL = 33 pF $V_{DD} = 5\text{ V}$	$f_{\text{OSC}} = 24\text{ MHz}$	1	2.0 ⁽³⁾	mA
			$f_{\text{OSC}} = 16\text{ MHz}$	0.6	-	
			$f_{\text{OSC}} = 8\text{ MHz}$	0.57	-	
$I_{DD(OSC)}$	HSE oscillator current consumption ⁽²⁾	Quartz or ceramic resonator, CL = 33 pF $V_{DD} = 3.3\text{ V}$	$f_{\text{OSC}} = 24\text{ MHz}$	0.5	1.0 ⁽³⁾	
			$f_{\text{OSC}} = 16\text{ MHz}$	0.25	-	
			$f_{\text{OSC}} = 8\text{ MHz}$	0.18	-	

1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Informative data.

Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A .

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7 ⁽¹⁾	μs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

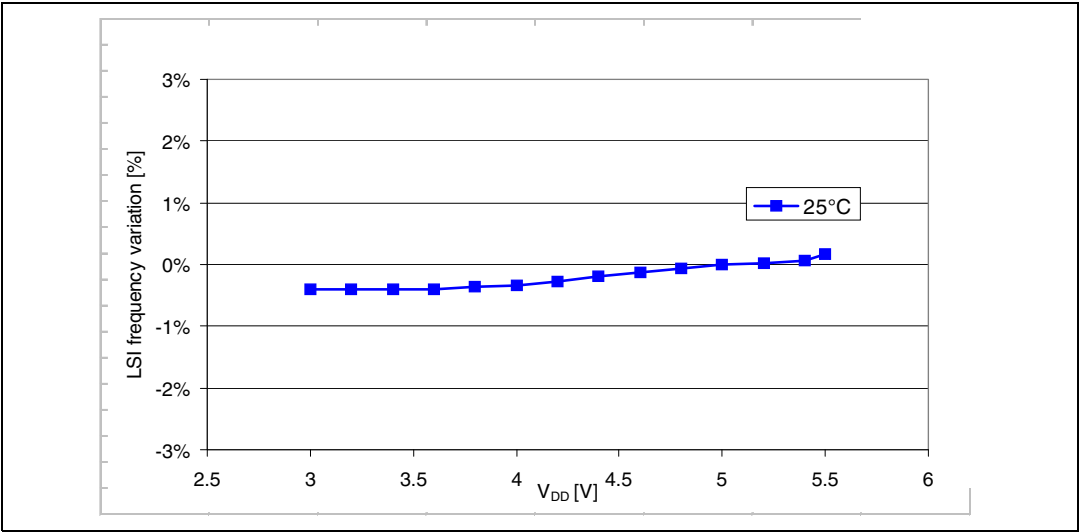
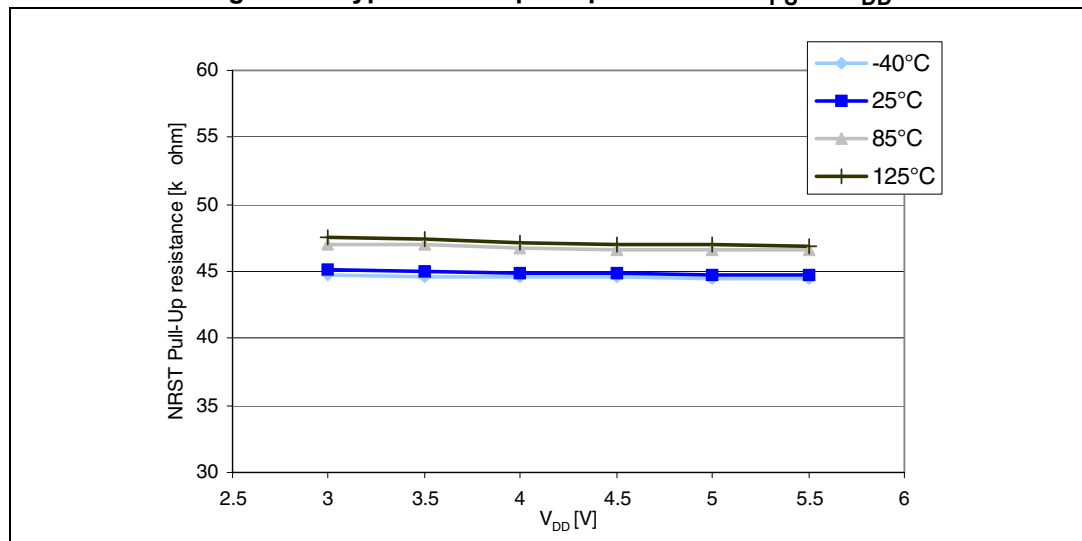
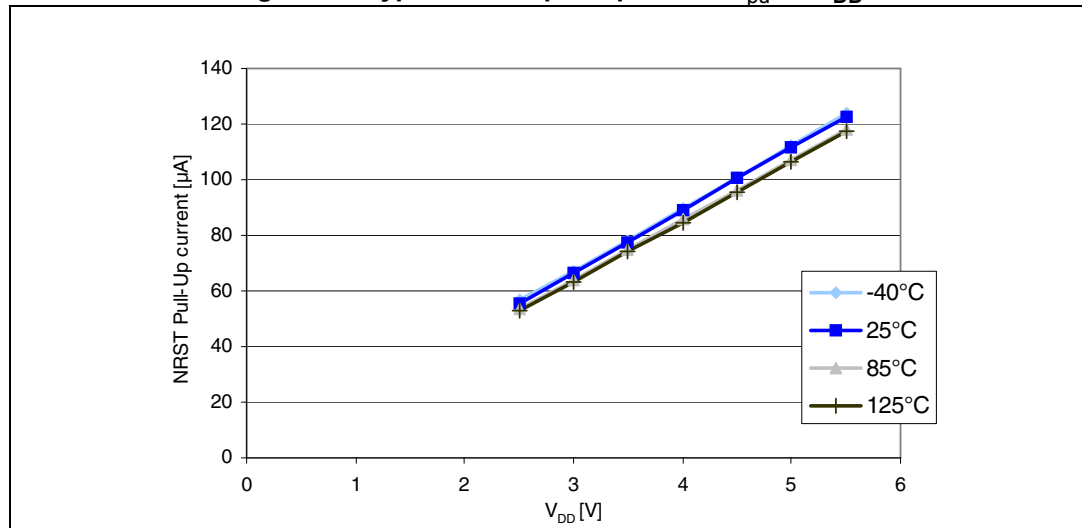


Figure 37. Typical NRST pull-up resistance R_{PU} vs V_{DD} Figure 38. Typical NRST pull-up current I_{PU} vs V_{DD} 

The reset network shown in [Figure 39](#) protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see [Table 39: NRST pin characteristics](#)), otherwise the reset is not taken into account internally.

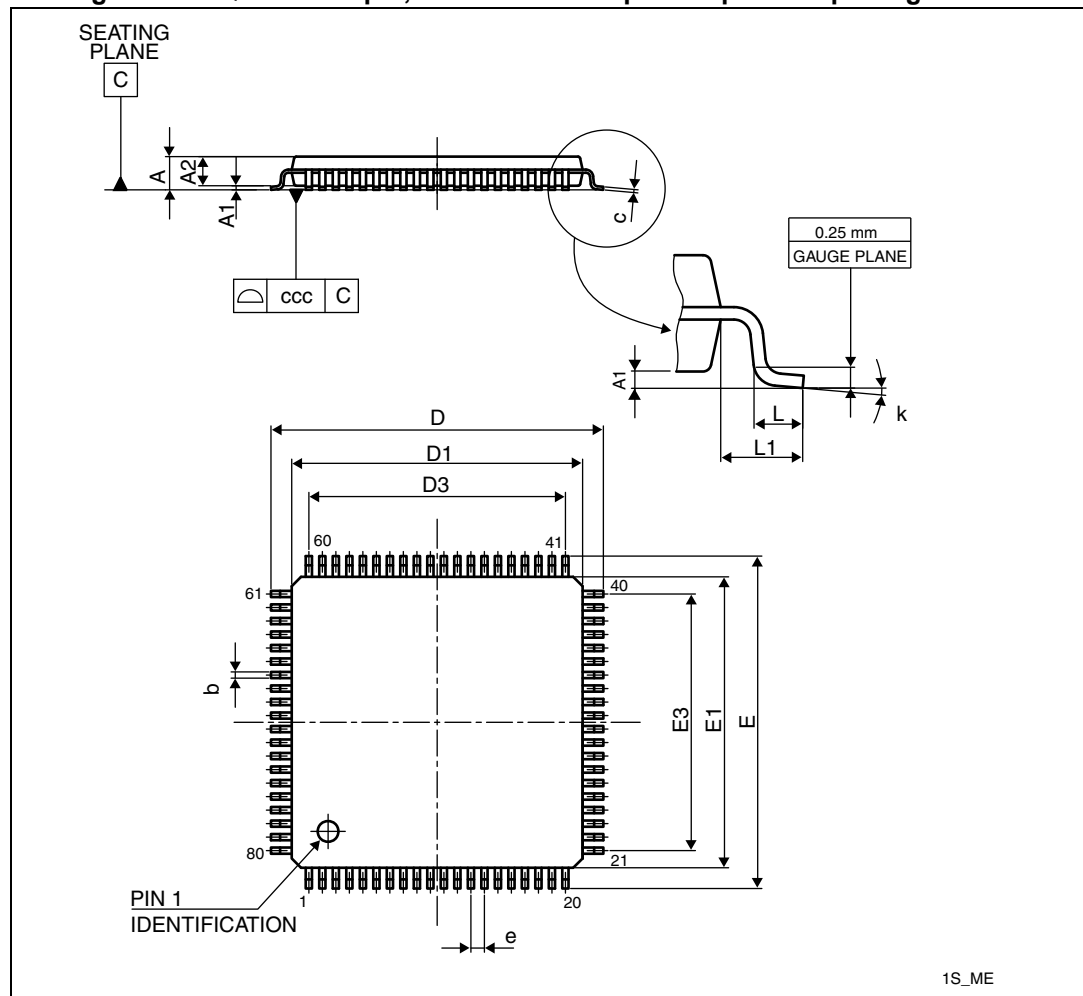
For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 10 nF.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

11.1 LQFP80 package information

Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

**Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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