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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5288tcy

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2 Description

The STM8AF526x/8x/Ax and STM8AF6269/8x/Ax automotive 8-bit microcontrollers described in this datasheet offer from 32 Kbyte to 128 Kbyte of non volatile memory and integrated true data EEPROM. They are referred to as high density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

The STM8AF52 series features a CAN interface.

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, wtachdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

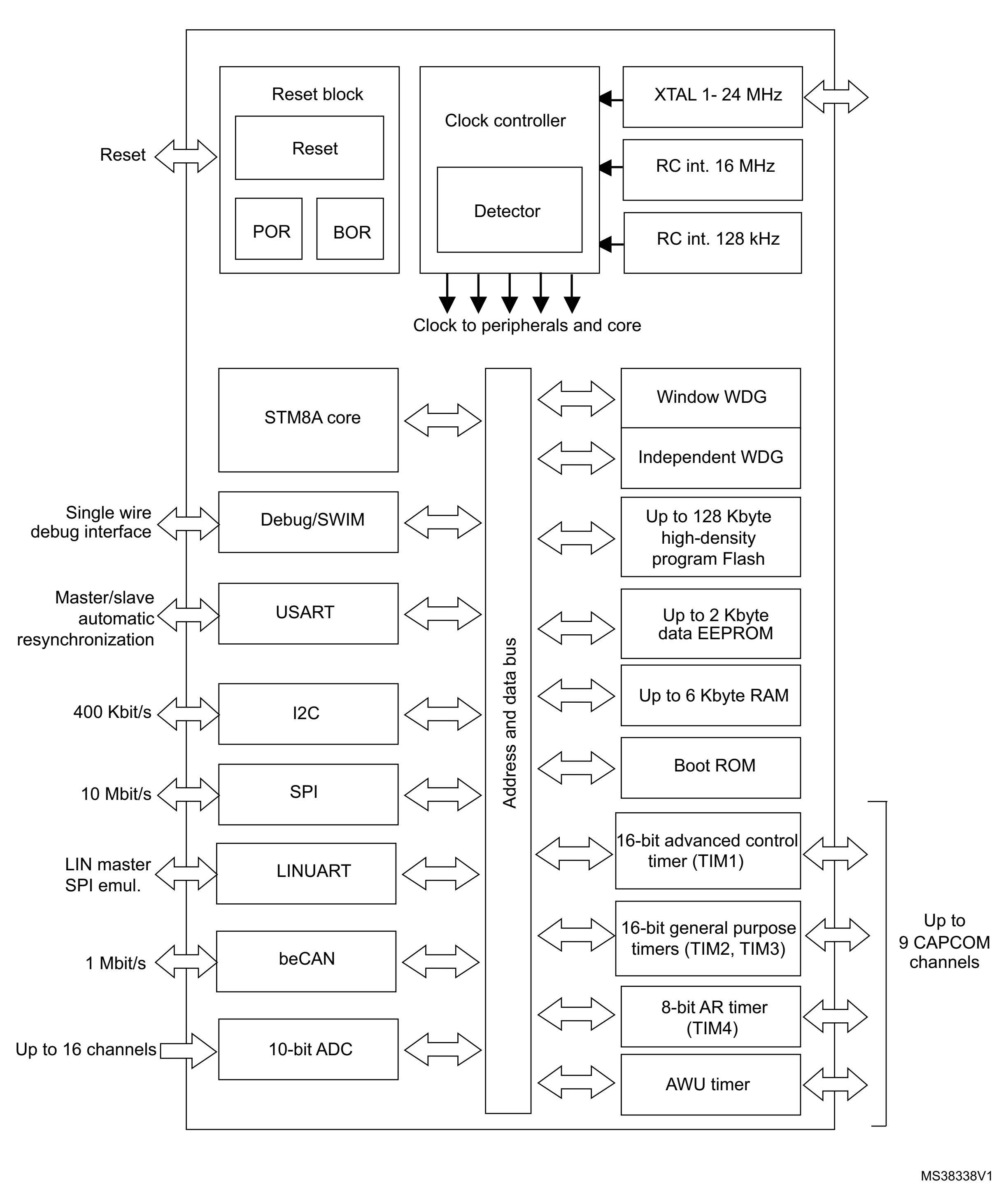
Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map, and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5.5 V operating supply.

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

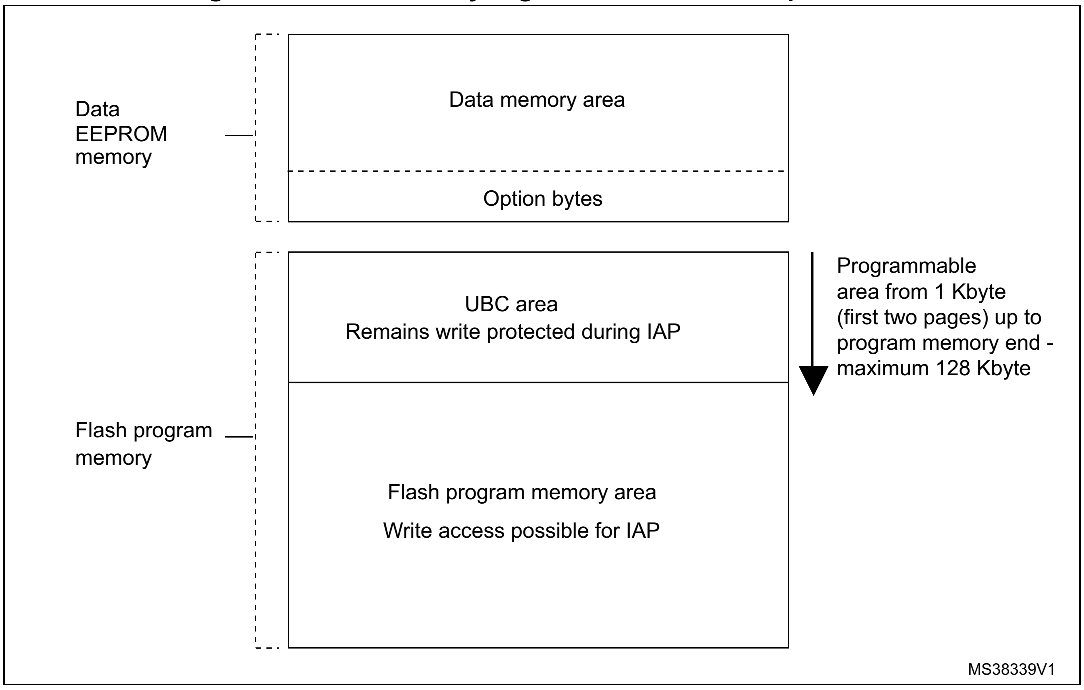
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see Section 9: Option bytes on page 54).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

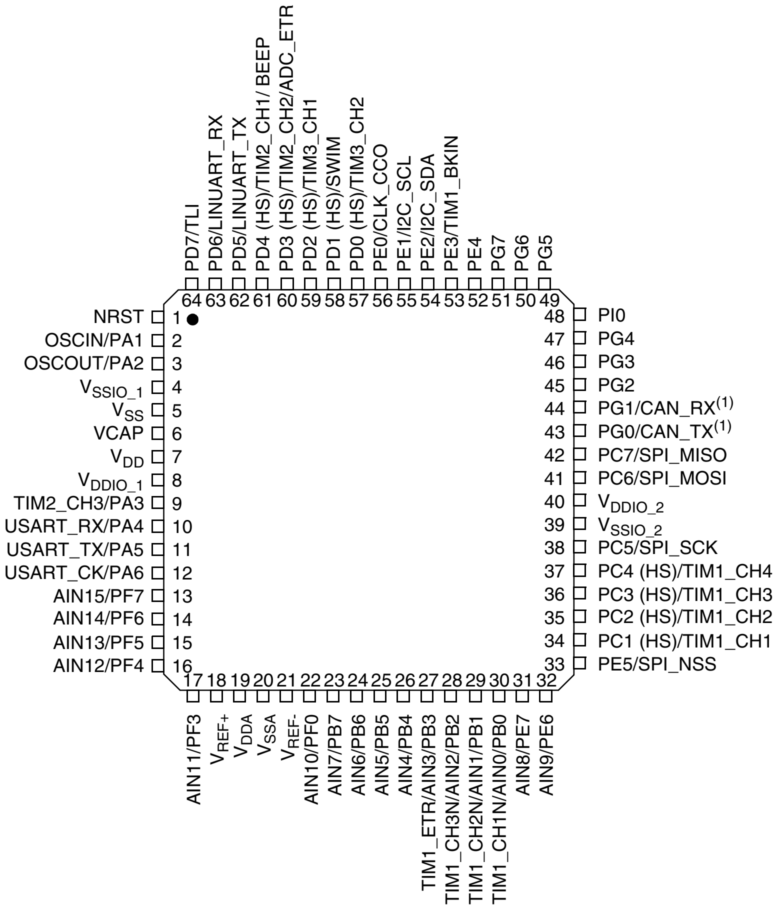
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Figure 4. LQFP 64-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X	-	-	O1	X	X	**Port H7**	Timer 1 - inverted channel 2	-
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	-	-	O1	X	X	**Port E7**	Analog input 8	-
40	32	24			PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E6**	Analog input 9	-
41	33	25	17	17	PE5/SPI_NSS(2)	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/ slave select	-
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X	-	O1	X	X	**Port C0**	ADC trigger input	-
43	34	26	18	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
44	35	27	19	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
45	36	28	20	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
46	37	29	21	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
47	38	30	22	22	PC5/SPI_SCK(2)	I/O	**X**	X	X	-	O3	X	X	**Port C5**	SPI clock	-
48	39	31	-	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
49	40	32	-	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
50	41	33	23	-	PC6/SPI_MOSI (2)	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
51	42	34	24	-	PC7/SPI_MISO (2)	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
52	43	35	-	23	PG0/CAN_TX	I/O	**X**	X	-	-	O1	X	X	**Port G0**	CAN transmit	-
53	44	36	-	24	PG1/CAN_RX	I/O	**X**	X	-	-	O1	X	X	**Port G1**	CAN receive	-
54	45	-	-	-	PG2	I/O	**X**	X	-	-	O1	X	X	**Port G2**	-	-

6.2 Alternate function remapping

As shown in the rightmost column of *Table 11*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 54*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

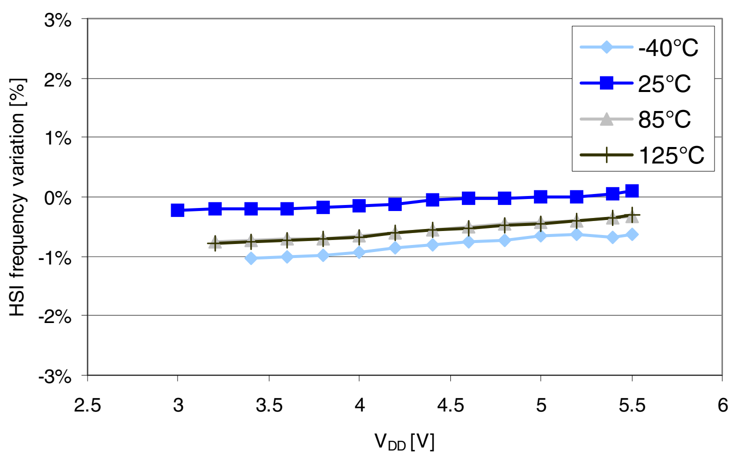
High-speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} = 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 150 °C	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 21. Typical HSI frequency vs V_{DD}



Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

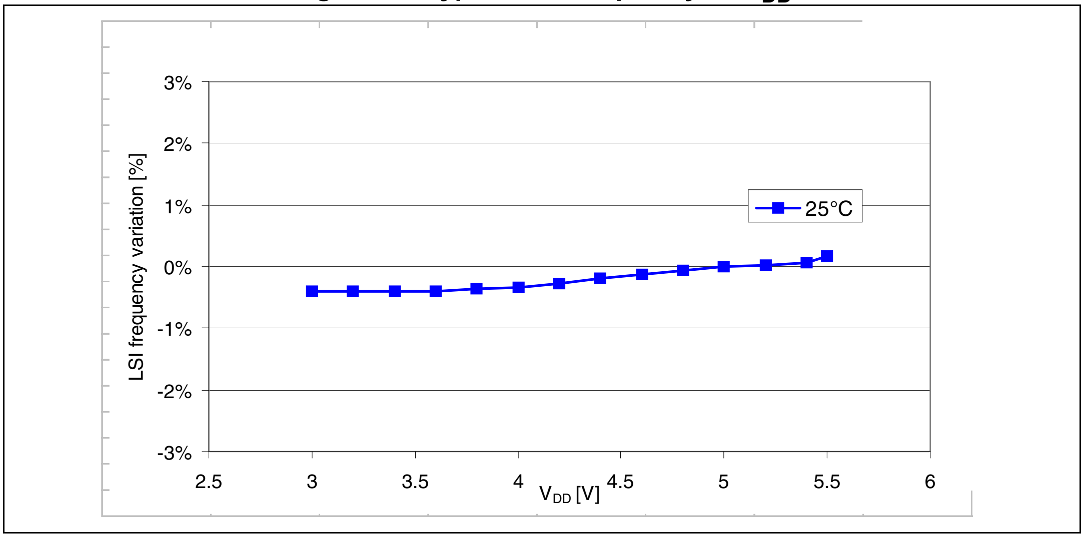


Figure 30. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

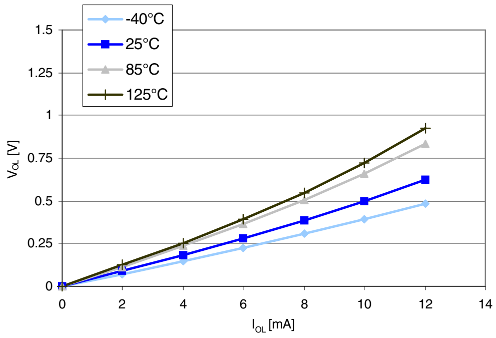


Figure 31. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

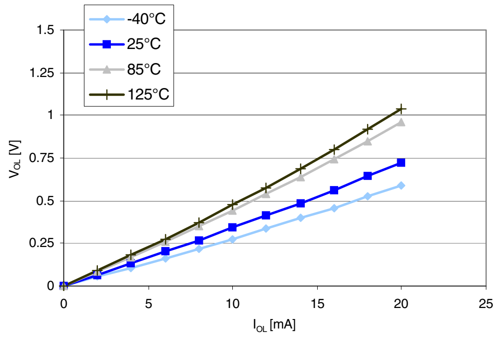


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

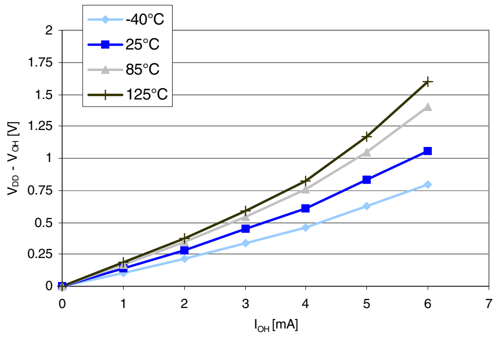


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

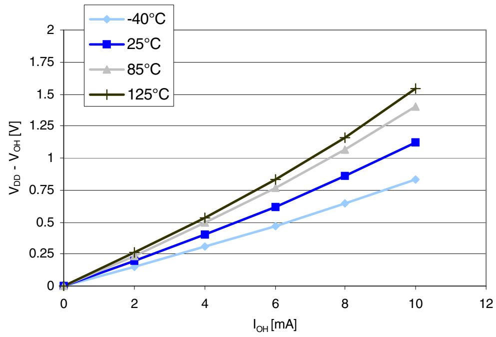


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

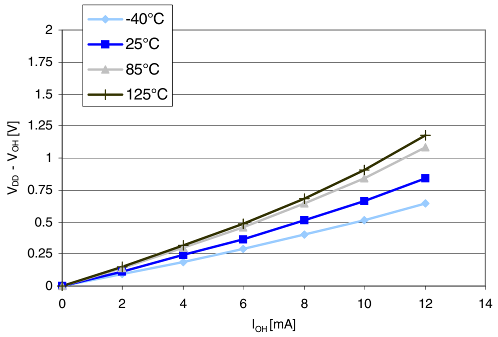
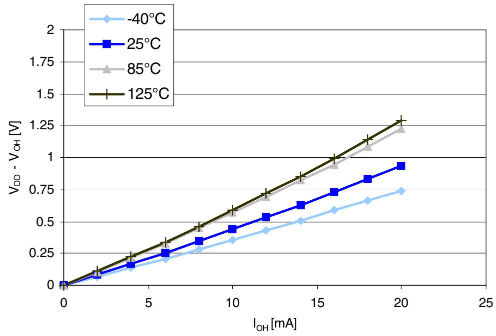


Figure 35. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

10.3.11 10-bit ADC characteristics

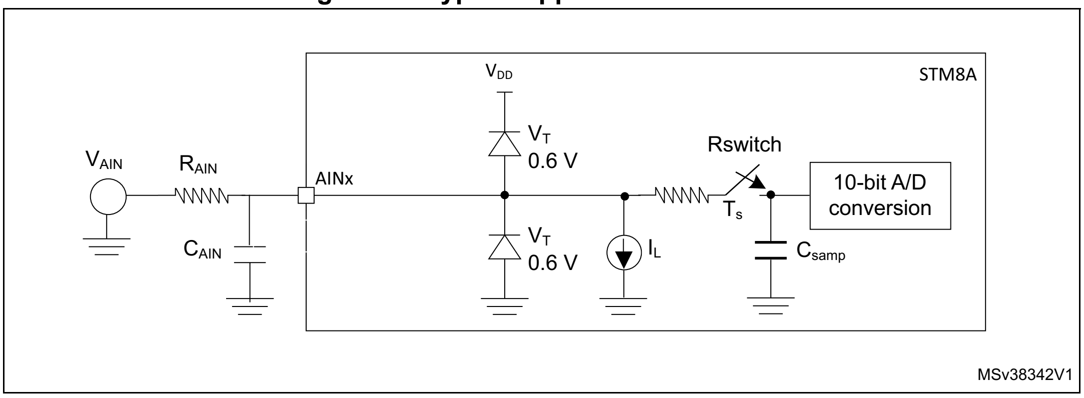
Subject to general operating conditions for V_{DDA}, f_{MASTER} and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x $1/f_{ADC}$)	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x $1/f_{ADC}$)	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 43. Typical application with ADC



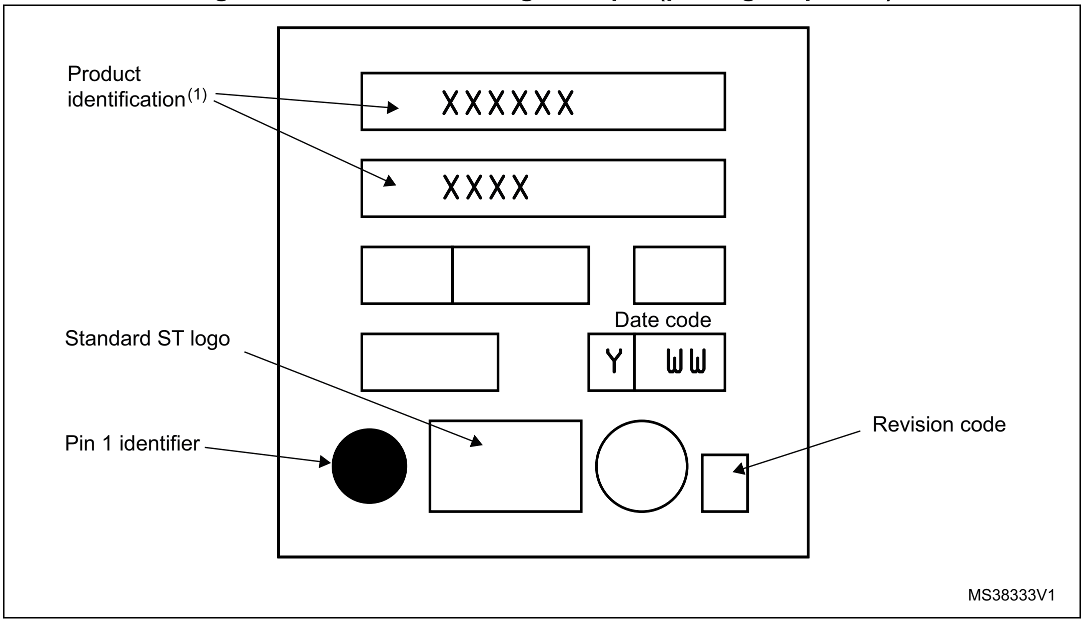
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP80 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP64 marking example (package top view)

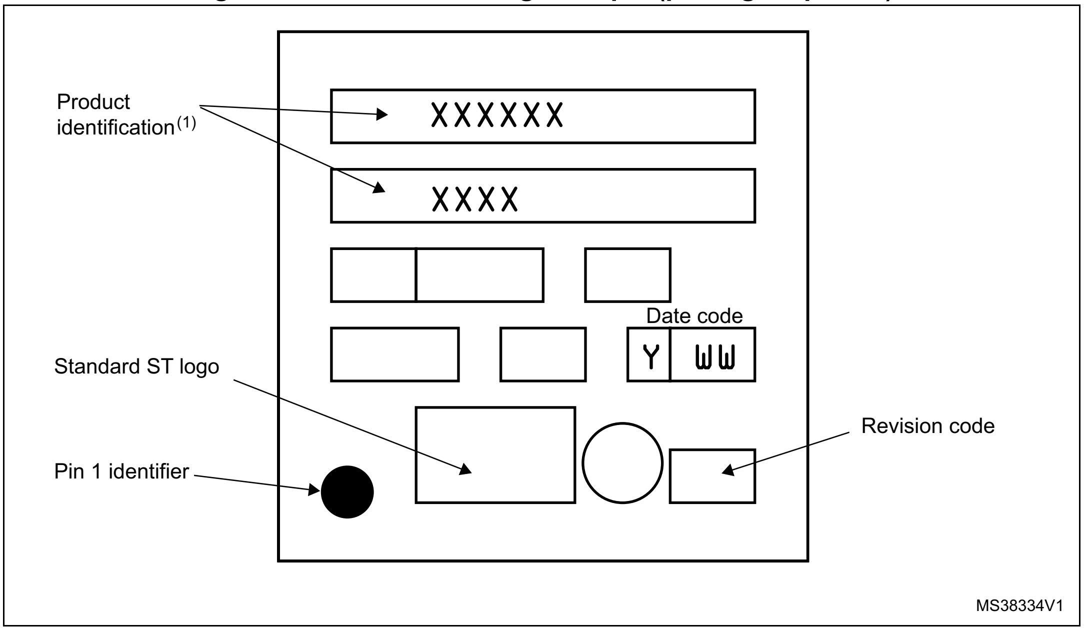


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Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

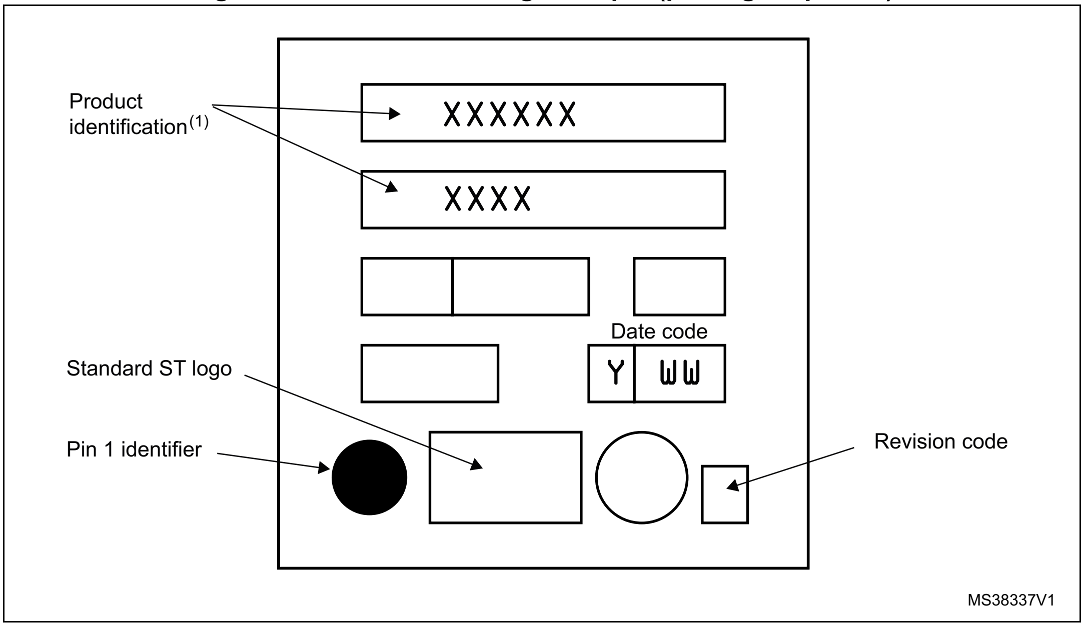
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

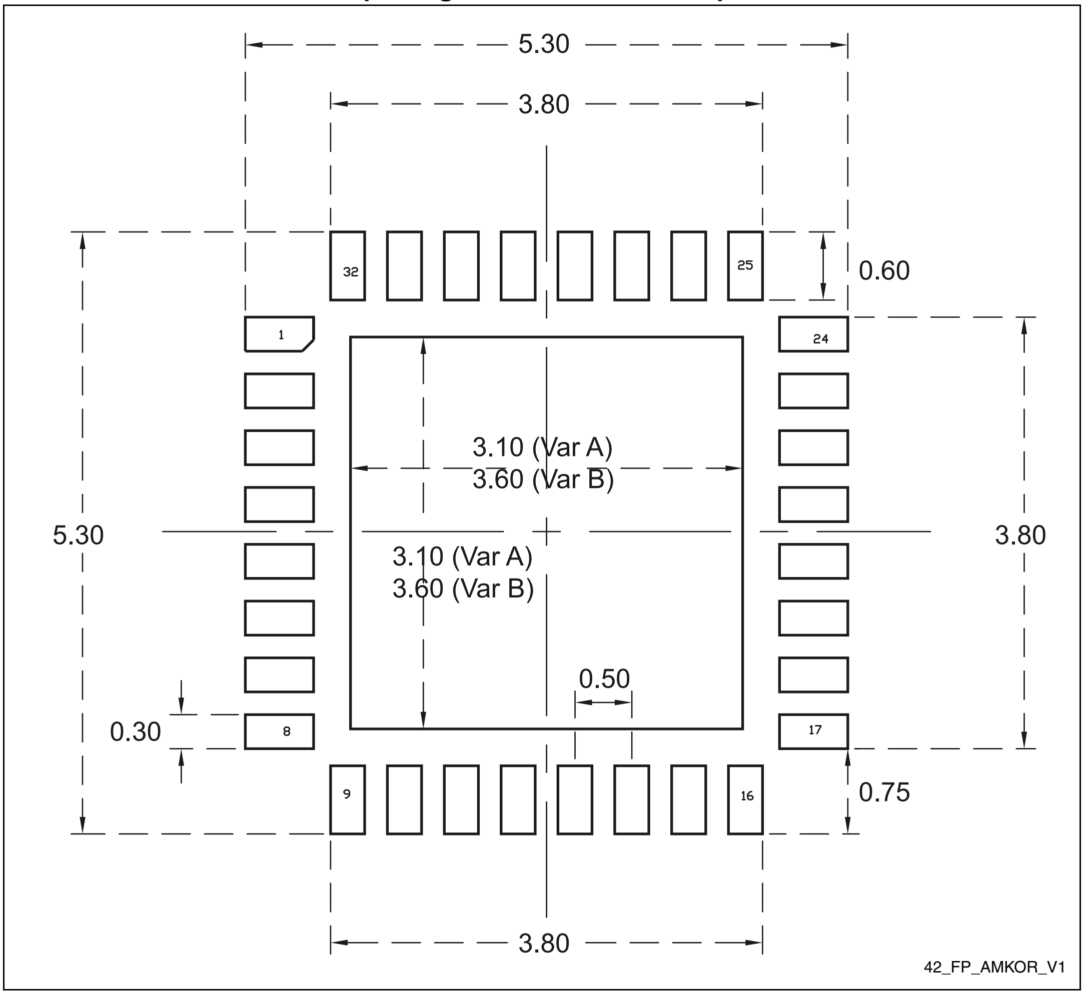
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.6 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 24: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

- $\mathbf{T_{Amax}}$ is the maximum ambient temperature in °C
- $\mathbf{\Theta_{JA}}$ is the package junction-to-ambient thermal resistance in ° C/W
- $\mathbf{P_{Dmax}}$ is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $\mathbf{P_{INTmax}}$ is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $\mathbf{P_{I/Omax}}$ represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low- and high-level in the application.

Table 54. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	25	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.