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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af5289tcy

2 Description

The STM8AF526x/8x/Ax and STM8AF6269/8x/Ax automotive 8-bit microcontrollers described in this datasheet offer from 32 Kbyte to 128 Kbyte of non volatile memory and integrated true data EEPROM. They are referred to as high density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

The STM8AF52 series features a CAN interface.

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, wtachdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

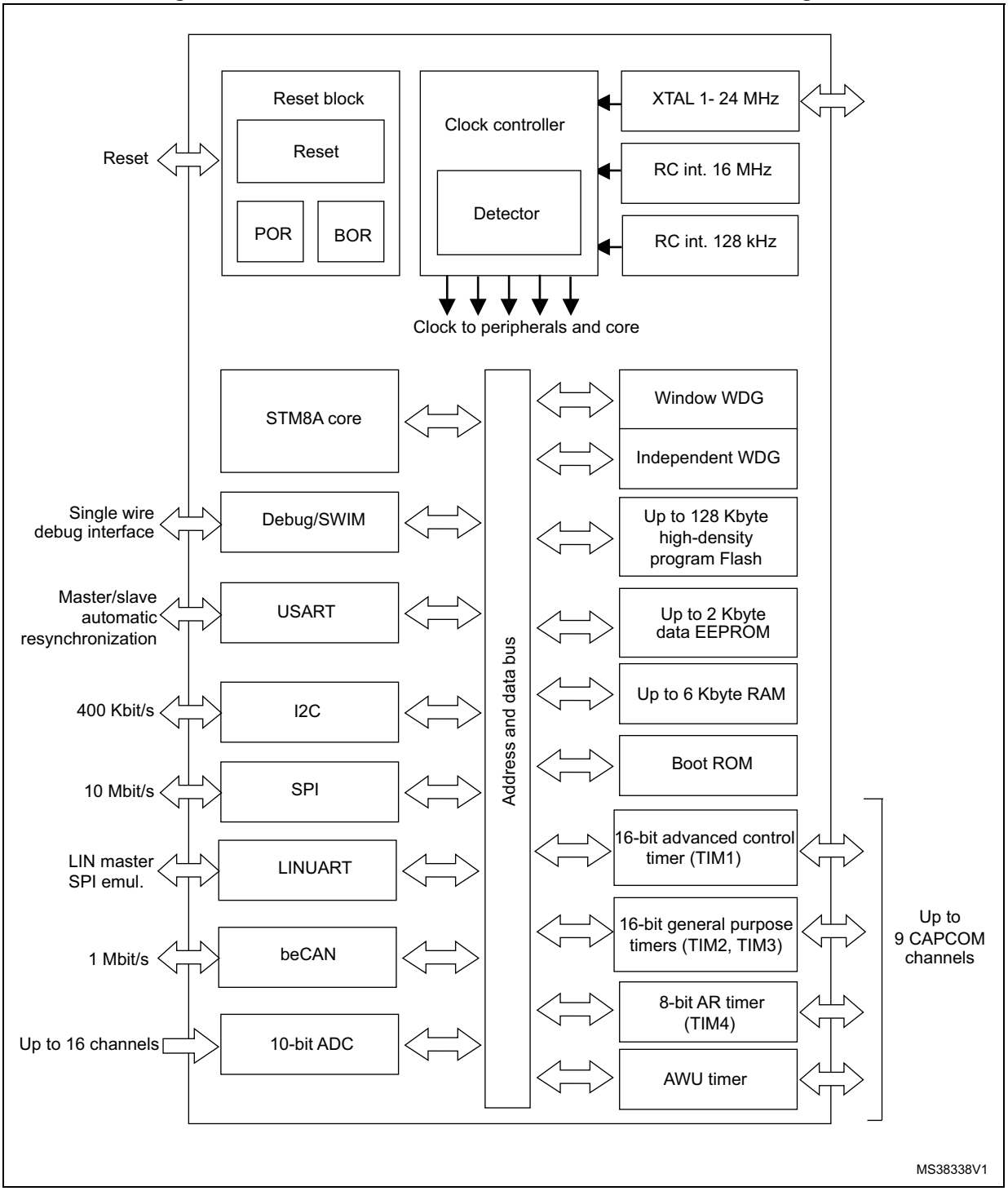
Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map, and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5.5 V operating supply.

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

5.2 Single wire interface module (SWIM) and debug module (DM)

5.2.1 SWIM

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 bytes/ms.

5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-flavored emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 24 interrupt vectors with hardware priority
- Five vectors for external interrupts (up to 37 depending on the package)
- Trap and reset interrupts

5.4 Flash program and data EEPROM

- 32 Kbytes to 128 Kbytes of high density single voltage Flash program memory
- Up to 2 Kbytes true (not emulated) data EEPROM
- Read while write: writing in the data memory is possible while executing code in the Flash program memory.

The whole Flash program memory and data EEPROM are factory programmed with 0x00.

5.4.1 Architecture

- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

Table 6. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

TIM1 - advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.5 Basic timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

Table 7. TIM4

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM4	8-bit	Up	2^n n = 0 to 7	0	None	No	No	No	No

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
  - Mask mode permitting ID range filtering
  - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

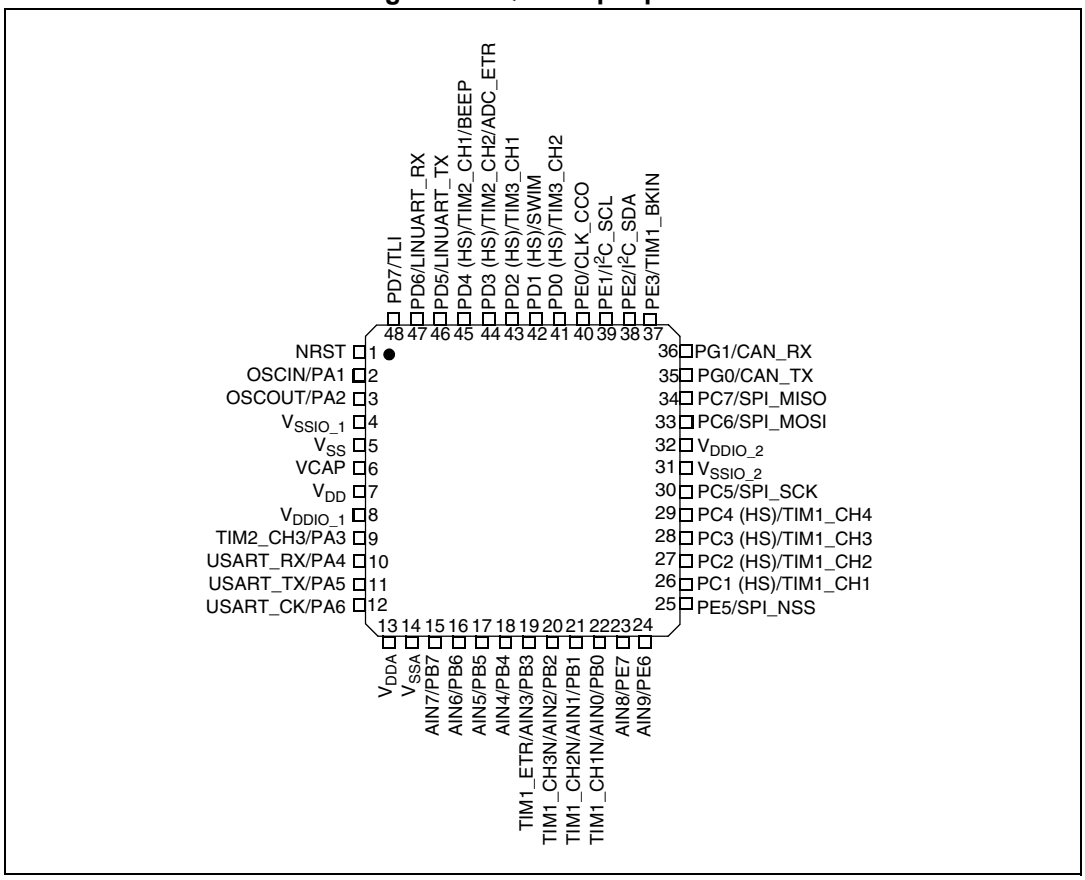
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Figure 5. LQFP 48-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 11*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 54*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 14. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x40
0x00 5060 to 0x005061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

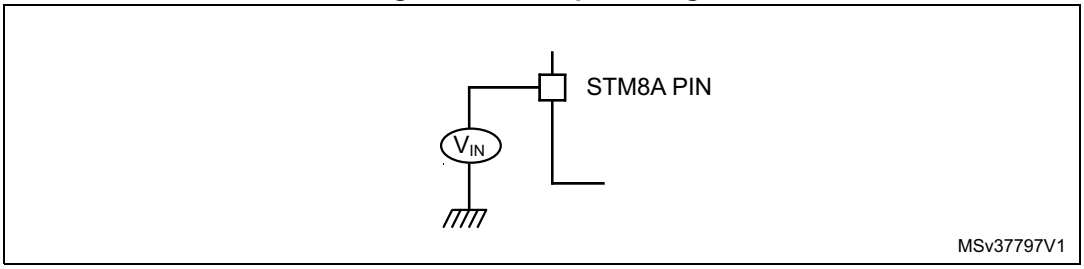
Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics* and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability. The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 20. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 88*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Current consumption curves

Figure 13 to *Figure 18* show typical current consumption measured with code executing in RAM.

Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @f_{CPU} = 16 MHz, peripherals = on

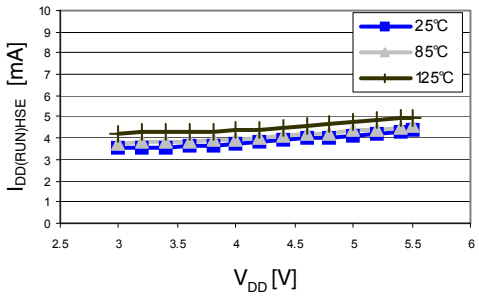


Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

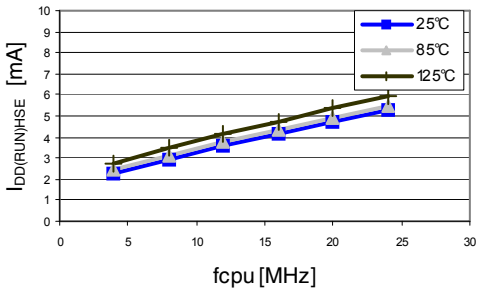


Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off

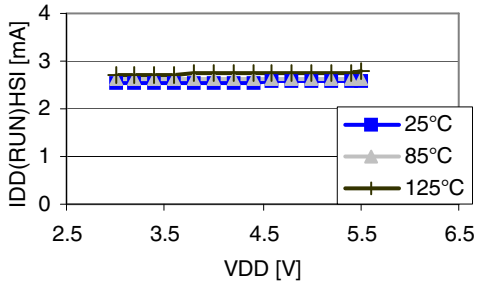


Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = on

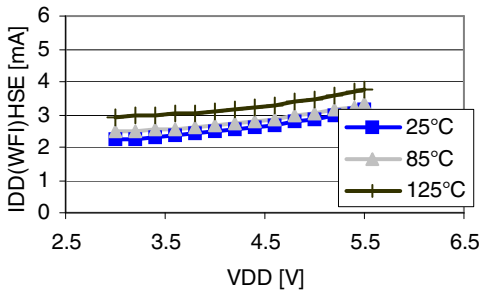


Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

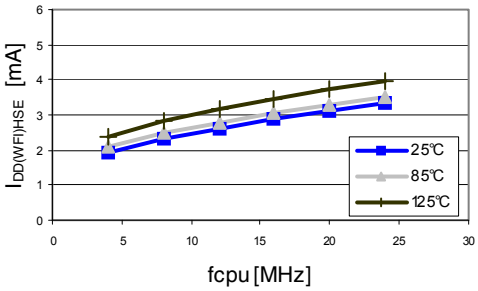
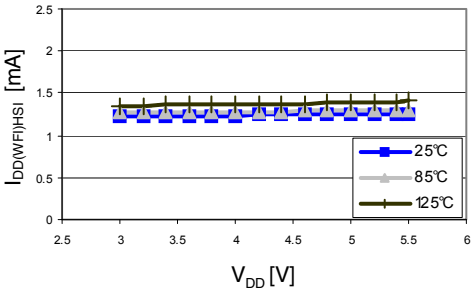


Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST high-level input voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST low-level output voltage(1)	I_{OL} = 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Figure 36. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

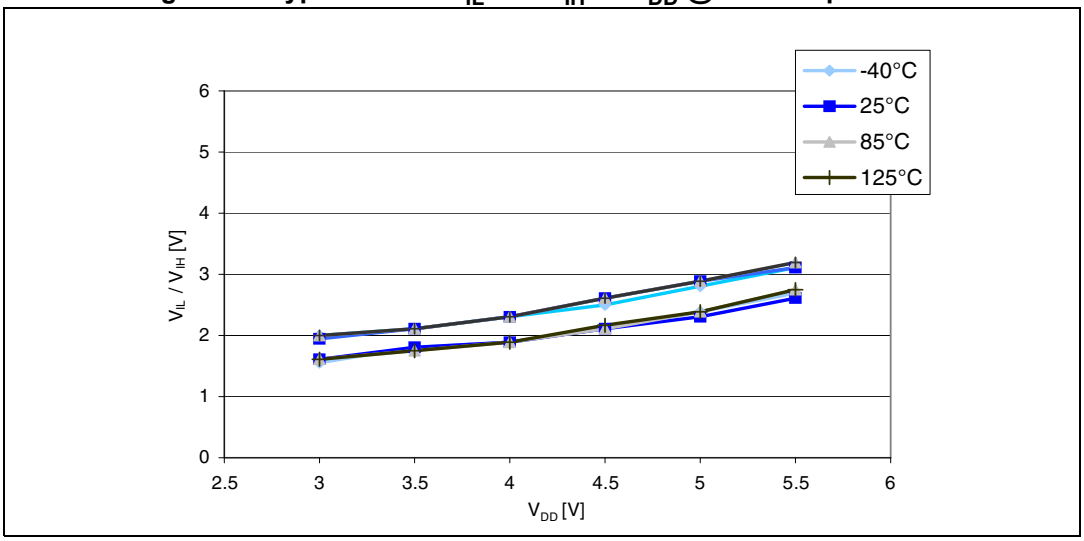
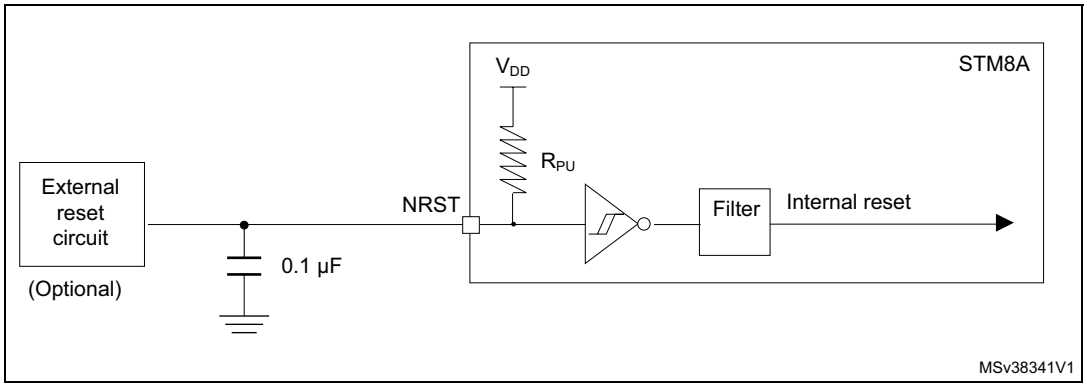


Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

1. Not tested in production.

Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	Added 'H' products to the datasheet (Flash no EEPROM). *Section : Features* on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1. *Table 1: Device summary*: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166. *Section 1: Introduction*, *Section 5: Product overview*, *Section 9: Option bytes*, *Section 6.2: Alternate function remapping*, *Table 21: Current characteristics:* Updated reference documentation: RM0009, PM0047, and UM0470. *Section 2: Description*: added information about peak performance. *Section 3: Product line-up*: Removed *STM8A common features* table. *Table 4: Peripheral clock gating bits (CLK_PCKENR1):* Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T. *Table 5: Peripheral clock gating bits (CLK_PCKENR2)*: Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T. *Section 5: Product overview*: Made minor content changes and improved readability and layout. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: Major modification, TMU included. *Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI)*: User trimming updated. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: LSI as CPU clock added. *Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE)*, *Section 5.5.5: External clock input*: Maximum frequency conditional 32 Kbyte/128 Kbyte. *Section 5.8: Analog to digital converter (ADC)*: Scan for 128 Kbyte removed. *Section 5.9: Communication interfaces*, *Section 5.9.3: Serial peripheral interface (SPI)*: SPI 10 Mb/s. *Figure 3: LQFP 80-pin pinout*, *Figure 4: LQFP 64-pin pinout*, *Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout*: Amended footnote 1. *Table 12: Memory model 128K:* HS output changed from 20 mA to 8 mA. *Section 7: Memory and register map*: Corrected *Table 8: Register and memory map*; removed address list; added *Table 14: General hardware register map*. *Section 10.3.2: Supply current characteristics* Note on typical/WC values added.

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	Replaced the salestype 'STM8H61xx' with 'STM8AH61xx on the first page. Added 'part numbers' to heading rows of *Table 1: Device summary*. Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD. *Table 18*: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]' *Section 9*: Updated introductory text concerning option bytes which do not need to be saved in a complementary form. *Table 18*: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively. *Table 21*: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'. Updated 80-pin package information in line with POA 0062342-revD in *Figure 45* and *Table 53*.
01-Jul-2009	4	Added 'STM8AH61xx' and 'STM8AH51xx to document header. Updated *: Features on page 1* (memories, timers, operating temperature, ADC and I/Os). Updated *Table 1: Device summary* Updated Kbyte value of program memory in *Section: Introduction* Changed the first two lines from the top in *Section: Description*. Updated *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram* Updated *Section 5: Product overview* In *Figure 5: LQFP 48-pin pinout*, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively. *Section 6: Pinouts and pin description:* deleted the text below the *Table 10: Legend/abbreviation for the pin description table* *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description:* 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote. Updated *Figure 8: Register and memory map*. *Table 12: Memory model 128K:* updated footnote Deleted the *Table: Stack and RAM partitioning* *Table 17: STM8A interrupt table*: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote Updated *Section 7: Memory and register map* Updated *Table: Data memory, Table: I/O static characteristics,* and *Table 39: NRST pin characteristics*. *Section 10.1.1: Minimum and maximum values:* added ambient temperature T_A = -40 °C Updated *Table 20: Voltage characteristics*. Updated *Table 21: Current characteristics*. Updated *Table 22: Thermal characteristics*. Updated *Table 24: General operating conditions*.

Table 55. Document revision history (continued)

Date	Revision	Changes
31-Mar-2014	10 (continued)	Added: – *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout;* – the caution in *Section 5.10: Input/output specifications,* – The table footnote “Not recommended for new designs” to *Table: STM8AF/H/P51xx product line-up with CAN* and *Table: STM8AF/H/P61xx product line-up without CAN.* – The figure footnotes to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* and *Figure: VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)*
13-Jun-2014	11	Added STM8AF52A6 part number.
09-Jun-2015	12	Added: – the third table footnote to *Table 25: Operating conditions at power-up/power-down*, – *Figure 47: LQFP80 marking example (package top view)*, – *Figure 50: LQFP64 marking example (package top view)*, – *Figure 53: LQFP48 marking example (package top view)*, – *Figure 56: LQFP32 marking example (package top view)*, – *Figure 59: VFQFPN32 marking example (package top view)*, – the footnote about the device marking to *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Removed STM8AF51xx and STM8AF61xx obsolete root part numbers, and consequently “H” products: – *Table 1: Device summary*, – *Section 1: Introduction*, – *Section 2: Description*, – *Section 3: Product line-up*, – *Table 12: Memory model 128K*, – *Section 10.3: Operating conditions*, – *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Moved *Section 11.6: Thermal characteristics* to *Section 11: Package information*. Updated: – the product naming in the document headers and captions, – the standard reference for EMI characteristics in *Table 46: EMI data*.
13-Jun-2016	13	Updated *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data*