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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af528atcx

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3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

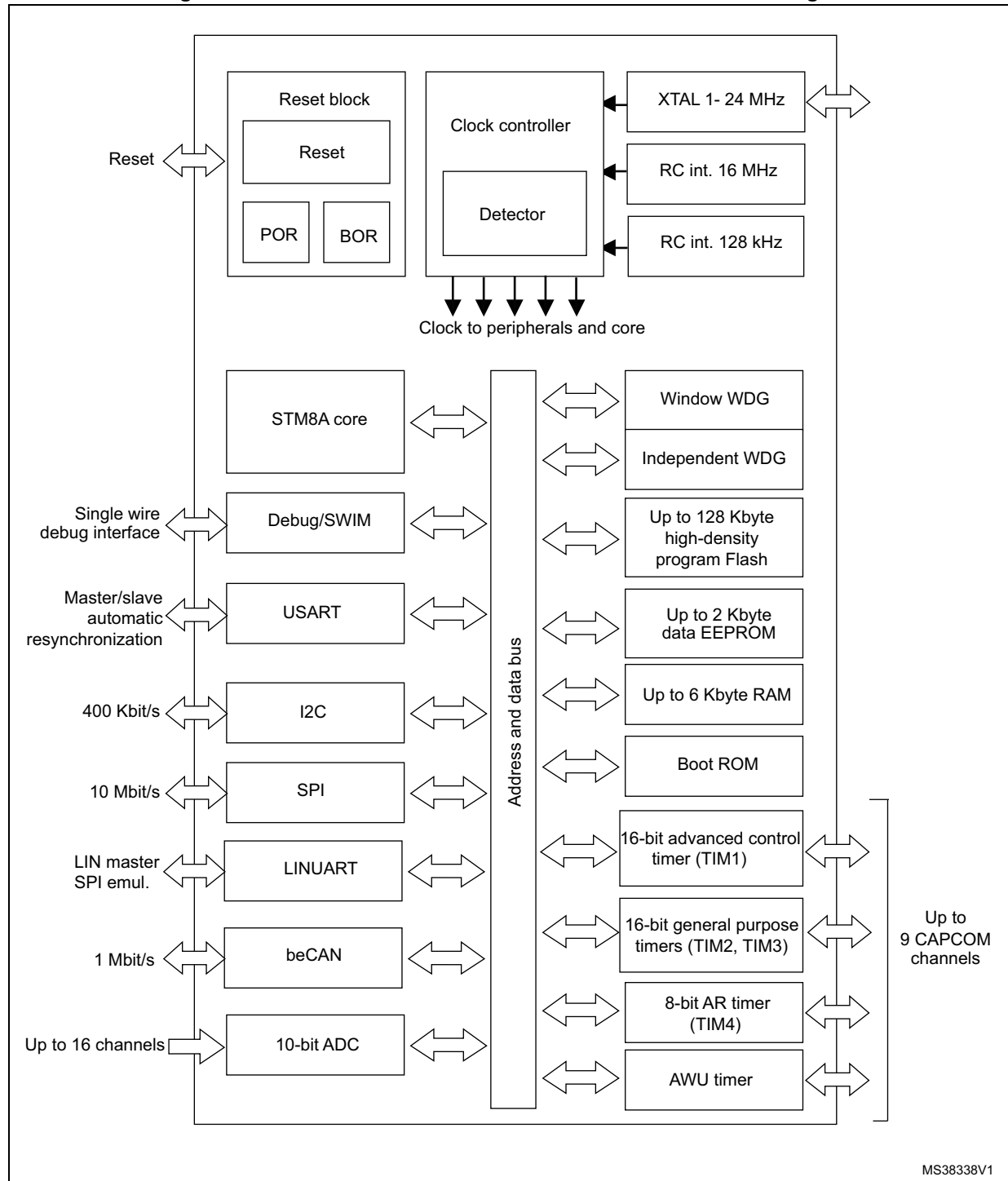
Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I ² C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	128 K	52/36						
STM8AF/P5289	LQFP64 (10x10)			64 K				
STM8AF/P5269				32 K				
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K						
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I ² C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I ² C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	128 K	2 K						
STM8AF/P6289	64 K							
STM8AF/P6269	32 K			1 K				
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			25/23
STM8AF/P6288								
STM8AF/P6286	LQFP32 (7x7)	64 K			7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I ² C	
STM8AF/P62A6	VFQFPN32 (5x5)	128 K						

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



- Interrupt:
 - Successful address/data communication
 - Error condition
 - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

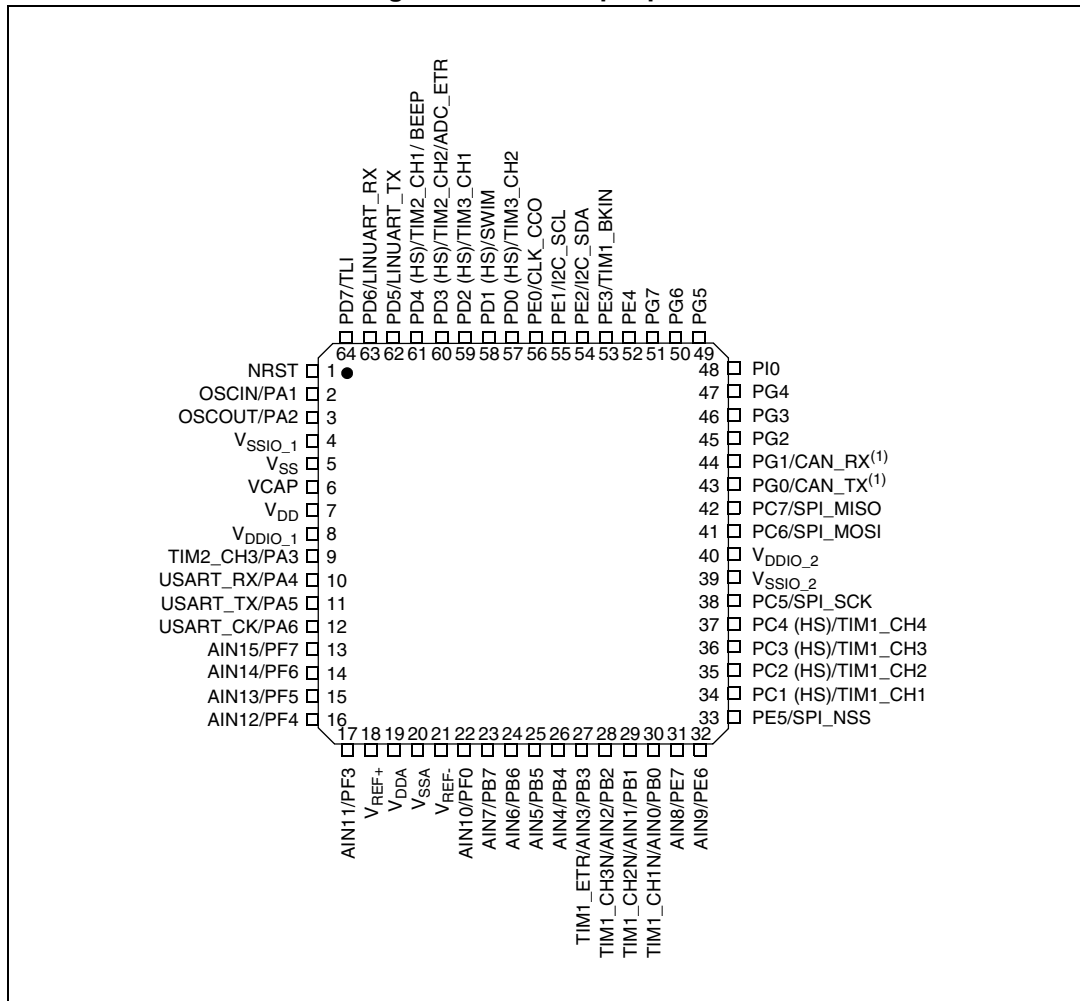
Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
 - Mask mode permitting ID range filtering
 - ID list mode

Interrupt management

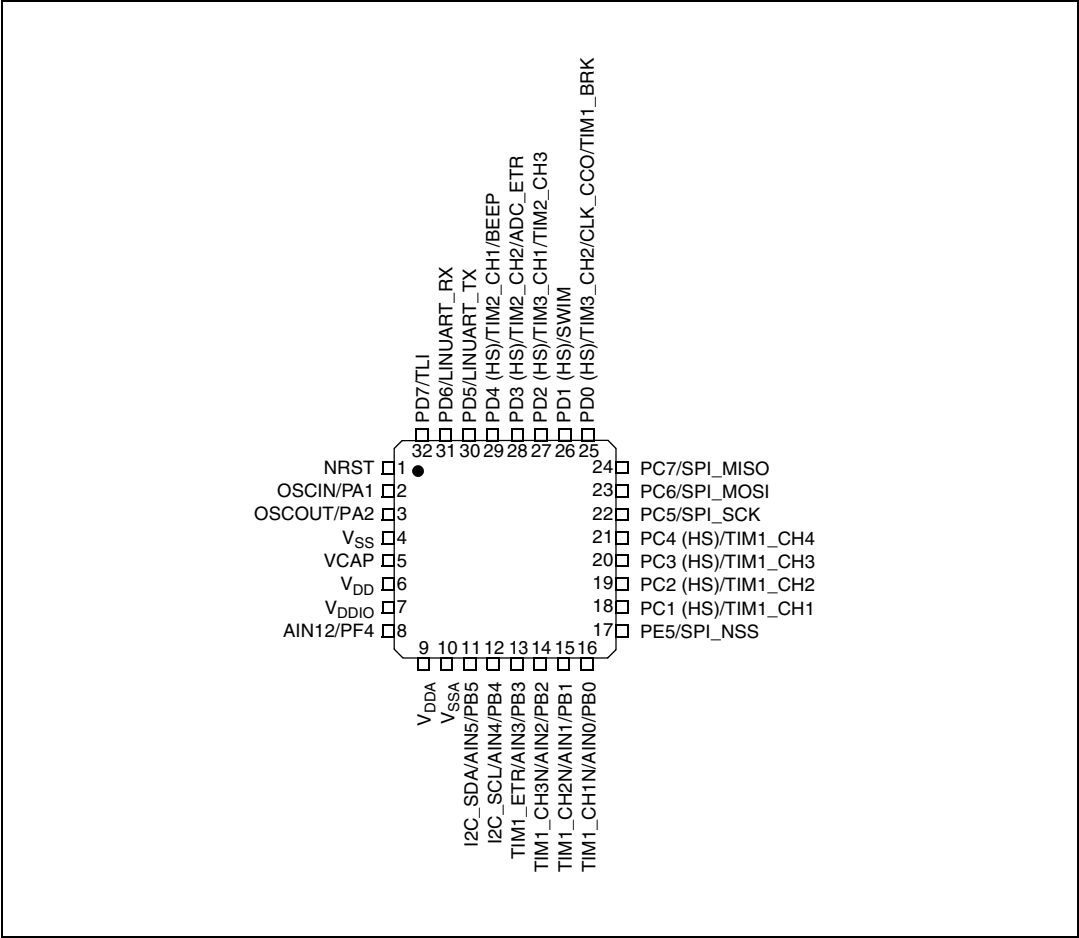
- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

Figure 4. LQFP 64-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout



1. HS stands for high sink capability.

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = -40\text{ }^{\circ}\text{C}$, $T_A = 25\text{ }^{\circ}\text{C}$, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

Figure 9. Pin loading conditions

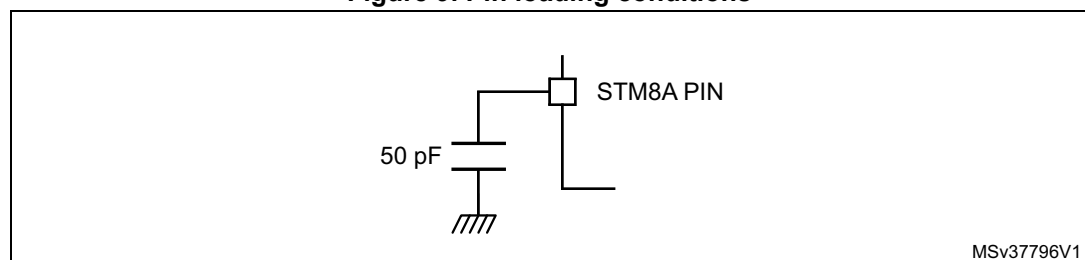


Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, $T_A = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(RUN)}^{(1)}$	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	$f_{CPU} = 24\text{ MHz}$ 1 ws	8.7	16.8 ⁽²⁾
			$f_{CPU} = 16\text{ MHz}$	7.4	14
			$f_{CPU} = 8\text{ MHz}$	4.0	7.4 ⁽²⁾
			$f_{CPU} = 4\text{ MHz}$	2.4	4.1 ⁽²⁾
			$f_{CPU} = 2\text{ MHz}$	1.5	2.5
$I_{DD(RUN)}^{(1)}$	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	$f_{CPU} = 24\text{ MHz}$	4.4	6.0 ⁽²⁾
			$f_{CPU} = 16\text{ MHz}$	3.7	5.0
			$f_{CPU} = 8\text{ MHz}$	2.2	3.0 ⁽²⁾
			$f_{CPU} = 4\text{ MHz}$	1.4	2.0 ⁽²⁾
			$f_{CPU} = 2\text{ MHz}$	1.0	1.5
$I_{DD(WFI)}^{(1)}$	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	$f_{CPU} = 24\text{ MHz}$	2.4	3.1 ⁽²⁾
			$f_{CPU} = 16\text{ MHz}$	1.65	2.5
			$f_{CPU} = 8\text{ MHz}$	1.15	1.9 ⁽²⁾
			$f_{CPU} = 4\text{ MHz}$	0.90	1.6 ⁽²⁾
			$f_{CPU} = 2\text{ MHz}$	0.80	1.5
$I_{DD(SLOW)}^{(1)}$	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz $f_{CPU} = 125\text{ kHz}$	1.50	1.95
			LSI internal RC $f_{CPU} = 128\text{ kHz}$	1.50	1.80 ⁽²⁾

1. The current due to I/O utilization is not taken into account in these values.

2. Guaranteed by design, not tested in production.

Table 27. Total current consumption in Halt and Active-halt modes. General conditions for V_{DD} applied. $T_A = -40\text{ }^{\circ}\text{C}$ to $55\text{ }^{\circ}\text{C}$ unless otherwise stated

Symbol	Parameter	Conditions			Typ	Max	Unit
		Main voltage regulator (MVR) ⁽¹⁾	Flash mode ⁽²⁾	Clock source and temperature condition			
$I_{DD(H)}$	Supply current in Halt mode	Off	Power-down	Clocks stopped	5	35 ⁽³⁾	μA
				Clocks stopped, $T_A = 25\text{ }^{\circ}\text{C}$	5	25	
$I_{DD(AH)}$	Supply current in Active-halt mode with regulator on	On	Power-down	External clock 16 MHz $f_{\text{MASTER}} = 125\text{ kHz}$	770	900 ⁽³⁾	
				LSI clock 128 kHz	150	230 ⁽³⁾	
	Supply current in Active-halt mode with regulator off	Off	Power-down	LSI clock 128 kHz	25	42 ⁽³⁾	
				LSI clock 128 kHz, $T_A = 25\text{ }^{\circ}\text{C}$	25	30	
$t_{WU(AH)}$	Wakeup time from Active-halt mode with regulator on	On	Operating mode	$T_A = -40\text{ to }150\text{ }^{\circ}\text{C}$	10	30 ⁽³⁾	μs
	Wakeup time from Active-halt mode with regulator off	Off			50	80 ⁽³⁾	

1. Configured by the REGAH bit in the CLK_ICR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.
3. Guaranteed by characterization results, not tested in production.

Current consumption for on-chip peripherals

Table 28. Oscillator current consumption

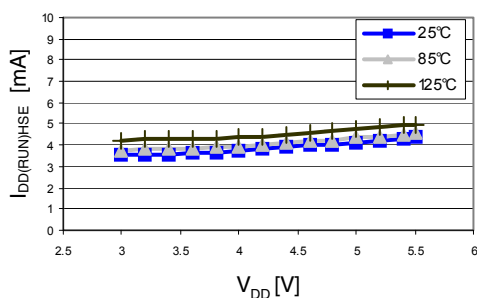
Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(OSC)}$	HSE oscillator current consumption ⁽²⁾	Quartz or ceramic resonator, CL = 33 pF $V_{DD} = 5\text{ V}$	$f_{\text{OSC}} = 24\text{ MHz}$	1	2.0 ⁽³⁾	mA
			$f_{\text{OSC}} = 16\text{ MHz}$	0.6	-	
			$f_{\text{OSC}} = 8\text{ MHz}$	0.57	-	
$I_{DD(OSC)}$	HSE oscillator current consumption ⁽²⁾	Quartz or ceramic resonator, CL = 33 pF $V_{DD} = 3.3\text{ V}$	$f_{\text{OSC}} = 24\text{ MHz}$	0.5	1.0 ⁽³⁾	
			$f_{\text{OSC}} = 16\text{ MHz}$	0.25	-	
			$f_{\text{OSC}} = 8\text{ MHz}$	0.18	-	

1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Informative data.

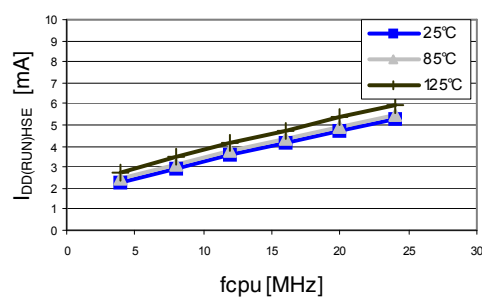
Current consumption curves

Figure 13 to Figure 18 show typical current consumption measured with code executing in RAM.

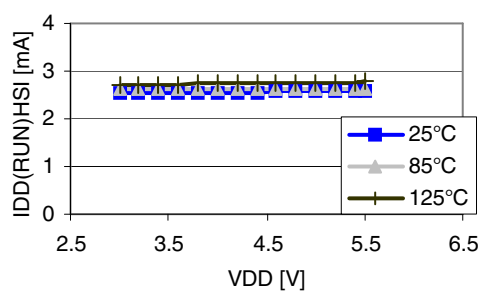
**Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = on**



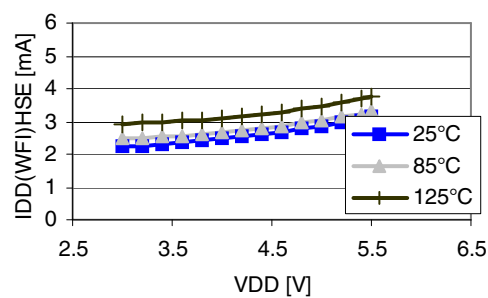
**Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU}
@ $V_{DD} = 5.0$ V, peripherals = on**



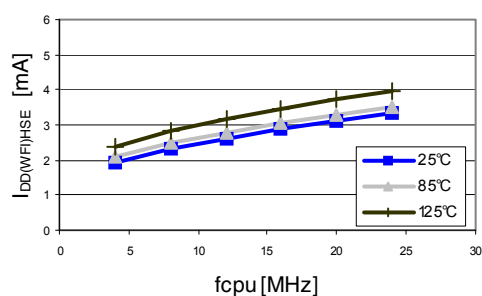
**Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = off**



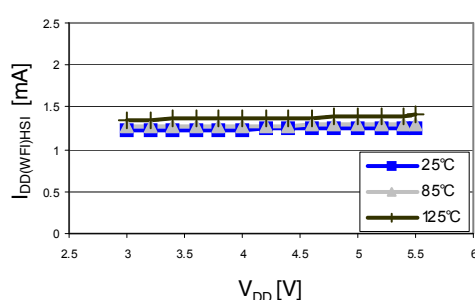
**Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = on**



**Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU}
@ $V_{DD} = 5.0$ V, peripherals = on**



**Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD}
@ $f_{CPU} = 16$ MHz, peripherals = off**



10.3.3 External clock sources and timing characteristics

HSE external clock

An HSE clock can be generated by feeding an external clock signal of up to 24 MHz to the OSCIN pin.

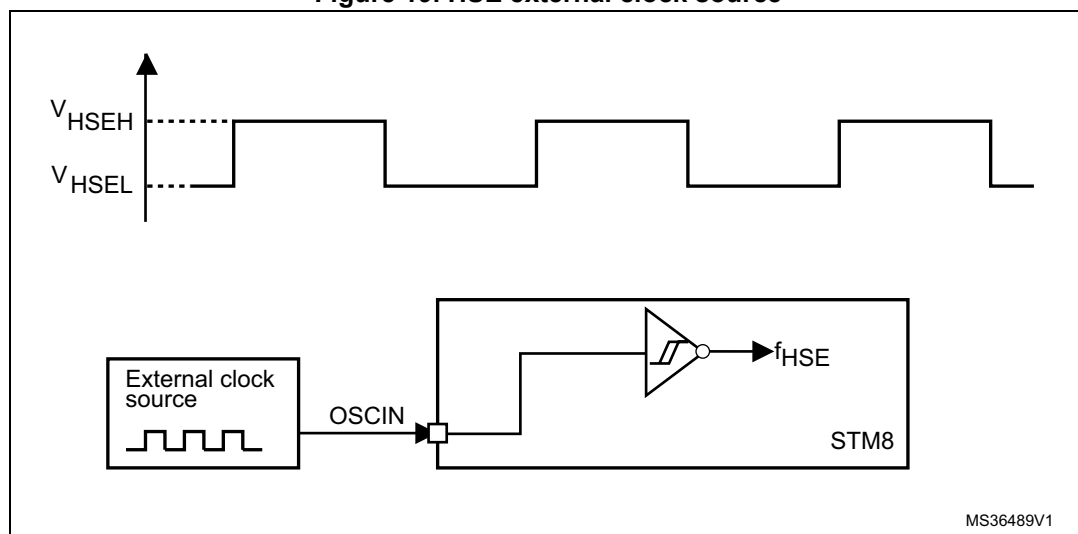
Clock characteristics are subject to general operating conditions for V_{DD} and T_A .

Table 31. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	$T_A = -40\text{ }^{\circ}\text{C to }150\text{ }^{\circ}\text{C}$	0 ⁽¹⁾	-	24	MHz
V_{HSEdHL}	Comparator hysteresis	-	$0.1 \times V_{DD}$	-	-	V
V_{HSEH}	OSCIN high-level input pin voltage	-	$0.7 \times V_{DD}$	-	V_{DD}	
V_{HSEL}	OSCIN low-level input pin voltage	-	V_{SS}	-	$0.3 \times V_{DD}$	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	μA

1. If CSS is used, the external clock must have a frequency above 500 kHz.

Figure 19. HSE external clock source



MS36489V1

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 24 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

10.3.11 10-bit ADC characteristics

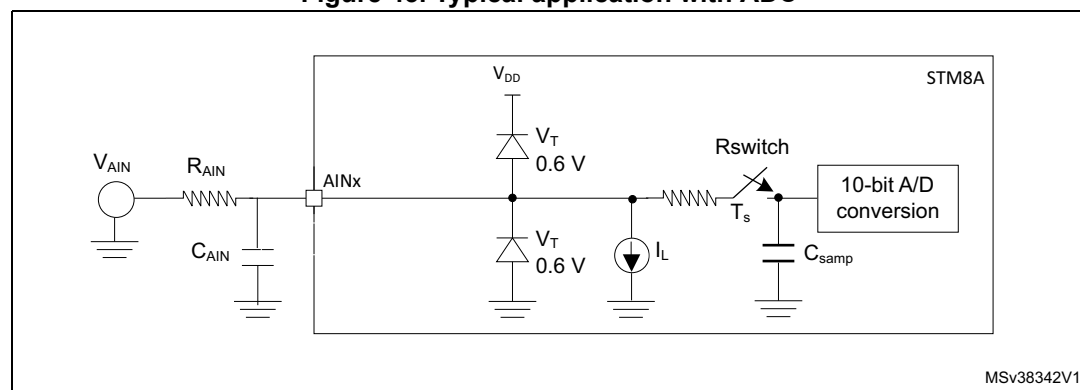
Subject to general operating conditions for V_{DDA} , f_{MASTER} and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range ⁽¹⁾	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{smp}	Internal sample and hold capacitor	-	-	-	3	pF
$t_S^{(1)}$	Sampling time ($3 \times 1/f_{ADC}$)	$f_{ADC} = 2$ MHz	-	1.5	-	μs
		$f_{ADC} = 4$ MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	$f_{ADC} = 2$ MHz	-	7	-	
		$f_{ADC} = 4$ MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time ($14 \times 1/f_{ADC}$)	$f_{ADC} = 2$ MHz	-	7	-	μs
		$f_{ADC} = 4$ MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	k Ω

1. During the sample time, the sampling capacitance, C_{smp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result.

Figure 43. Typical application with ADC



1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{smp} = internal sample and hold capacitor.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class ⁽¹⁾
LU	Static latch-up class	$T_A = 25\text{ °C}$	A
		$T_A = 85\text{ °C}$	
		$T_A = 125\text{ °C}$	
		$T_A = 150\text{ °C}$	

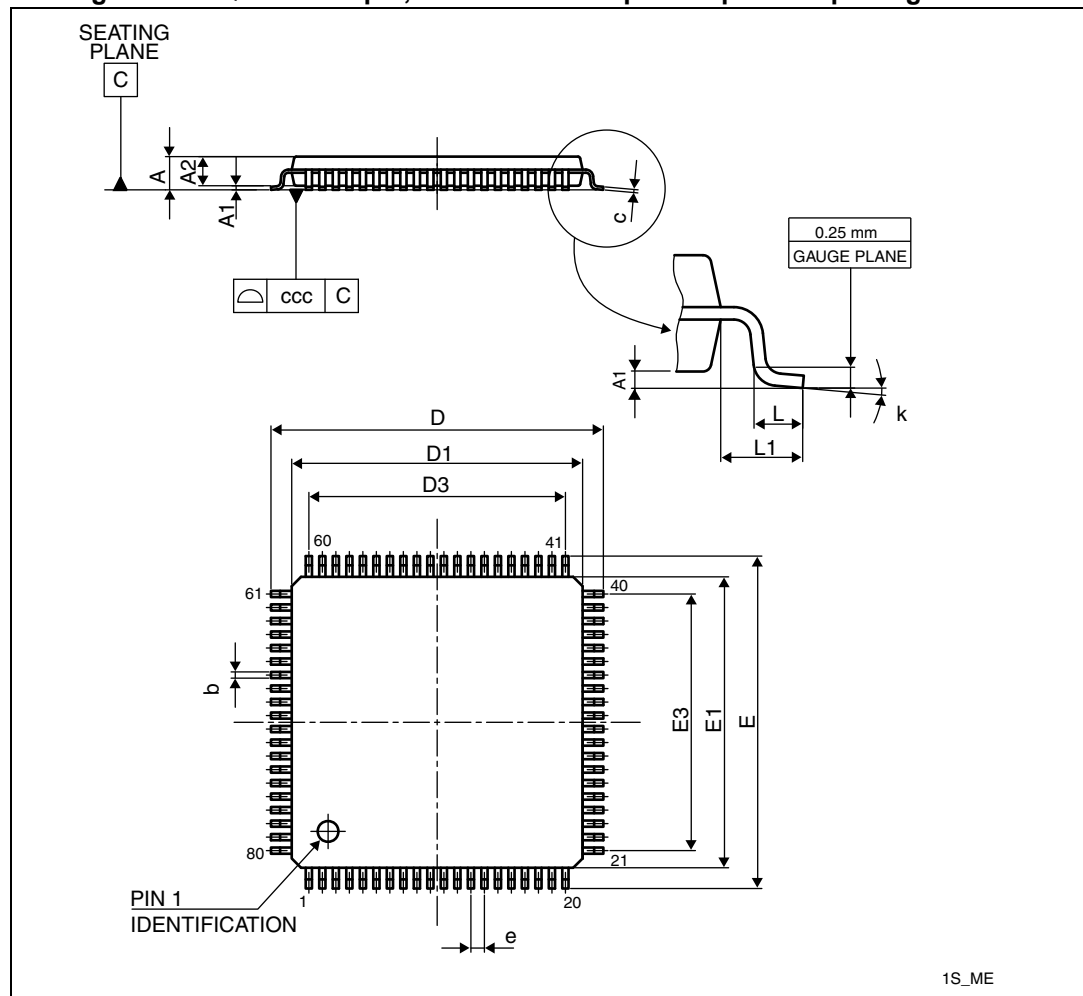
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

11.1 LQFP80 package information

Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



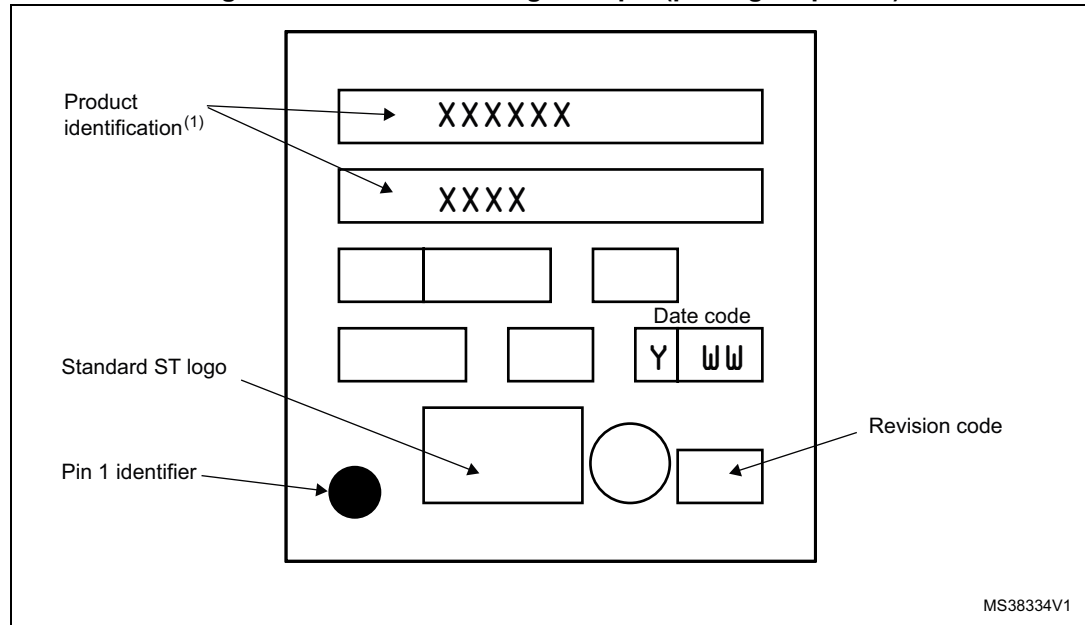
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

**Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

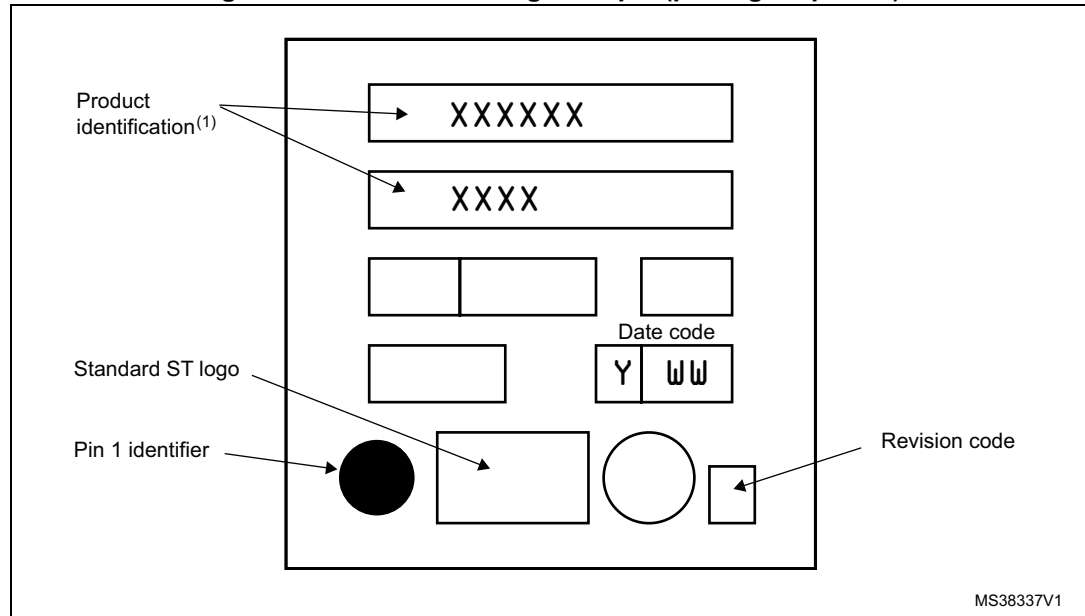
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

13 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

13.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

13.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high-speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of high density Flash program memory. Updated the number of I/Os for devices in 80-, 64-, and 48-pin packages in <i>Table: STM8AF52xx product line-up with CAN</i>, <i>Table: STM8AF62xx product line-up without CAN</i>, <i>Table: STM8AF/H/P51xx product line-up with CAN</i>, and <i>Table: STM8AF/H/P61xx product line-up without CAN</i>. Added TMU brief description in Section 5.4: Flash program and data EEPROM, updated TMU_MAXATT description in Table 19: Option byte description, and TMU_MAWATT reset value in Table 18: Option bytes. Updated clock sources in Section 5.5.1: Features. Added Table 4: Peripheral clock gating bits (CLK_PCKENR1). Added calibration using TIM3 in Section 5.7.2: Auto-wakeup counter. Added Table 8: ADC naming and Table 9: Communication peripheral naming correspondence. Updated SPI data rate to $f_{\text{MASTER}}/2$ in Section 5.9.3: Serial peripheral interface (SPI). Added reset state in Table 10: Legend/abbreviation for the pin description table. <i>Table: STM8A microcontroller family pin description</i>: modified footnotes related to PD1/SWIM, corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. <i>Section: Register map</i>: Removed CAN register CLK_CANCCR. Removed I2C_PECR register. Added <i>footnote</i> for Px_IDR registers in Table 13: I/O port hardware register map. Updated register reset values for Px_IDR and PD_CR1 registers. Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, TMU, clock controller, interrupt controller, timers, communication interfaces, and ADC, by Table 14: General hardware register map. Added debug module register map Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off, updated Section 5.6: Low-power operating modes, and Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated. $I_{\text{DD}}(\text{FAH})$ and $I_{\text{DD}}(\text{SAH})$ renamed $I_{\text{DD}}(\text{AH})$; $t_{\text{WU}}(\text{FAH})$ and $t_{\text{WU}}(\text{SAH})$ renamed $t_{\text{WU}}(\text{AH})$.