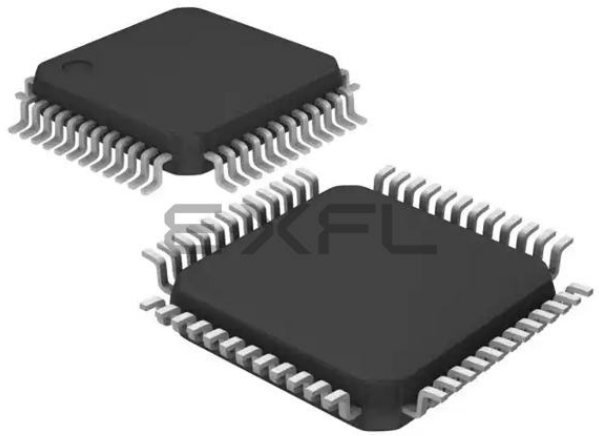


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | STM8A |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a8tay |

# List of tables

# 3 Product line-up

**Table 2. STM8AF526x/8x/Ax product line-up with CAN**

| Order code | Package | High density Flash program memory (bytes) | RAM (bytes) | Data EEPROM (bytes) | 10-bit A/D chan. | Timers (IC/OC/PWM) | Serial interfaces | I/0 wakeup pins |
|---|---|---|---|---|---|---|---|---|
| STM8AF/P52AA | LQFP80 (14x14) | 128 K | 6 K | 2 K | 16 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9) | CAN, LIN(UART), SPI, USART, I²C | 68/37 |
| STM8AF/P528A | | 64 K | | | | | | |
| STM8AF/P52A9 | LQFP64 (10x10) | 128 K | | | | | | 52/36 |
| STM8AF/P5289 | | 64 K | | | | | | |
| STM8AF/P5269 | | 32 K | | 1 K | | | | |
| STM8AF/P52A8 | LQFP48 (7x7) | 128 K | | 2 K | 10 | | | 38/35 |
| STM8AF/P5288 | | 64 K | | | | | | |
| STM8AF/P5268 | | 32 K | | 1K | | | | |
| STM8AF/P5286 | VFQFPN32 (5x5) | 64 K | | 2 K | 6 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8) | CAN, LIN(UART), I²C | 25/24 |
| STM8AF/P52A6 | | 128 K | | | | | | |

**Table 3. STM8AF6269/8x/Ax product line-up without CAN**

| Order code | Package | High density Flash program memory (bytes) | RAM (bytes) | Data EEPROM (bytes) | 10-bit A/D chan. | Timers (IC/OC/PWM) | Serial interfaces | I/0 wakeup pins |
|---|---|---|---|---|---|---|---|---|
| STM8AF/P62AA | LQFP80 (14x14) | 128 K | 6 K | 2 K | 16 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9) | LIN(UART), SPI, USART, I²C | 68/37 |
| STM8AF/P628A | | 64 K | | | | | | |
| STM8AF/P62A9 | LQFP64 (10x10) | 128 K | | | | | | 52/36 |
| STM8AF/P6289 | | 64 K | | 2 K | | | | |
| STM8AF/P6269 | | 32 K | | 1 K | | | | |
| STM8AF/P62A8 | LQFP48 (7x7) | 128 K | | 2 K | 10 | | | 38/35 |
| STM8AF/P6288 | | 64 K | | | | | | |
| STM8AF/P6286 | LQFP32 (7x7) | | | | 7 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8) | LIN(UART), SPI, I²C | 25/23 |
| STM8AF/P62A6 | VFQFPN32 (5x5) | 128 K | | | | | | |

## 5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain ($I^2C$ interface)

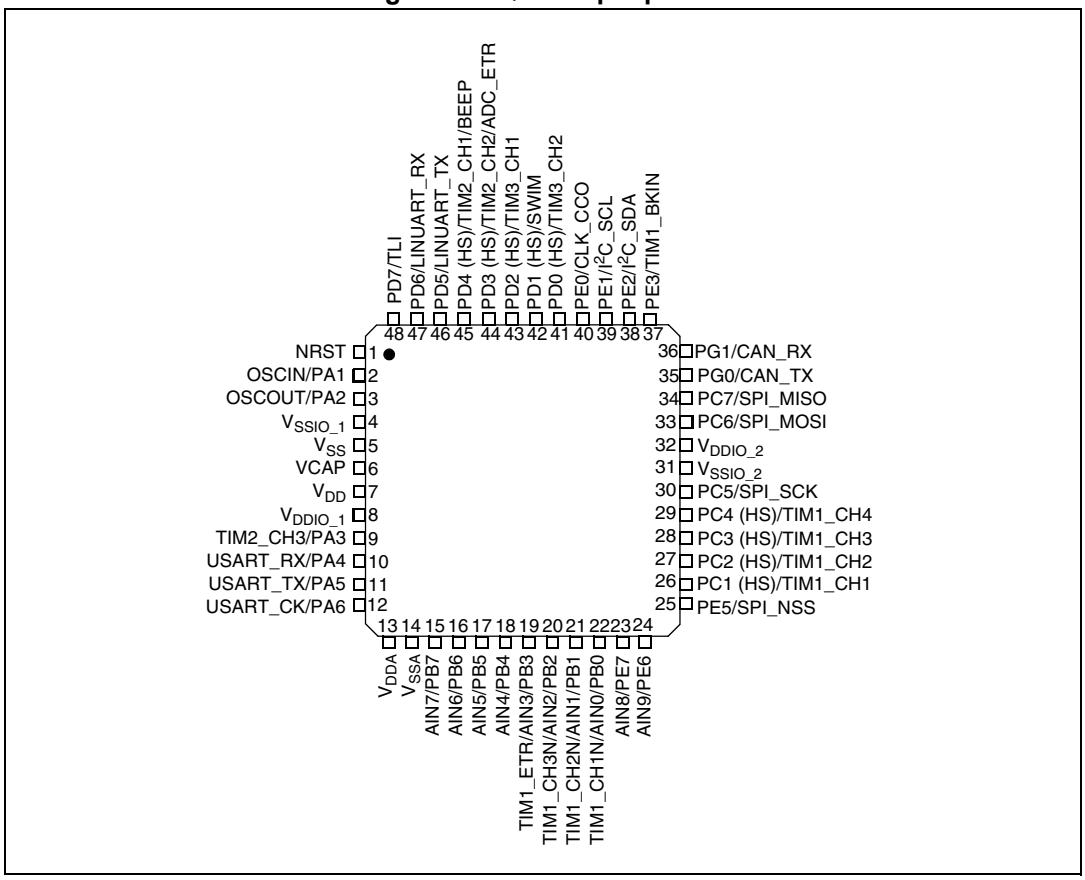
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

**Caution:** In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

**Figure 5. LQFP 48-pin pinout**




1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

**Table 14. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xXX |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF |
| 0x00 50CB | | Reserved area (1 byte) | | |
| 0x00 50CC | | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 bytes) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 bytes) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX(2) |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 bytes) | | | |

# 9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 18: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be changed in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

**Table 18. Option bytes**

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0x00 |
| 0x00 4801 | User boot code (UBC) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x00 4802 | | NOPT1 | NUBC[7:0] | | | | | | | | 0xFF |
| 0x00 4803 | Alternate function remapping (AFR) | OPT2 | AFR7 | AFR6 | AFR5 | AFR4 | AFR3 | AFR2 | AFR1 | AFR0 | 0x00 |
| 0x00 4804 | | NOPT2 | NAFR7 | NAFR6 | NAFR5 | NAFR4 | NAFR3 | NAFR2 | NAFR1 | NAFR0 | 0xFF |
| 0x00 4805 | Watchdog option | OPT3 | Reserved | | | | LSI_EN | IWDG_HW | WWDG_HW | WWDG_HALT | 0x00 |
| 0x00 4806 | | NOPT3 | Reserved | | | | NLSI_EN | NIWDG_HW | NWWDG_HW | NWWG_HALT | 0xFF |
| 0x00 4807 | Clock option | OPT4 | Reserved | | | | EXTCLK | CKAWUSEL | PRSC1 | PRSC0 | 0x00 |
| 0x00 4808 | | NOPT4 | Reserved | | | | NEXTCLK | NCKAWUSEL | NPRSC1 | NPRSC0 | 0xFF |
| 0x00 4809 | HSE clock startup | OPT5 | HSECNT[7:0] | | | | | | | | 0x00 |
| 0x00 480A | | NOPT5 | NHSECNT[7:0] | | | | | | | | 0xFF |

**Table 21. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDDIO}$ | Total current into $V_{DDIO}$ power lines (source)(1)(2)(3) | 100 | mA |
| $I_{VSSIO}$ | Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 20 | |
| | Output current source by any I/Os and control pin | -20 | |
| $I_{INJ(PIN)}$(4) | Injected current on any pin | ±10 | |
| $I_{INJ(TOT)}$ | Sum of injected currents | 50 | |

1. All power ($V_{DD}$, $V_{DDIO}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSIO}$, $V_{SSA}$) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. $V_{DDIO}$ includes the sum of the positive injection currents. $V_{SSIO}$ includes the sum of the negative injection currents.
4. This condition is implicitly insured if VIN maximum is respected. If VIN maximum cannot be respected, the injection current must be limited externally to the IINJ(PIN) value. A positive injection is induced by VIN > VDD while a negative injection is induced by VIN < VSS. For true open-drain pads, there is no positive injection current allowed and the corresponding VIN maximum must always be respected.

**Table 22. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| $T_J$ | Maximum junction temperature | 160 | |

**Table 23. Operating lifetime(1)**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| OLF | Conforming to AEC-Q100 rev G | -40 to 125 °C | Grade 1 |
| | | -40 to 150 °C | Grade 0 |

1. For detailed mission profile analysis, please contact the nearest ST Sales Office.

### Current consumption curves

*Figure 13* to *Figure 18* show typical current consumption measured with code executing in RAM.

**Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. $V_{DD}$ @$f_{CPU}$ = 16 MHz, peripherals = on**

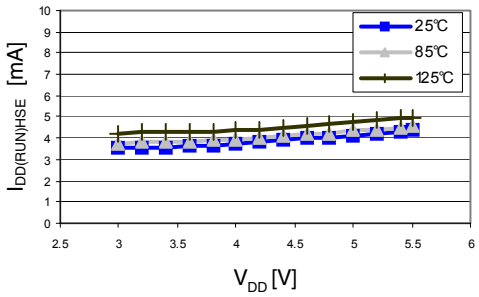



**Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. $f_{CPU}$ @ $V_{DD}$ = 5.0 V, peripherals = on**

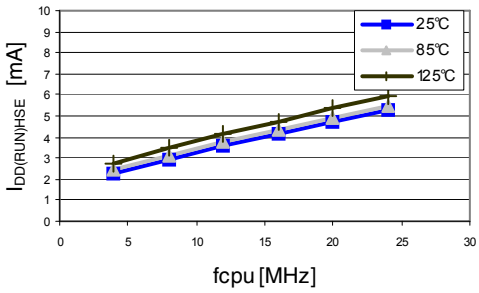



**Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = off**

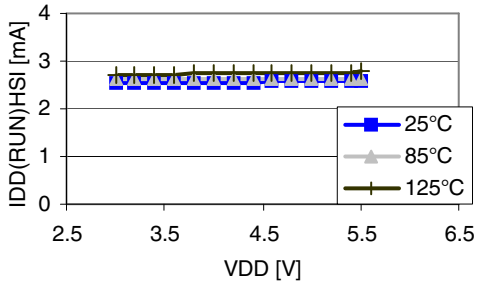



**Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = on**

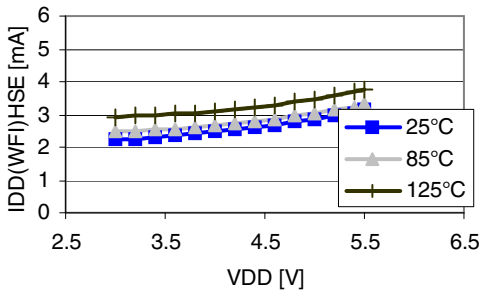



**Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. $f_{CPU}$ @ $V_{DD}$ = 5.0 V, peripherals = on**

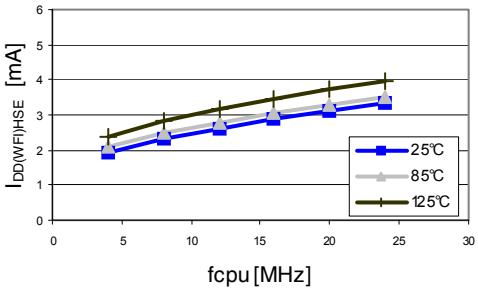



**Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = off**

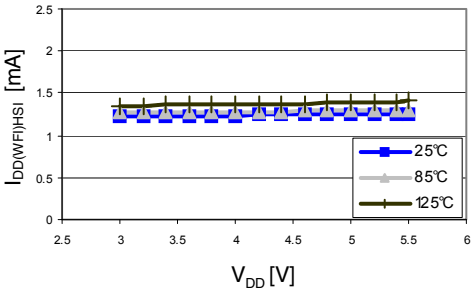
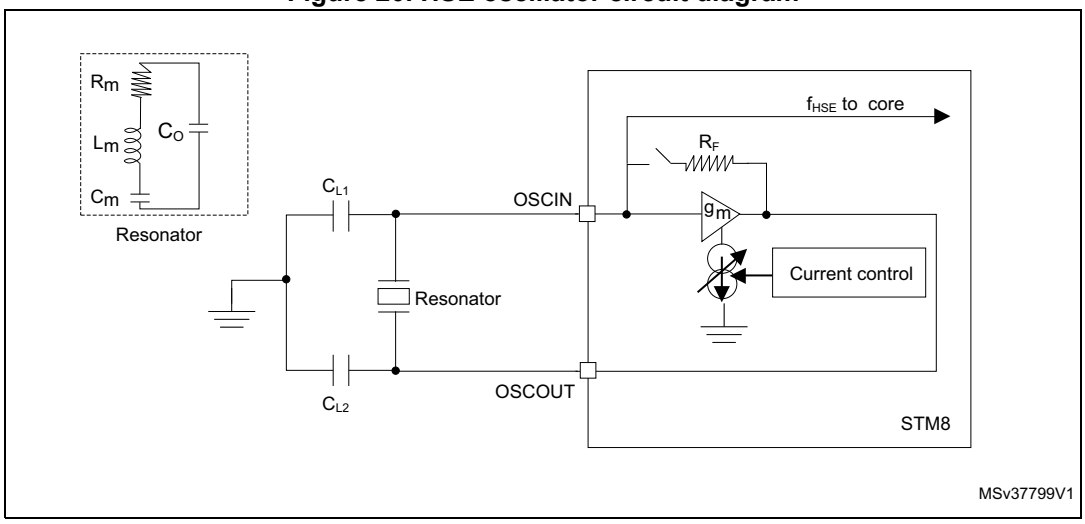


**Table 32. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 220 | - | kΩ |
| $C_{L1}/C_{L2}$ (1) | Recommended load capacitance | - | - | - | 20 | pF |
| $g_m$ | Oscillator trans conductance | - | 5 | - | - | mA/V |
| $t_{SU(HSE)}$ (2) | Startup time | $V_{DD}$ is stabilized | - | 2.8 | - | ms |

1. The oscillator needs two load capacitors, $C_{L1}$ and $C_{L2}$, to act as load for the crystal. The total load capacitance ($C_{Load}$) is $(C_{L1} * C_{L2})/(C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1/2}$. Some oscillators have built-in load capacitors, $C_{L1}$ and $C_{L2}$.
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 24 MHz oscillation is reached. It can vary with the crystal type that is used.

**Figure 20. HSE oscillator circuit diagram**




## HSE oscillator critical $g_m$ formula

The crystal characteristics have to be checked with the following formula:

**Equation 1**

$$g_m \gg g_{mcrit}$$

where $g_{mcrit}$ can be calculated with the crystal parameters as follows:

**Equation 2**

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

**$R_m$**: Notional resistance (see crystal specification)
**$L_m$**: Notional inductance (see crystal specification)
**$C_m$**: Notional capacitance (see crystal specification)
**Co**: Shunt capacitance (see crystal specification)
**$C_{L1} = C_{L2} = C$**: Grounded external capacitance

### 10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$.

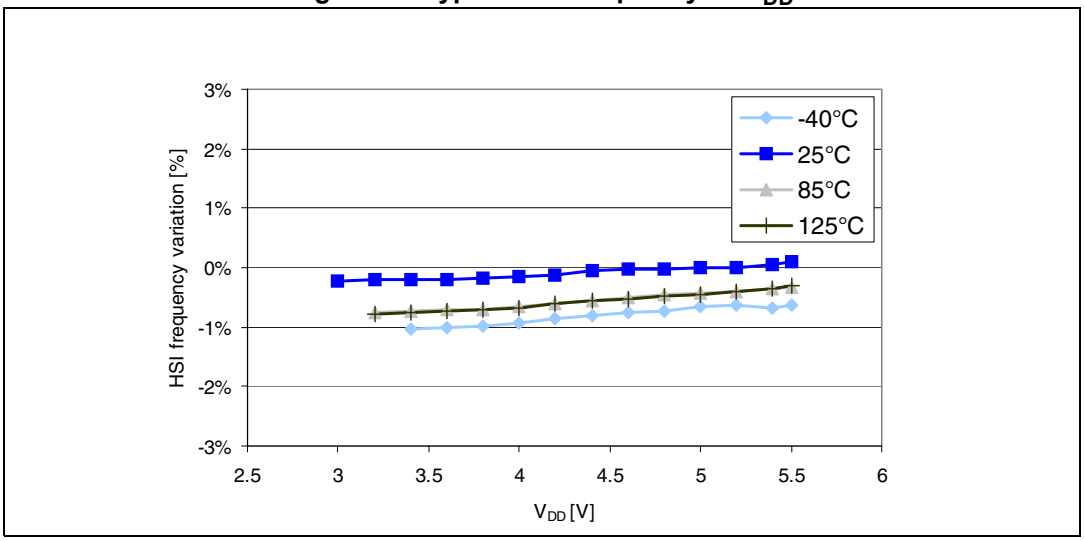
#### High-speed internal RC oscillator (HSI)

**Table 33. HSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HS}$ | HSI oscillator user trimming accuracy | Trimmed by the application for any $V_{DD}$ and $T_A$ conditions | -1 | - | 1 | % |
| | HSI oscillator accuracy (factory calibrated) | $V_{DD} = 3.0\ V \leq V_{DD} \leq 5.5\ V$, $-40\ °C \leq T_A \leq 150\ °C$ | -5 | - | 5 | |
| $t_{su(HSI)}$ | HSI oscillator wakeup time | - | - | - | 2(1) | µs |

1. Guaranteed by characterization results, not tested in production.

**Figure 21. Typical HSI frequency vs $V_{DD}$**



### 10.3.7 Reset pin characteristics

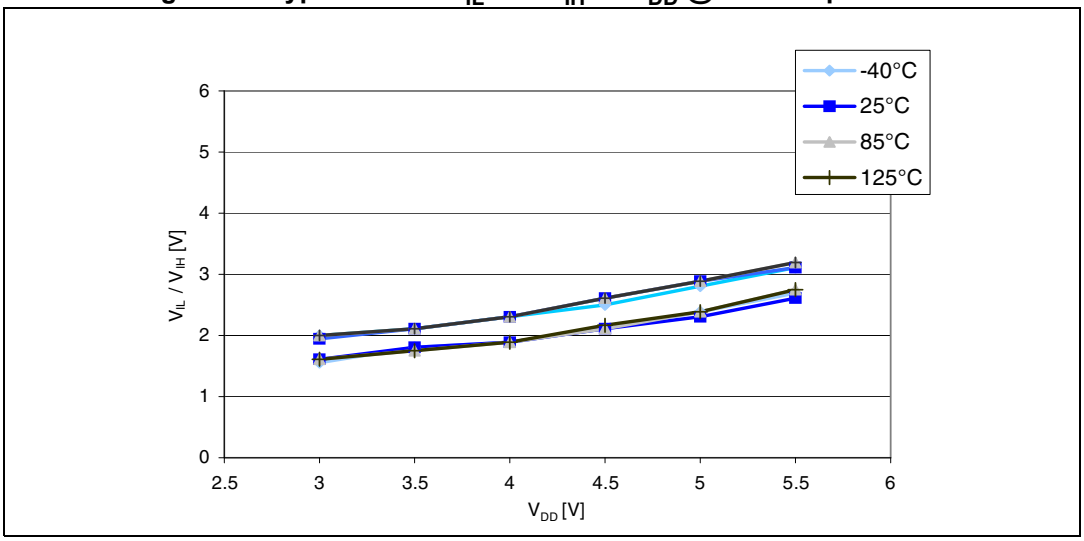
Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 39. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST low-level input voltage(1) | - | $V_{SS}$ | - | 0.3 x $V_{DD}$ | V |
| $V_{IH(NRST)}$ | NRST high-level input voltage(1) | - | 0.7 x $V_{DD}$ | - | $V_{DD}$ | |
| $V_{OL(NRST)}$ | NRST low-level output voltage(1) | $I_{OL}$ = 3 mA | - | - | 0.6 | |
| $R_{PU(NRST)}$ | NRST pull-up resistor | - | 30 | 40 | 60 | kΩ |
| $t_{IFP}$ | NRST input filtered pulse(1) | - | 85 | - | 315 | ns |
| $t_{INFP(NRST)}$ | NRST Input not filtered pulse duration(2) | - | 500 | - | - | |

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

**Figure 36. Typical NRST $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ four temperatures**



### Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

**Table 46. EMI data**

| Symbol | Parameter | Conditions | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | General conditions | Monitored frequency band | Max $f_{CPU}$(1) | | | |
| | | | | 8 MHz | 16 MHz | 24 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP80 package conforming to IEC 61967-2 | 0.1 MHz to 30 MHz | 15 | 17 | 22 | dBµV |
| | | | 30 MHz to 130 MHz | 18 | 22 | 16 | |
| | | | 130 MHz to 1 GHz | -1 | 3 | 5 | |
| | EMI level | | - | 2 | 2.5 | 2.5 | |

1. Guaranteed by characterization results, not tested in production.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

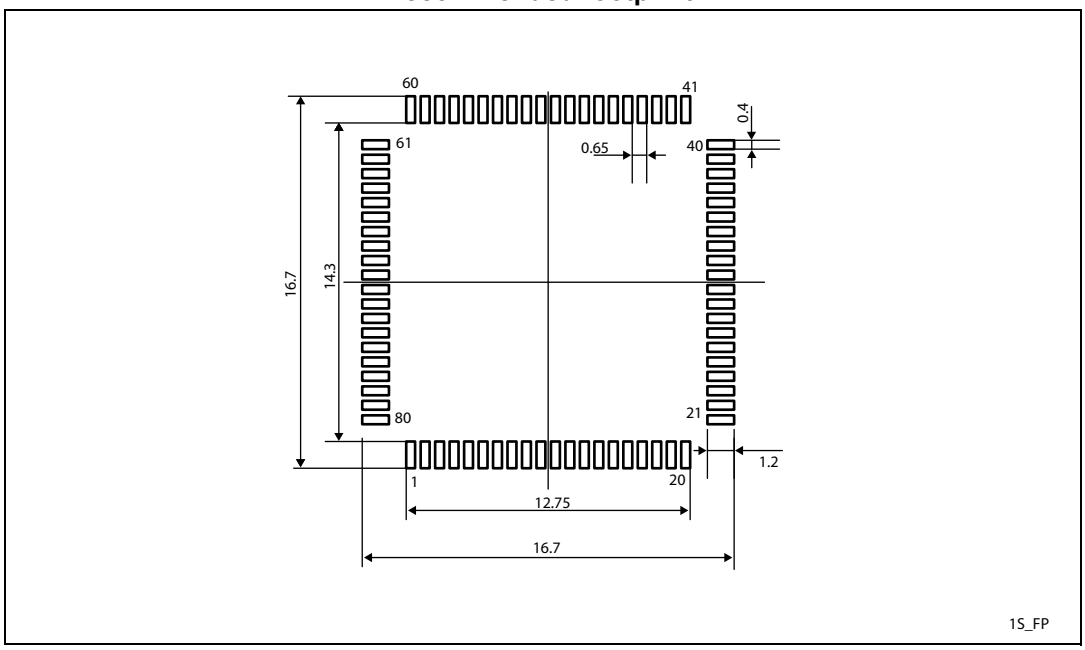
Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**Table 47. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = 25 °C, conforming to JESD22-A114 | 3A | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-C101 | 3 | 500 | |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-A115 | B | 200 | |

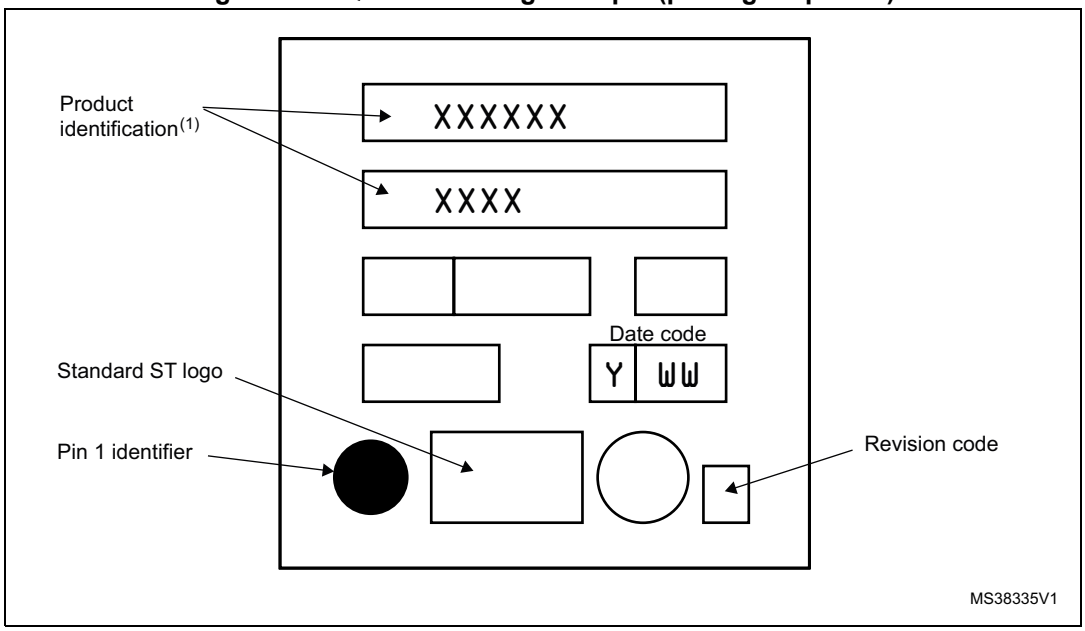
1. Guaranteed by characterization results, not tested in production

**Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint**



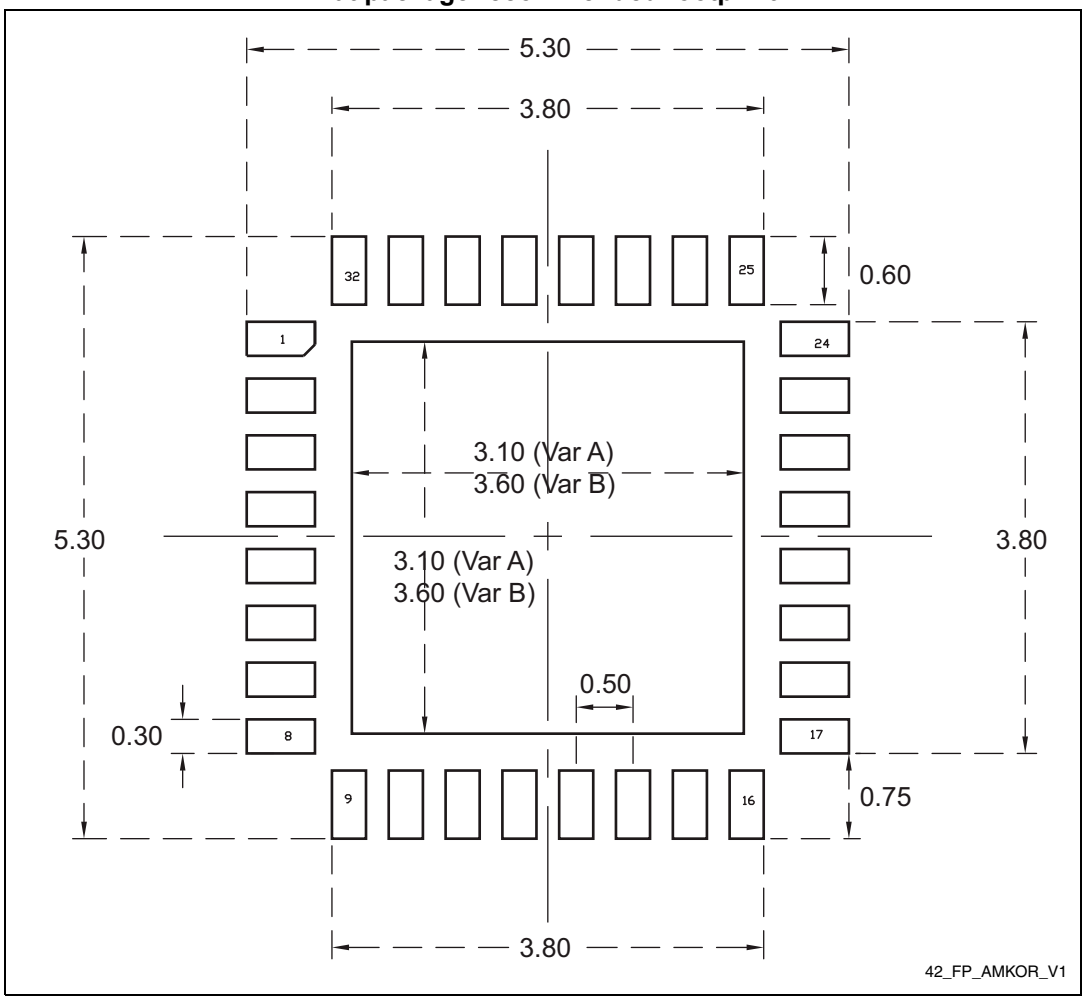

1. Dimensions are expressed in millimeters.

**Figure 53. LQFP48 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

**Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 11.6 Thermal characteristics

In case the maximum chip junction temperature ($T_{Jmax}$) specified in *Table 24: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

$T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

**$T_{Amax}$** is the maximum ambient temperature in °C

**$\Theta_{JA}$** is the package junction-to-ambient thermal resistance in ° C/W

**$P_{Dmax}$** is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

**$P_{INTmax}$** is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

**$P_{I/Omax}$** represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low- and high-level in the application.

**Table 54. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm | 38 | °C/W |
| | Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm | 46 | |
| | Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm | 57 | |
| | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 59 | |
| | Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm | 25 | |

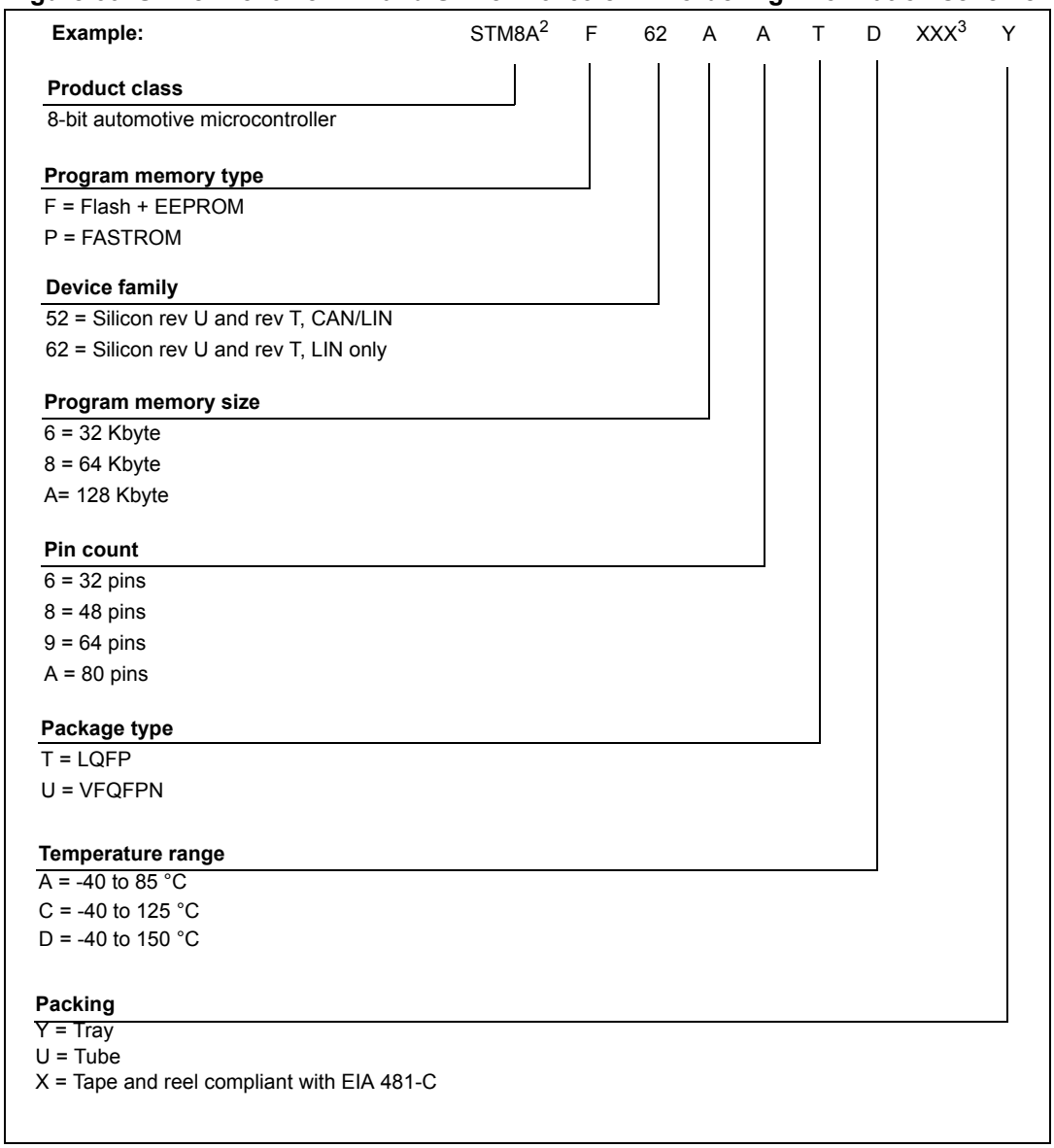
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

### 11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

# 12 Ordering information

**Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme[1]**




1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 01-Jul-2009 | 4 (continued) | Removed table*: Total current consumption and timing in halt, fast active halt and slow active halt modes at $V_{DD}$ = 3.3 V.*<br>Added *Table 28: Oscillator current consumption.*<br>Added *Table 29: Programming current consumption.*<br>Updated *Table 30: Typical peripheral current consumption VDD = 5.0 V*<br>Updated *Table 31: HSE external clock characteristics.*<br>Updated *Table 32: HSE oscillator characteristics.*<br>*Table 20: HSE oscillator circuit diagram:* changed 'consumption control' to 'current control'<br>*Section : HSE oscillator critical gm formula:* clarified formula<br>Updated *Table 33: HSI oscillator characteristics.*<br>Removed *'RAM and hardware registers'*<br>Removed *Table: RAM and hardware registers.*<br>Updated *Table 35: Flash program memory/data EEPROM memory*<br>Added *Table 36: Flash program memory.*<br>Added *Table 37: Data memory.*<br>Updated *Table 38: I/O static characteristics.*<br>Updated *Table 39: NRST pin characteristics.*<br>Updated *Table 40: TIM 1, 2, 3, and 4 electrical specifications*<br>*Section 10.3.9: SPI interface:* changed title from "SPI serial peripheral interface".<br>Updated *Table 41: SPI characteristics.*<br>*Figure 40: SPI timing diagram in slave mode and with CPHA = 0*: Changed title and added footnote.<br>*Figure 41: SPI timing diagram in slave mode and with CPHA = 1:* changed the title.<br>Updated *Table 43: ADC characteristics.*<br>Updated *Figure 43: Typical application with ADC.*<br>Removed *Table: ADC accuracy for VDDA = 3.3 V.*<br>Updated *Table 44: ADC accuracy for VDDA = 5 V.*<br>Updated *Table 46: EMI data.*<br>Updated *Table 48: Electrical sensitivities.*<br>Added text about Ecopack in the *Section 11: Package information.*<br>*Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline:* deleted footnote.<br>Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*.<br>Added *Section 13: STM8 development tools.* |
| 22-Oct-2009 | 5 | Updated *Table 1: Device summary*: added STM8AF5178, STM8AF519A and STM8AF619A. |

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 13-Oct-2016 | 14 | Updated:<br>– Title of *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout*, (previously STM8AF5286UC VFQFPN32 32-pin pinout)<br>– Footnotes of *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*<br>– *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* replaced “STM8AF5286UC VQFPN32” with “STM8AF52x6 VQFPN32” at header row<br>– *Section 10.2: Absolute maximum ratings*<br>– *Section : Device marking on page 93*<br>– *Section : Device marking on page 96*<br>– *Section : Device marking on page 99*<br>– *Section : Device marking on page 104*<br>– *Section : Device marking on page 108*<br>Added:<br>– Footnote on *Figure 47: LQFP80 marking example (package top view)*, *Figure 50: LQFP64 marking example (package top view)*, *Figure 56: LQFP32 marking example (package top view)*, *Figure 59: VFQFPN32 marking example (package top view)*. |
| 10-Nov-2016 | 15 | Updated header row and PA6/USART_CK pin row on *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*. |