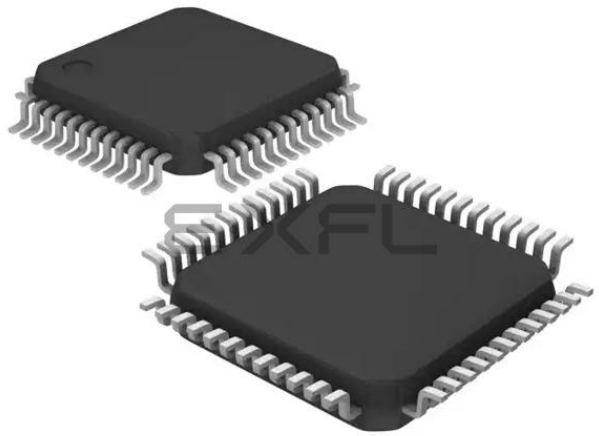

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a8tcx

1 Introduction

This datasheet refers to the STM8AF526x/8x/Ax and STM8AF6269/8x/Ax products with 32 to 128 Kbyte of program memory.

In the order code, the letter ‘F’ refers to product versions with Flash and data EEPROM and ‘P’ to product versions with FASTROM. The identifiers ‘F’ and ‘P’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S and STM8A Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

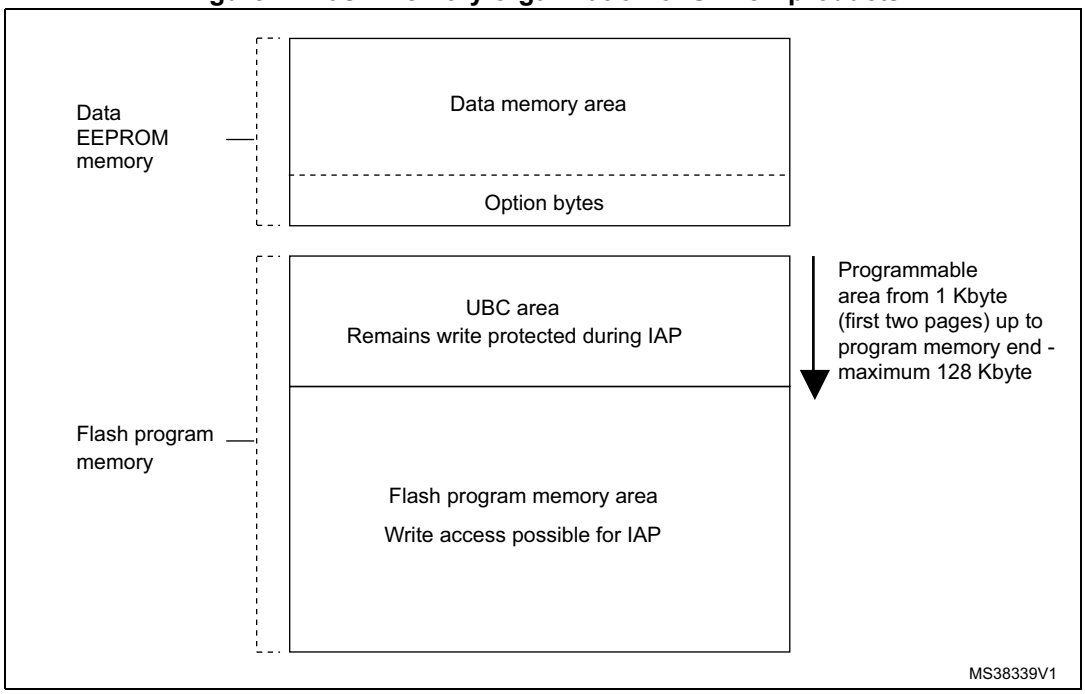
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 54*).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

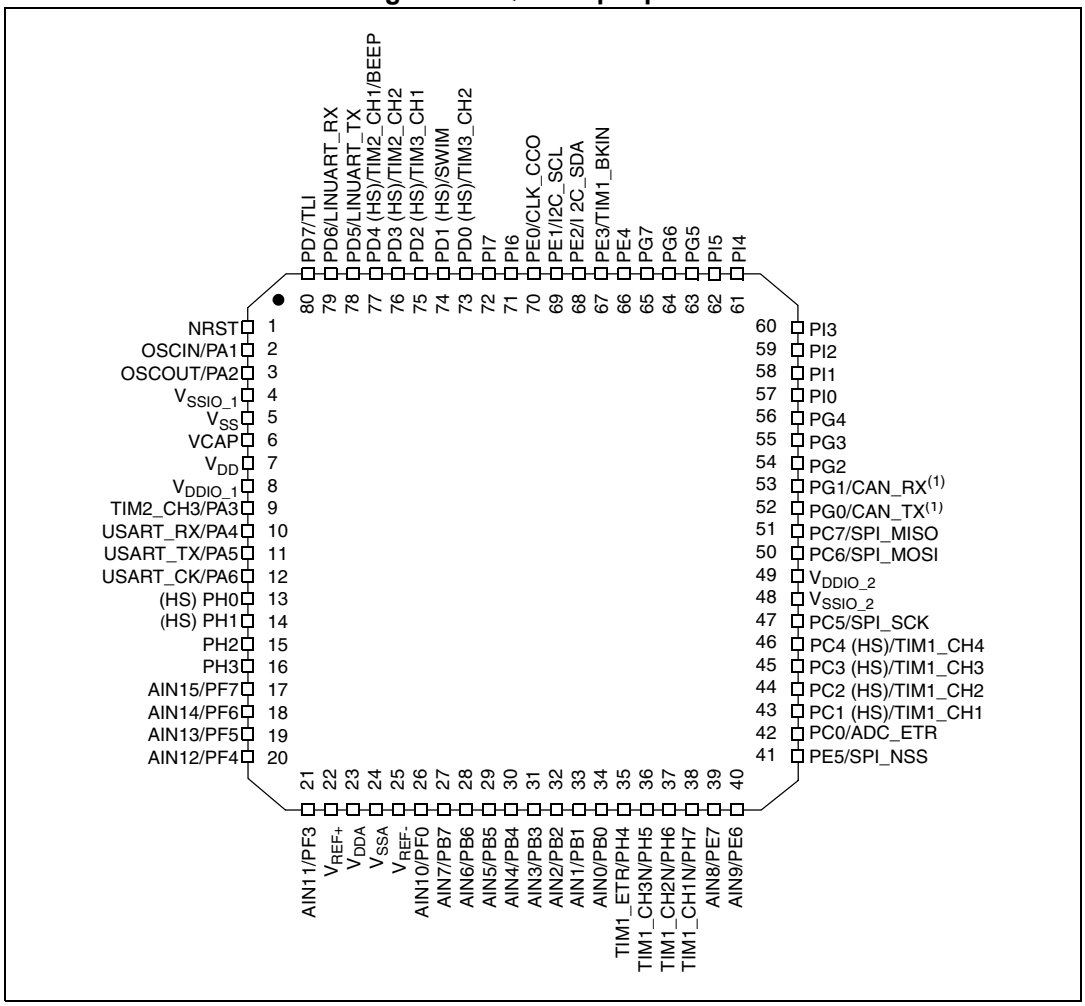
STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. (HS) stands for high sink capability.

Table 10. Legend/abbreviation for the pin description table

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = high sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
55	46	-	-	-	PG3	I/O	**X**	X	-	-	O1	X	X	**Port G3**	-	-
56	47	-	-	-	PG4	I/O	**X**	X	-	-	O1	X	X	**Port G4**	-	-
57	48	-	-	-	PI0	I/O	**X**	X	-	-	O1	X	X	**Port I0**	-	-
58	-	-	-	-	PI1	I/O	**X**	X	-	-	O1	X	X	**Port I1**	-	-
59	-	-	-	-	PI2	I/O	**X**	X	-	-	O1	X	X	**Port I2**	-	-
60	-	-	-	-	PI3	I/O	**X**	X	-	-	O1	X	X	**Port I3**	-	-
61	-	-	-	-	PI4	I/O	**X**	X	-	-	O1	X	X	**Port I4**	-	-
62	-	-	-	-	PI5	I/O	**X**	X	-	-	O1	X	X	**Port I5**	-	-
63	49	-	-	-	PG5	I/O	**X**	X	-	-	O1	X	X	**Port G5**	-	-
64	50	-	-	-	PG6	I/O	**X**	X	-	-	O1	X	X	**Port G6**	-	-
65	51	-	-	-	PG7	I/O	**X**	X	-	-	O1	X	X	**Port G7**	-	-
66	52	-	-	-	PE4	I/O	**X**	X	X	-	O1	X	X	**Port E4**	-	-
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
68	54	38	-	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port E2**	I^2C data	-
69	55	39	-	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port E1**	I^2C clock	-
70	56	40	-	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
71	-	-	-	-	PI6	I/O	**X**	X	-	-	O1	X	X	**Port I6**	-	-
72	-	-	-	-	PI7	I/O	**X**	X	-	-	O1	X	X	**Port I7**	-	-
73	57	41	25	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
75	59	43	27	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	28	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]

8 Interrupt table

Table 17. STM8A interrupt table(1)

Priority	Source block	Description	Interrupt vector address	Wakeup from Halt	Comments
-	Reset	Reset	0x00 8000	Yes	-
-	TRAP	SW interrupt	0x00 8004	-	-
0	TLI	External top level interrupt	0x00 8008	-	-
1	AWU	Auto-wakeup from Halt	0x00 800C	Yes	-
2	Clock controller	Main clock controller	0x00 8010	-	-
3	MISC	External interrupt E0	0x00 8014	Yes	Port A interrupts
4	MISC	External interrupt E1	0x00 8018	Yes	Port B interrupts
5	MISC	External interrupt E2	0x00 801C	Yes	Port C interrupts
6	MISC	External interrupt E3	0x00 8020	Yes	Port D interrupts
7	MISC	External interrupt E4	0x00 8024	Yes	Port E interrupts
8	CAN	CAN interrupt Rx	0x00 8028	Yes	-
9	CAN	CAN interrupt TX/ER/SC	0x00 802C	-	-
10	SPI	End of transfer	0x00 8030	Yes	-
11	Timer 1	Update/overflow/ trigger/break	0x00 8034	-	-
12	Timer 1	Capture/compare	0x00 8038	-	-
13	Timer 2	Update/overflow	0x00 803C	-	-
14	Timer 2	Capture/compare	0x00 8040	-	-
15	Timer 3	Update/overflow	0x00 8044	-	-
16	Timer 3	Capture/compare	0x00 8048	-	-
17	USART	Tx complete	0x00 804C	-	-
18	USART	Receive data full reg.	0x00 8050	-	-
19	I^2C	I^2C interrupts	0x00 8054	Yes	-
20	LINUART	Tx complete/error	0x00 8058	-	-
21	LINUART	Receive data full reg.	0x00 805C	-	-
22	ADC	End of conversion	0x00 8060	-	-
23	Timer 4	Update/overflow	0x00 8064	-	-
24	EEPROM	End of programming/ write in not allowed area	0x00 8068	-	-

1. All unused interrupts must be initialized with ‘IRET’ for robust programming.

Table 19. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0xFF: Pages 4 to 255 defined as UBC, memory write-protected *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. **AFR4: Alternate function remapping option 4** 0: Port D7 alternate function = TLI 1: Reserved **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Table 27. Total current consumption in Halt and Active-halt modes. General conditions for V_{DD} applied. T_A = -40 °C to 55 °C unless otherwise stated

Symbol	Parameter	Conditions			Typ	Max	Unit
		Main voltage regulator (MVR)(1)	Flash mode(2)	Clock source and temperature condition			
$I_{DD(H)}$	Supply current in Halt mode	Off	Power-down	Clocks stopped	5	35(3)	µA
				Clocks stopped, T_A = 25 °C	5	25	
$I_{DD(AH)}$	Supply current in Active-halt mode with regulator on	On	Power-down	External clock 16 MHz f_{MASTER} = 125 kHz	770	900(3)	
				LSI clock 128 kHz	150	230(3)	
	Supply current in Active-halt mode with regulator off	Off	Power-down	LSI clock 128 kHz	25	42(3)	
				LSI clock 128 kHz, T_A = 25 °C	25	30	
$t_{WU(AH)}$	Wakeup time from Active-halt mode with regulator on	On	Operating mode	T_A = -40 to 150 °C	10	30(3)	µs
	Wakeup time from Active-halt mode with regulator off	Off			50	80(3)	

1. Configured by the REGAH bit in the CLK_ICKR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.
3. Guaranteed by characterization results, not tested in production.

Current consumption for on-chip peripherals

Table 28. Oscillator current consumption

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 5 V	f_{OSC} = 24 MHz	1	2.0(3)	mA
			f_{OSC} = 16 MHz	0.6	-	
			f_{OSC} = 8 MHz	0.57	-	
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 3.3 V	f_{OSC} = 24 MHz	0.5	1.0(3)	
			f_{OSC} = 16 MHz	0.25	-	
			f_{OSC} = 8 MHz	0.18	-	

1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Informative data.

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

High-speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} = 3.0\ V \leq V_{DD} \leq 5.5\ V$, $-40\ °C \leq T_A \leq 150\ °C$	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 21. Typical HSI frequency vs V_{DD}

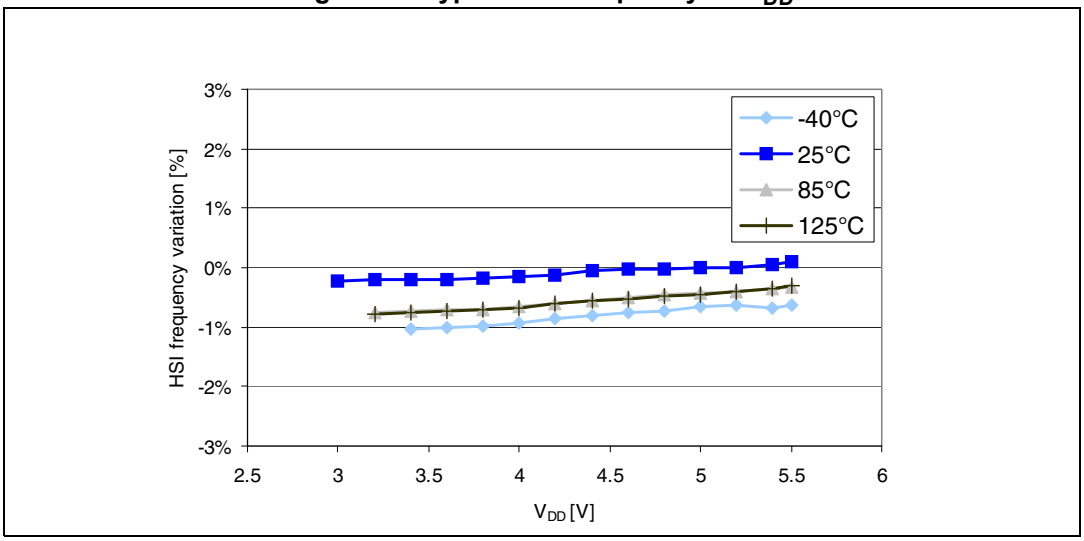
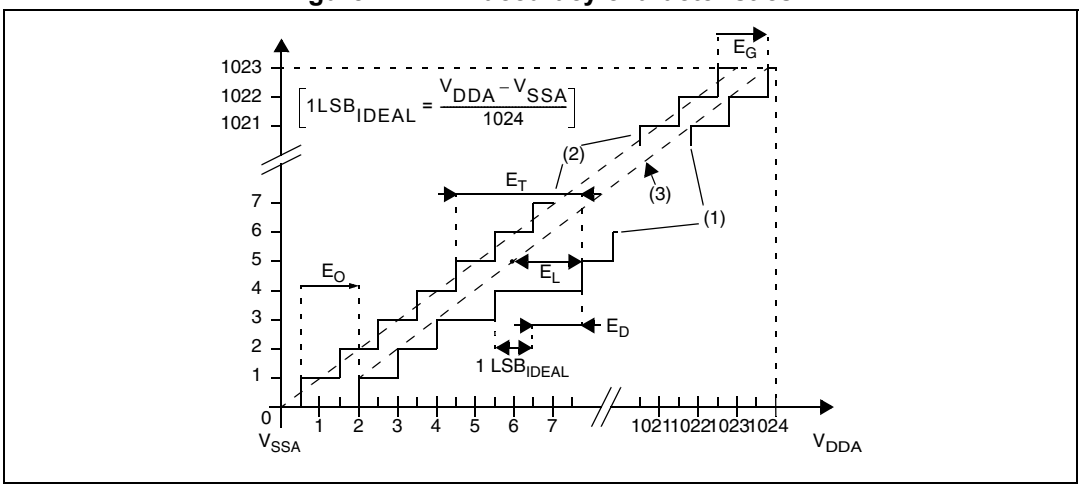


Table 44. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



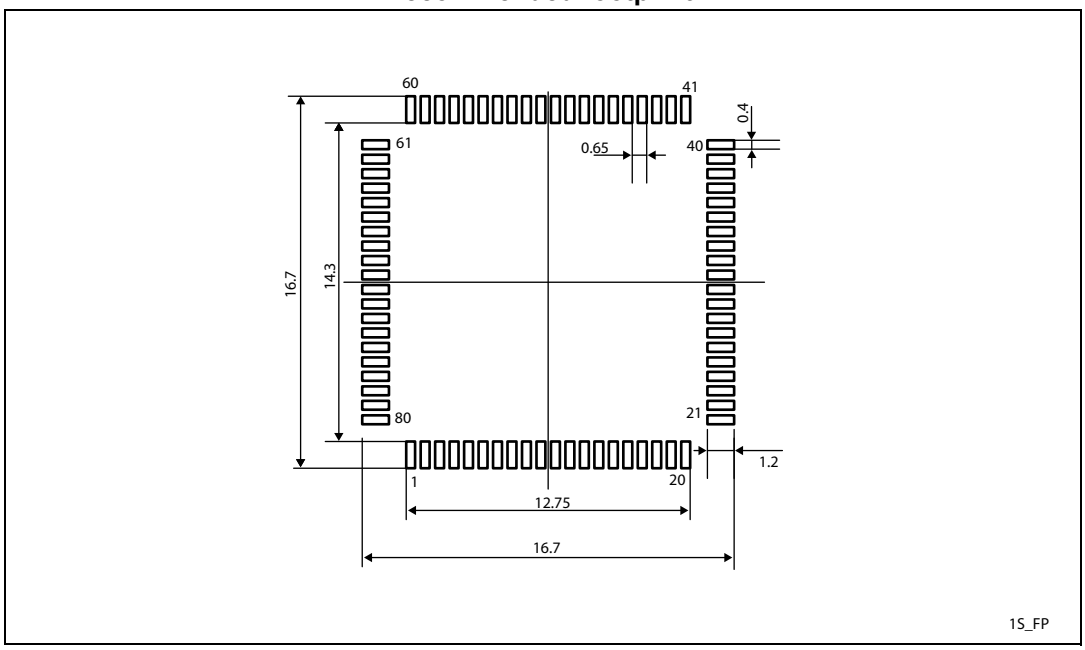
1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Table 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

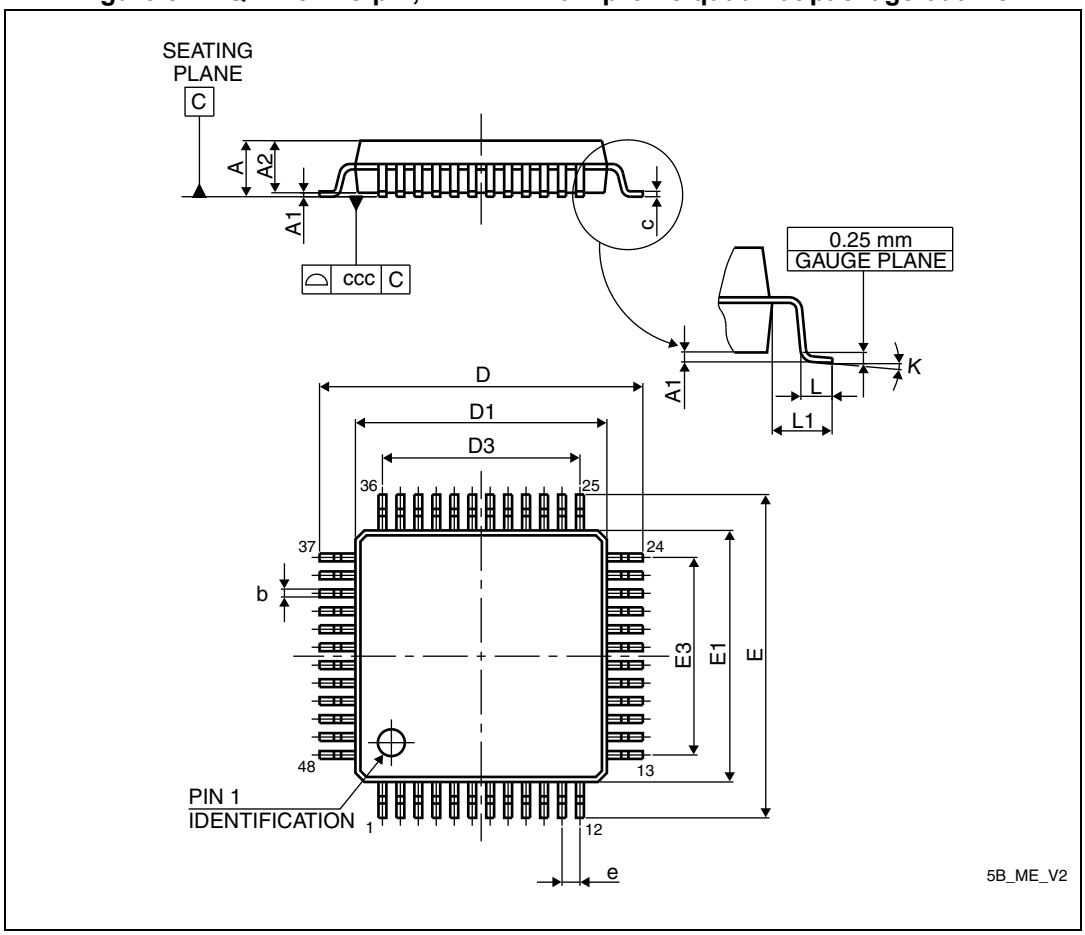
Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

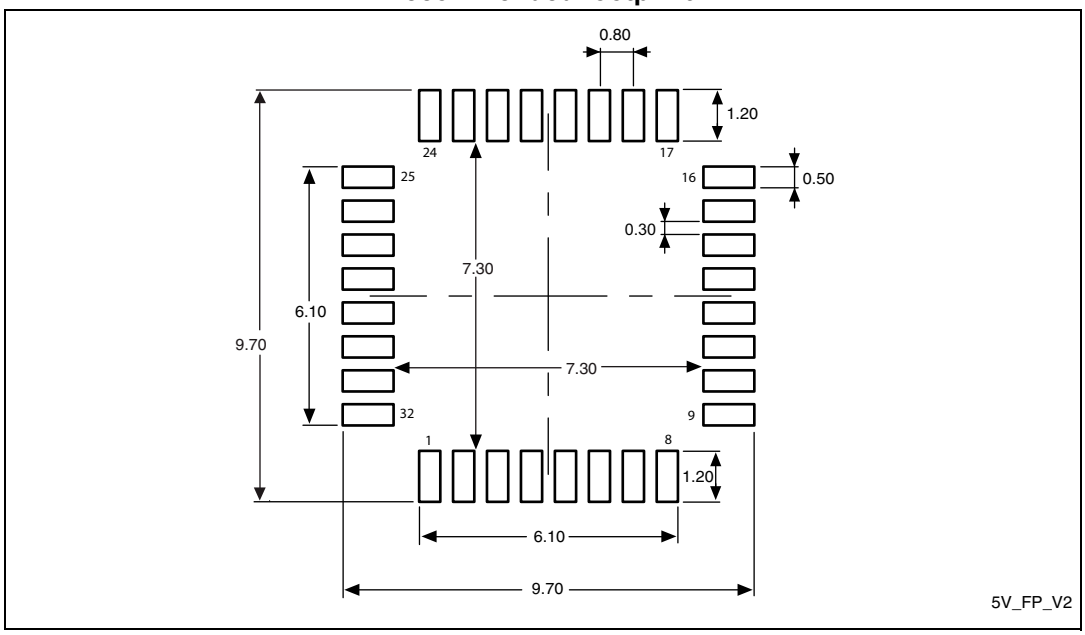
11.3 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 55. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.6 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 24: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low- and high-level in the application.

Table 54. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	25	

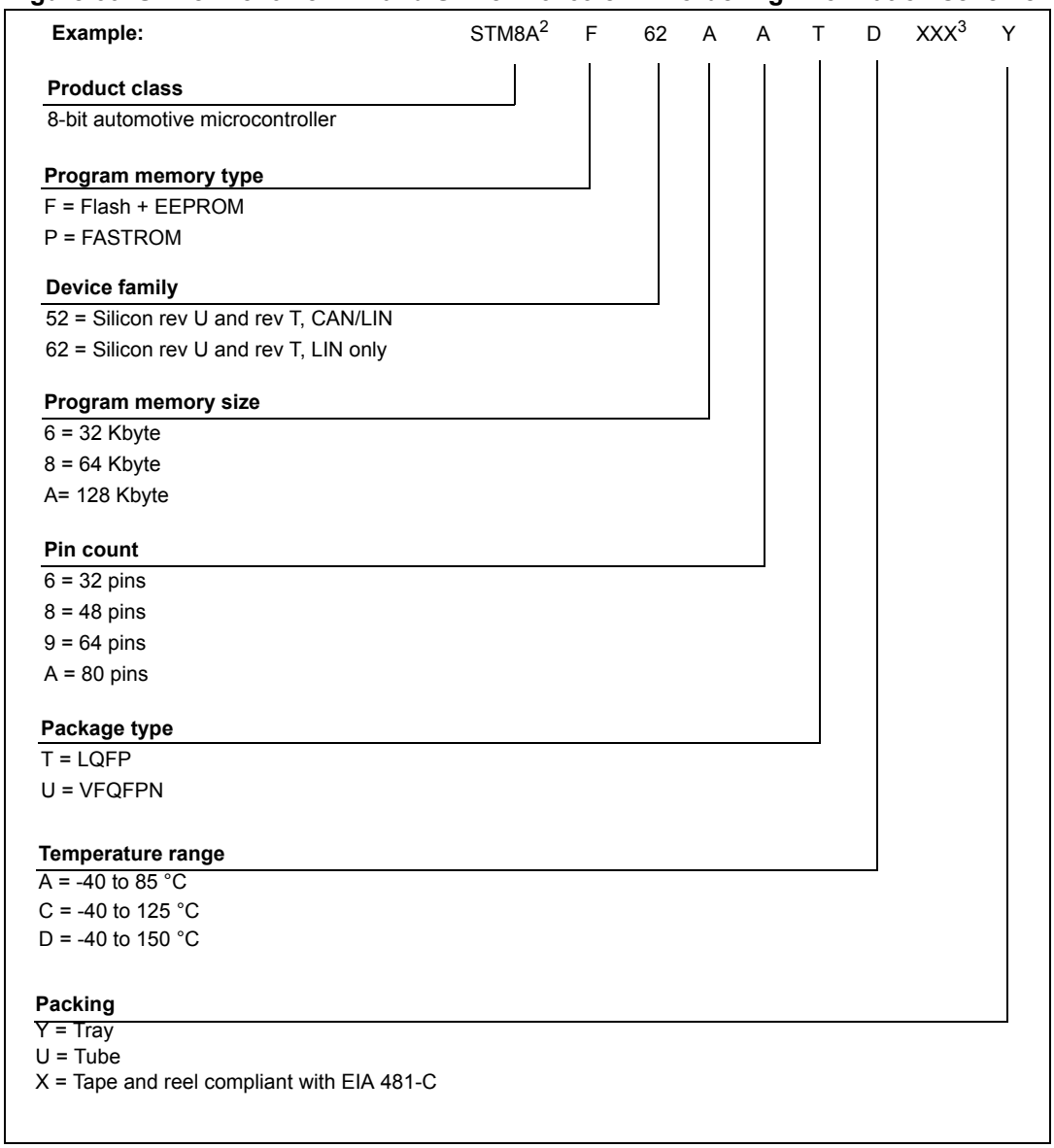
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12 Ordering information

Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme[1]



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8 (continued)	Removed note 1 in *Table 24: General operating conditions* and note 1 below *Figure 11: fCPUmax versus VDD*. Removed note 3 in *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C*. Removed note 2 in *Table 31: HSE external clock characteristics* and *Table 35: Flash program memory/data EEPROM memory* Removed note 1 in *Table 37: Data memory*. Modified T_{WE} maximum value in *Table 36: Flash program memory* and *Table 37: Data memory*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table 39: NRST pin characteristics*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 39: Recommended reset pin protection,* and updated external capacitor value. Updated *Note 1* in *Table 40: TIM 1, 2, 3, and 4 electrical specifications.* Updated *Note 1* in *Table 41: SPI characteristics.* Moved know limitations to separate errata sheet. Added “not recommended for new design” note to device family 51, memory size 7 and 9, and temperature range B, in *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added Raisonance compiler in *Section 13.2: Software tools.*
18-Jul-2012	9	Updated wildcards of document part numbers. Added VFQFPN package. Added STM8AF62A6 part number. *Table 1: Device summary* updated footnote *1* and added footnote *2*. *Table: STM8AF52xx product line-up with CAN* and *Table: STM8AF62xx product line-up without CAN*: added “P” version for all order codes; updated size of data EEPROM for 64K devices to 2K instead of 1.5K; updated RAM. *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram*: updated POR, BOR and WDG; removed PDR; added legend. *Section 5.4: Flash program and data EEPROM*: removed non relevant bullet points and added a sentence about the factory program. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)* and updated *Table 5: Peripheral clock gating bits (CLK_PCKENR2)* *Section : ADC features*: updated ADC input range. *Table 12: Memory model 128K:* updated RAM size, RAM end addresses, and stack roll-over addresses; updated footnote *1* *Table 18: Option bytes:* updated factory default setting for NOPT17; updated footnotes. *Table 20: Voltage characteristics:* updated V_{DDX} - V_{DD} to V_{DDX} - V_{SS}. *Table 24: General operating conditions:* updated V_{CAP}.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-Jul-2012	9 (continued)	*Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* updated conditions for $I_{DD(RUN)}$. *Table 38: I/O static characteristics:* added new condition and new max values for rise and fall time; updated footnote 2. *Section 10.3.7: Reset pin characteristics:* updated text below *Figure 38: Typical NRST pull-up current Ipu vs VDD* *Figure 39: Recommended reset pin protection:* updated unit of capacitor. *Table 41: SPI characteristics:* updated SCK high and low time conditions and values. *Figure 42: SPI timing diagram - master mode:* replaced 'SCK input' signals with 'SCK output' signals. Updated *Table 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data* Replaced *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* Added *Figure 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint* *and* *Figure 55: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* Updated *Figure 57: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline* Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1* *Section 13.2.2: C and assembly toolchains:* added www.iar.com.
31-Mar-2014	10	Updated: – *Table 1: Device summary*, – *Table: STM8AF52xx product line-up with CAN*, – *Table: STM8AF/H/P51xx product line-up with CAN*, – *Table: STM8AF/H/P61xx product line-up without CAN*, – *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*, – The maximum speed in *Section 5.9.3: Serial peripheral interface (SPI)*, – t_{TEMP} Reset release delay /VDD rising typical and max values in *Table 25: Operating conditions at power-up/power-down*, – The symbol $t_{IFP(NRST)}$ with $t_{INFP(NRST)}$ in *Table 39: NRST pin characteristics*, – The address and comment for Reset in *Table 17: STM8A interrupt table*.