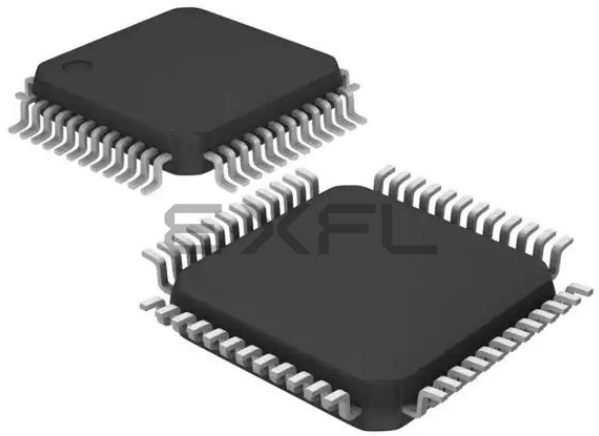

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a8tcy

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3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P5289		64 K						
STM8AF/P5269		32 K		1 K				
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K		1K				
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I²C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I²C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P6289		64 K		2 K				
STM8AF/P6269		32 K		1 K				
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P6288		64 K						
STM8AF/P6286	LQFP32 (7x7)				7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P62A6	VFQFPN32 (5x5)	128 K						

1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

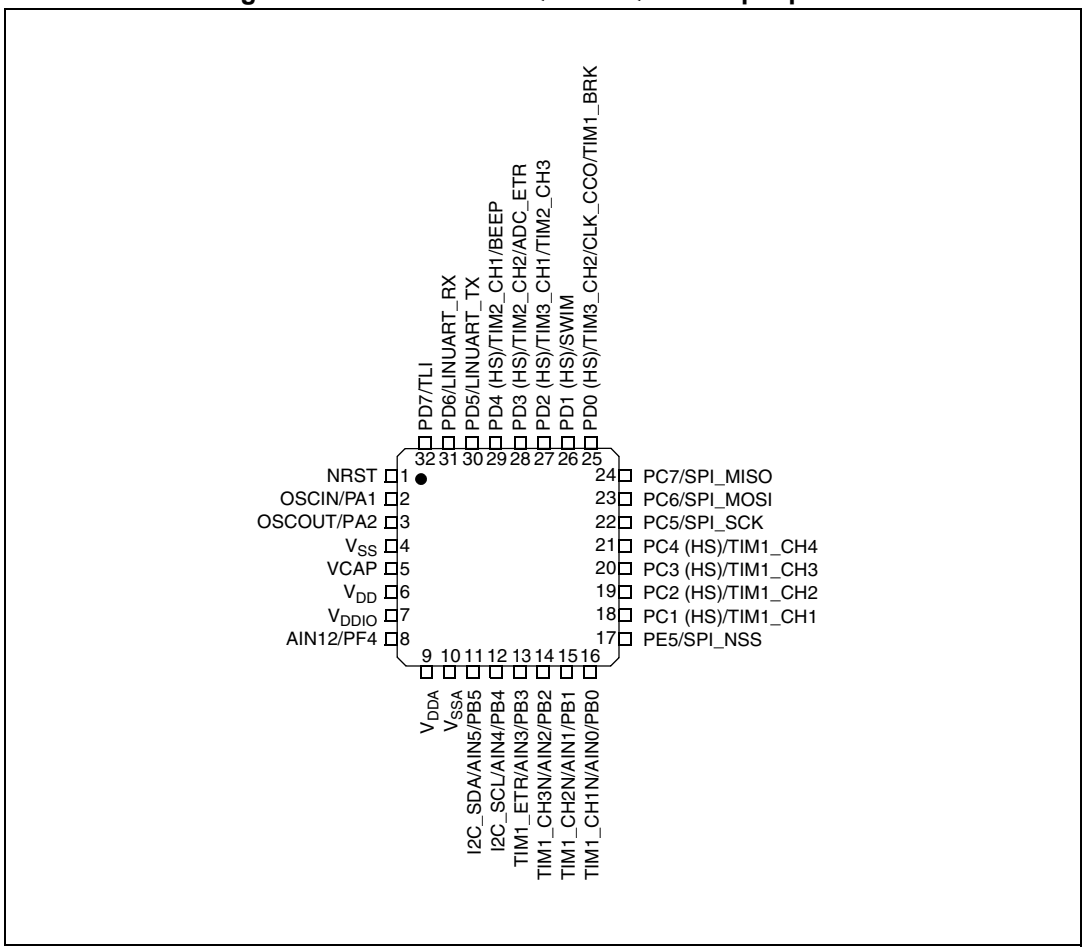
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout



1. HS stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	2	2	2	PA1/OSCIN(1)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/ crystal in	-
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	4	4	-	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	5	5	4	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	6	6	5	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	7	7	6	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	8	7	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	10	10	-	-	PA4/USART_RX	I/O	**X**	X	X	-	O3	X	X	**Port A4**	USART receive	-
11	11	11	-	-	PA5/USART_TX	I/O	**X**	X	X	-	O3	X	X	**Port A5**	USART transmit	-
12	12	12	-	8	PA6/USART_CK (2)	I/O	**X**	X	X	-	O3	X	X	**Port A6**	USART synchro nous clock	-
13	-	-	-	-	PH0	I/O	X	X	-	HS	O3	X	X	**Port H0**	-	-
14	-	-	-	-	PH1	I/O	**X**	X	-	HS	O3	X	X	**Port H1**	-	-
15	-	-	-	-	PH2	I/O	**X**	X	-	-	O1	X	X	**Port H2**	-	-
16	-	-	-	-	PH3	I/O	**X**	X	-	-	O1	X	X	**Port H3**	-	-
17	13	-	-	-	PF7/AIN15	I/O	**X**	X	-	-	O1	X	X	**Port F7**	Analog input 15	-
18	14	-	-	-	PF6/AIN14	I/O	**X**	X	-	-	O1	X	X	**Port F6**	Analog input 14	-
19	15	-	-	-	PF5/AIN13	I/O	**X**	X	-	-	O1	X	X	**Port F5**	Analog input 13	-
20	16	-	8	-	PF4/AIN12	I/O	**X**	X	-	-	O1	X	X	**Port F4**	Analog input 12	-
21	17	-	-	-	PF3/AIN11	I/O	**X**	X	-	-	O1	X	X	**Port F3**	Analog input 11	-

Table 12. Memory model 128K

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
128 K	0x00 27FFF	6 K	0x00 17FF	0x00 1400
64 K	0x00 17FFF			
32 K	0x00 0FFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 13. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

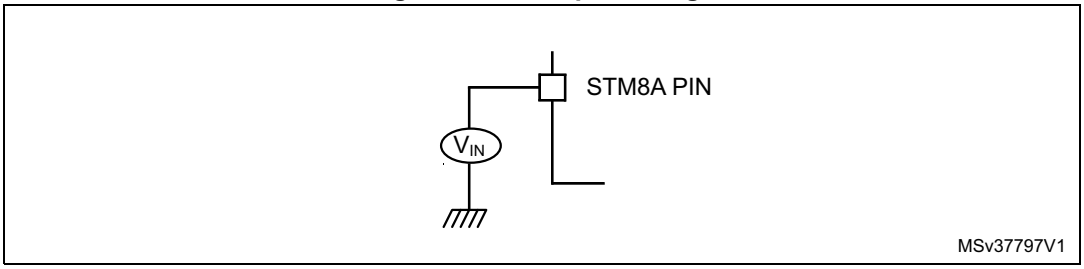
Table 19. Option byte description (continued)

Option byte no.	Description
OPT12	**TMU_KEY 5 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	**TMU_KEY 6 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	**TMU_KEY 7 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	**TMU_KEY 8 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	**BL[7:0]: Bootloader enable** If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics* and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability. The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 20. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 88*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 21. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDDIO}	Total current into V_{DDIO} power lines (source)(1)(2)(3)	100	mA
I_{VSSIO}	Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(4)	Injected current on any pin	±10	
$I_{INJ(TOT)}$	Sum of injected currents	50	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. V_{DDIO} includes the sum of the positive injection currents. V_{SSIO} includes the sum of the negative injection currents.
4. This condition is implicitly insured if VIN maximum is respected. If VIN maximum cannot be respected, the injection current must be limited externally to the IINJ(PIN) value. A positive injection is induced by VIN > VDD while a negative injection is induced by VIN < VSS. For true open-drain pads, there is no positive injection current allowed and the corresponding VIN maximum must always be respected.

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	160	

Table 23. Operating lifetime(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100 rev G	-40 to 125 °C	Grade 1
		-40 to 150 °C	Grade 0

1. For detailed mission profile analysis, please contact the nearest ST Sales Office.

Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 °C to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 24 MHz 1 ws	8.7	16.8(2)	mA
			f_{CPU} = 16 MHz	7.4	14	
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	f_{CPU} = 24 MHz	4.4	6.0(2)	
			f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 24 MHz	2.4	3.1(2)	
			f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

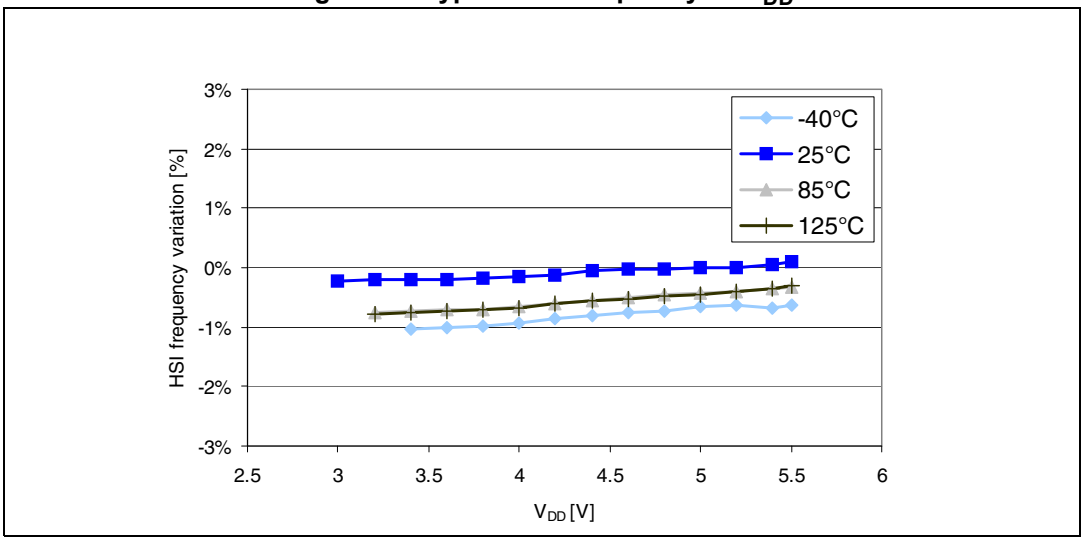
High-speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} = 3.0\ V \leq V_{DD} \leq 5.5\ V$, $-40\ °C \leq T_A \leq 150\ °C$	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 21. Typical HSI frequency vs V_{DD}



10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 °C to 150 °C.

Table 35. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 16 to 24 MHz with 1 ws f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 16 to 24 MHz with 1 ws f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	

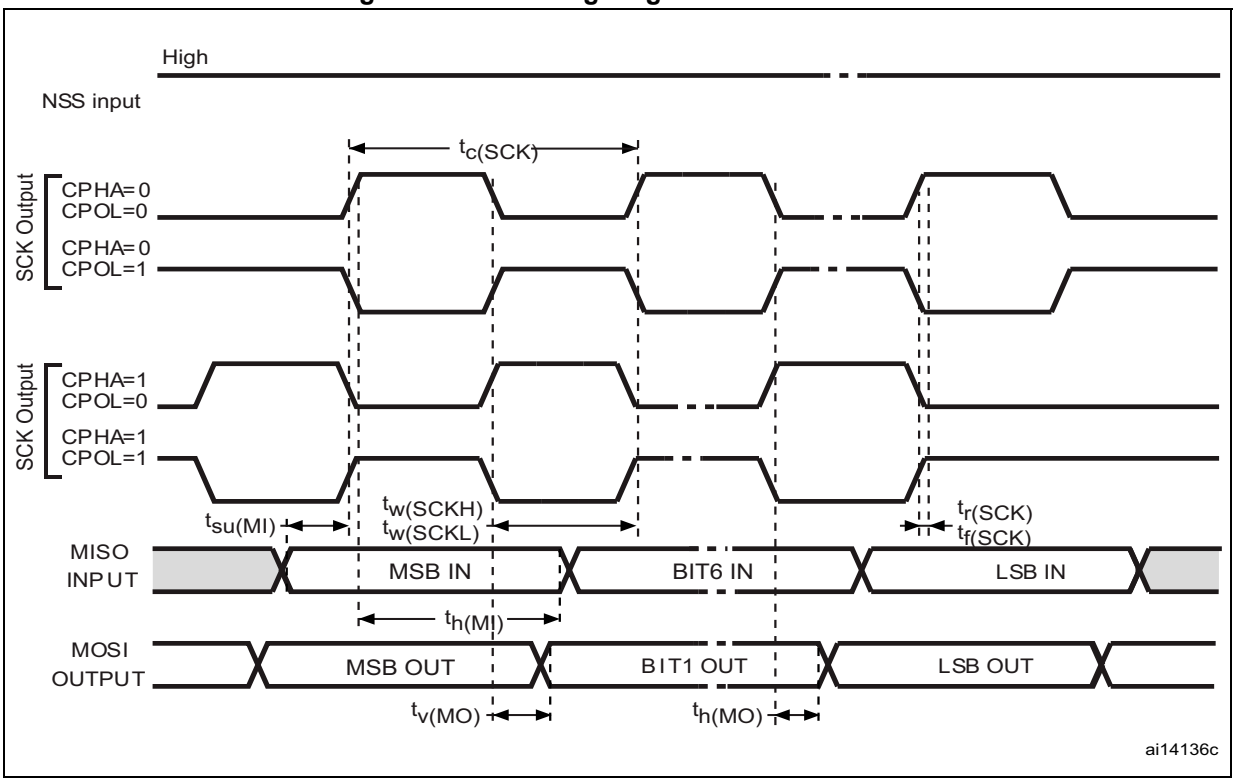
1. Guaranteed by characterization results, not tested in production.

Table 36. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Figure 42. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- ***ESD***: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- ***FTB***: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

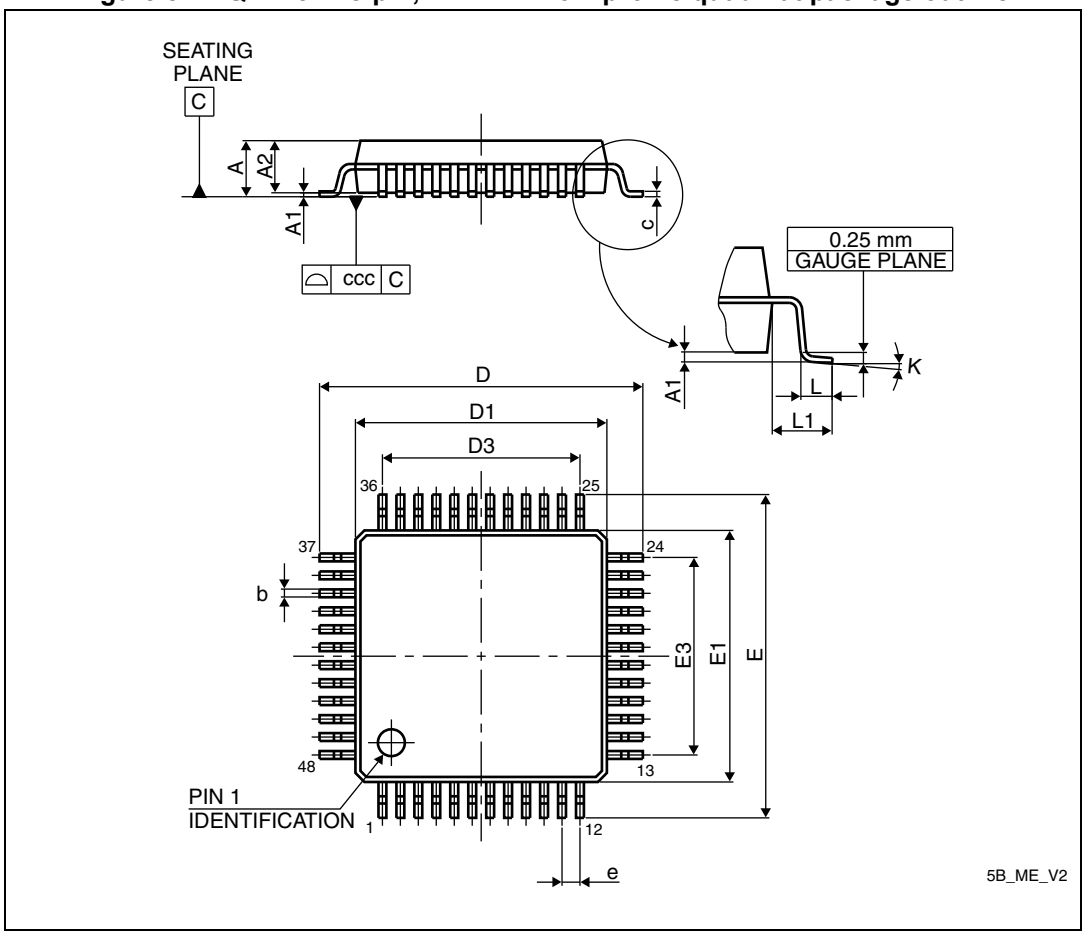
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A

11.3 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	Added 'H' products to the datasheet (Flash no EEPROM). *Section : Features* on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1. *Table 1: Device summary*: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166. *Section 1: Introduction*, *Section 5: Product overview*, *Section 9: Option bytes*, *Section 6.2: Alternate function remapping*, *Table 21: Current characteristics:* Updated reference documentation: RM0009, PM0047, and UM0470. *Section 2: Description*: added information about peak performance. *Section 3: Product line-up*: Removed *STM8A common features* table. *Table 4: Peripheral clock gating bits (CLK_PCKENR1):* Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T. *Table 5: Peripheral clock gating bits (CLK_PCKENR2)*: Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T. *Section 5: Product overview*: Made minor content changes and improved readability and layout. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: Major modification, TMU included. *Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI)*: User trimming updated. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: LSI as CPU clock added. *Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE)*, *Section 5.5.5: External clock input*: Maximum frequency conditional 32 Kbyte/128 Kbyte. *Section 5.8: Analog to digital converter (ADC)*: Scan for 128 Kbyte removed. *Section 5.9: Communication interfaces*, *Section 5.9.3: Serial peripheral interface (SPI)*: SPI 10 Mb/s. *Figure 3: LQFP 80-pin pinout*, *Figure 4: LQFP 64-pin pinout*, *Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout*: Amended footnote 1. *Table 12: Memory model 128K:* HS output changed from 20 mA to 8 mA. *Section 7: Memory and register map*: Corrected *Table 8: Register and memory map*; removed address list; added *Table 14: General hardware register map*. *Section 10.3.2: Supply current characteristics* Note on typical/WC values added.

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	Replaced the salestype 'STM8H61xx' with 'STM8AH61xx on the first page. Added 'part numbers' to heading rows of *Table 1: Device summary*. Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD. *Table 18*: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]' *Section 9*: Updated introductory text concerning option bytes which do not need to be saved in a complementary form. *Table 18*: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively. *Table 21*: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'. Updated 80-pin package information in line with POA 0062342-revD in *Figure 45* and *Table 53*.
01-Jul-2009	4	Added 'STM8AH61xx' and 'STM8AH51xx to document header. Updated *: Features on page 1* (memories, timers, operating temperature, ADC and I/Os). Updated *Table 1: Device summary* Updated Kbyte value of program memory in *Section: Introduction* Changed the first two lines from the top in *Section: Description*. Updated *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram* Updated *Section 5: Product overview* In *Figure 5: LQFP 48-pin pinout*, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively. *Section 6: Pinouts and pin description:* deleted the text below the *Table 10: Legend/abbreviation for the pin description table* *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description:* 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote. Updated *Figure 8: Register and memory map*. *Table 12: Memory model 128K:* updated footnote Deleted the *Table: Stack and RAM partitioning* *Table 17: STM8A interrupt table*: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote Updated *Section 7: Memory and register map* Updated *Table: Data memory, Table: I/O static characteristics,* and *Table 39: NRST pin characteristics*. *Section 10.1.1: Minimum and maximum values:* added ambient temperature T_A = -40 °C Updated *Table 20: Voltage characteristics*. Updated *Table 21: Current characteristics*. Updated *Table 22: Thermal characteristics*. Updated *Table 24: General operating conditions*.

Table 55. Document revision history (continued)

Date	Revision	Changes
01-Jul-2009	4 (continued)	Removed table*: Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 3.3 V.* Added *Table 28: Oscillator current consumption.* Added *Table 29: Programming current consumption.* Updated *Table 30: Typical peripheral current consumption VDD = 5.0 V* Updated *Table 31: HSE external clock characteristics.* Updated *Table 32: HSE oscillator characteristics.* *Table 20: HSE oscillator circuit diagram:* changed 'consumption control' to 'current control' *Section : HSE oscillator critical gm formula:* clarified formula Updated *Table 33: HSI oscillator characteristics.* Removed *'RAM and hardware registers'* Removed *Table: RAM and hardware registers.* Updated *Table 35: Flash program memory/data EEPROM memory* Added *Table 36: Flash program memory.* Added *Table 37: Data memory.* Updated *Table 38: I/O static characteristics.* Updated *Table 39: NRST pin characteristics.* Updated *Table 40: TIM 1, 2, 3, and 4 electrical specifications* *Section 10.3.9: SPI interface:* changed title from "SPI serial peripheral interface". Updated *Table 41: SPI characteristics.* *Figure 40: SPI timing diagram in slave mode and with CPHA = 0*: Changed title and added footnote. *Figure 41: SPI timing diagram in slave mode and with CPHA = 1:* changed the title. Updated *Table 43: ADC characteristics.* Updated *Figure 43: Typical application with ADC.* Removed *Table: ADC accuracy for VDDA = 3.3 V.* Updated *Table 44: ADC accuracy for VDDA = 5 V.* Updated *Table 46: EMI data.* Updated *Table 48: Electrical sensitivities.* Added text about Ecopack in the *Section 11: Package information.* *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline:* deleted footnote. Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added *Section 13: STM8 development tools.*
22-Oct-2009	5	Updated *Table 1: Device summary*: added STM8AF5178, STM8AF519A and STM8AF619A.