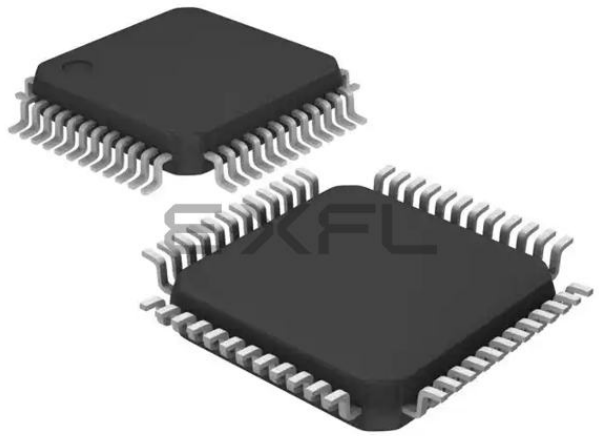

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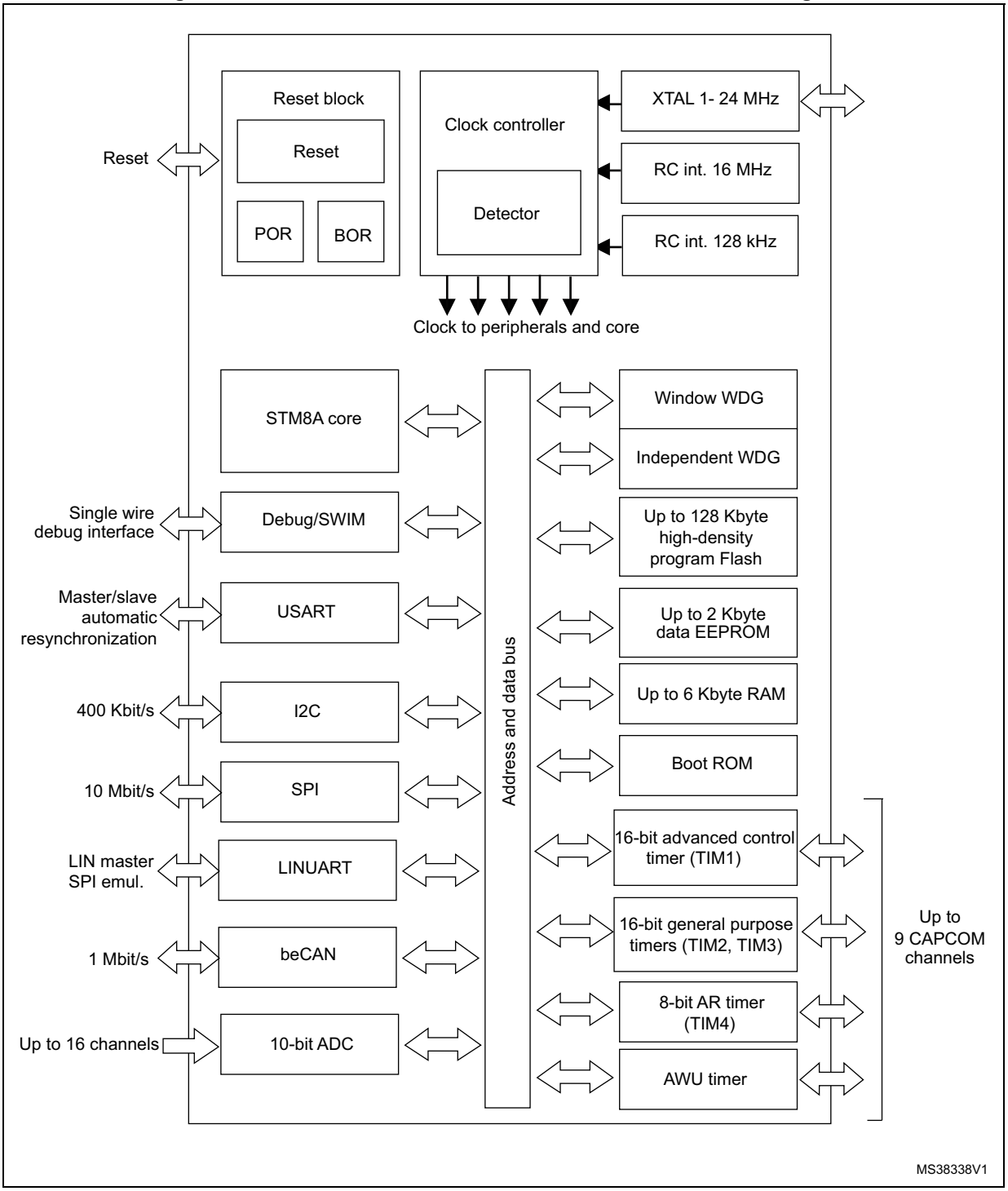
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a8tdx

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

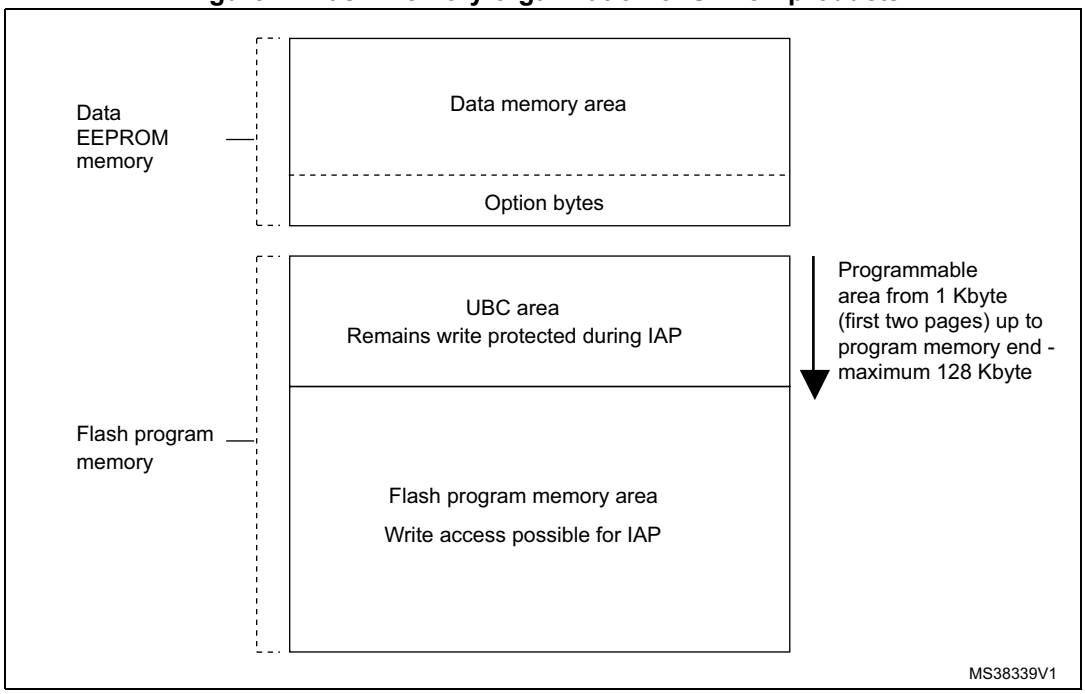
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 54*).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ for master, 8 Mbit/s or f_{MASTER} /2 for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

5.9.4 Inter integrated circuit (I^2C) interface

The devices covered by this datasheet contain one I^2C interface. The interface is available on all the supported packages.

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
  - Mask mode permitting ID range filtering
  - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	2	2	2	PA1/OSCIN(1)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/ crystal in	-
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	4	4	-	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	5	5	4	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	6	6	5	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	7	7	6	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	8	7	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	10	10	-	-	PA4/USART_RX	I/O	**X**	X	X	-	O3	X	X	**Port A4**	USART receive	-
11	11	11	-	-	PA5/USART_TX	I/O	**X**	X	X	-	O3	X	X	**Port A5**	USART transmit	-
12	12	12	-	8	PA6/USART_CK (2)	I/O	**X**	X	X	-	O3	X	X	**Port A6**	USART synchro nous clock	-
13	-	-	-	-	PH0	I/O	X	X	-	HS	O3	X	X	**Port H0**	-	-
14	-	-	-	-	PH1	I/O	**X**	X	-	HS	O3	X	X	**Port H1**	-	-
15	-	-	-	-	PH2	I/O	**X**	X	-	-	O1	X	X	**Port H2**	-	-
16	-	-	-	-	PH3	I/O	**X**	X	-	-	O1	X	X	**Port H3**	-	-
17	13	-	-	-	PF7/AIN15	I/O	**X**	X	-	-	O1	X	X	**Port F7**	Analog input 15	-
18	14	-	-	-	PF6/AIN14	I/O	**X**	X	-	-	O1	X	X	**Port F6**	Analog input 14	-
19	15	-	-	-	PF5/AIN13	I/O	**X**	X	-	-	O1	X	X	**Port F5**	Analog input 13	-
20	16	-	8	-	PF4/AIN12	I/O	**X**	X	-	-	O1	X	X	**Port F4**	Analog input 12	-
21	17	-	-	-	PF3/AIN11	I/O	**X**	X	-	-	O1	X	X	**Port F3**	Analog input 11	-

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART	UART1_SR	USART status register	0xC0
0x00 5231		UART1_DR	USART data register	0xXX
0x00 5232		UART1_BRR1	USART baud rate register 1	0x00
0x00 5233		UART1_BRR2	USART baud rate register 2	0x00
0x00 5234		UART1_CR1	USART control register 1	0x00
0x00 5235		UART1_CR2	USART control register 2	0x00
0x00 5236		UART1_CR3	USART control register 3	0x00
0x00 5237		UART1_CR4	USART control register 4	0x00
0x00 5238		UART1_CR5	USART control register 5	0x00
0x00 5239		UART1_GTR	USART guard time register	0x00
0x00 523A		UART1_PSCR	USART prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	LINUART	UART3_SR	LINUART status register	0xC0
0x00 5241		UART3_DR	LINUART data register	0xXX
0x00 5242		UART3_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART3_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART3_CR1	LINUART control register 1	0x00
0x00 5245		UART3_CR2	LINUART control register 2	0x00
0x00 5246		UART3_CR3	LINUART control register 3	0x00
0x00 5247		UART3_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 19. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0xFF: Pages 4 to 255 defined as UBC, memory write-protected *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. **AFR4: Alternate function remapping option 4** 0: Port D7 alternate function = TLI 1: Reserved **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

10.3 Operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	1 wait state T_A = -40 °C to 150 °C	16	24	MHz
		0 wait state T_A = -40 °C to 150 °C	0	16	
V_{DD}/V_{DDIO}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
T_A	Ambient temperature	Suffix A	- 40	85	°C
		Suffix C		125	
		Suffix D		150	
T_J	Junction temperature range	Suffix A	- 40	90	
		Suffix C		130	
		Suffix D		155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.

Figure 11. f_{CPUmax} versus V_{DD}

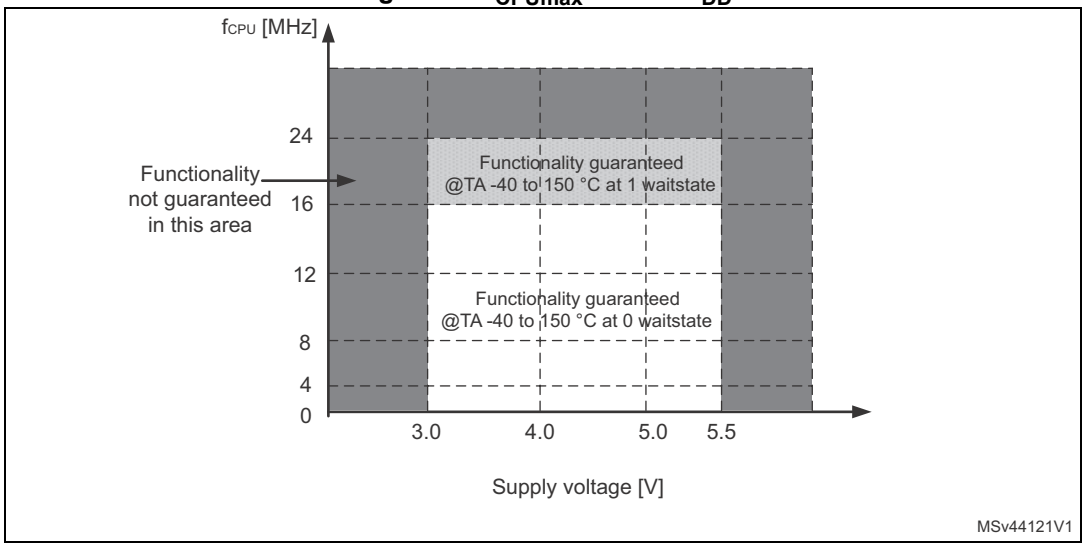


Table 25. Operating conditions at power-up/power-down

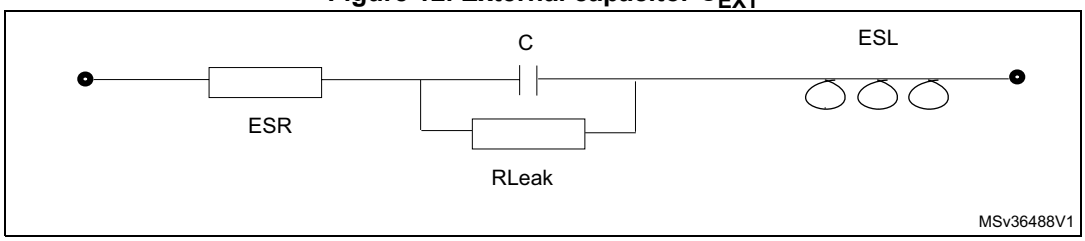
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	1.7	ms
	Reset generation delay	V_{DD} falling	-	3	-	µs
V_{IT+}	Power-on reset threshold(2) (3)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70(1)	-	mV

1. Guaranteed by design, not tested in production.
2. If V_{DD} is below 3 V, the code execution is guaranteed above the V_{IT-} and V_{IT+} thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1 µF requires Q=1 µF x 1.8 V = 1.8 µC.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 24*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 59* and *Figure 10 on page 60*.

If not explicitly stated, general conditions of temperature and voltage apply.

Table 29. Programming current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(PROG)}$	Programming current	V_{DD} = 5 V, -40 °C to 150 °C, erasing and programming data or Flash program memory	1.0	1.7	mA

Table 30. Typical peripheral current consumption V_{DD} = 5.0 V(1)

Symbol	Parameter	Typ. f_{master} = 2 MHz	Typ. f_{master} = 16 MHz	Typ. f_{master} =24 MHz	Unit
$I_{DD(TIM1)}$	TIM1 supply current(2)	0.03	0.23	0.34	mA
$I_{DD(TIM2)}$	TIM2 supply current (2)	0.02	0.12	0.19	
$I_{DD(TIM3)}$	TIM3 supply current(2)	0.01	0.1	0.16	
$I_{DD(TIM4)}$	TIM4 supply current(2)	0.004	0.03	0.05	
$I_{DD(USART)}$	USART supply current(2)	0.03	0.09	0.15	
$I_{DD(LINUART)}$	LINUART supply current(2)	0.03	0.11	0.18	
$I_{DD(SPI)}$	SPI supply current(2)	0.01	0.04	0.07	
$I_{DD(I^2C)}$	I^2C supply current(2)	0.02	0.06	0.91	
$I_{DD(CAN)}$	CAN supply current(3)	0.06	0.30	0.40	
$I_{DD(AWU)}$	AWU supply current(2)	0.003	0.02	0.05	
$I_{DD(TOT\_DIG)}$	All digital peripherals on	0.22	1	2.4	
$I_{DD(ADC)}$	ADC supply current when converting(4)	0.93	0.95	0.96	

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1 MHz. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 13 to *Figure 18* show typical current consumption measured with code executing in RAM.

Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @f_{CPU} = 16 MHz, peripherals = on

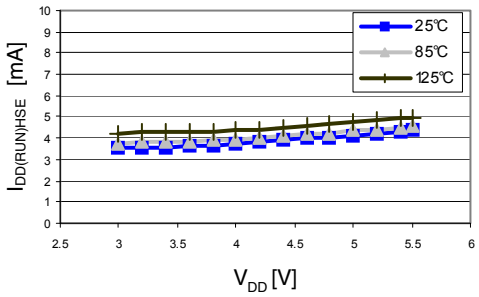


Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

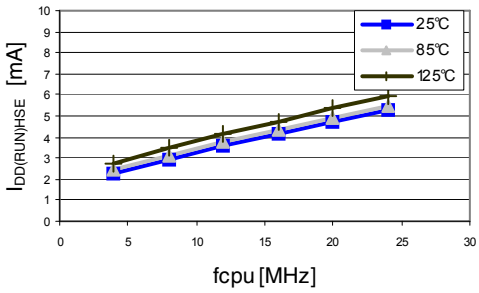


Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off

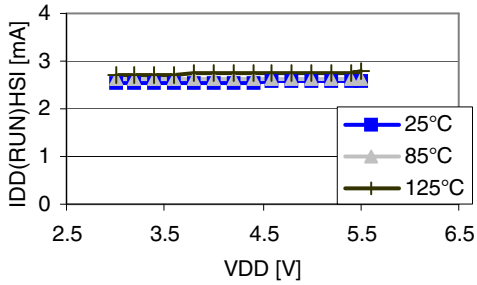


Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = on

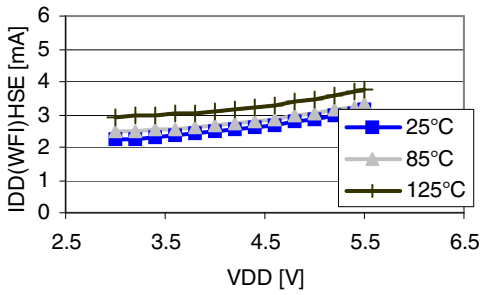


Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

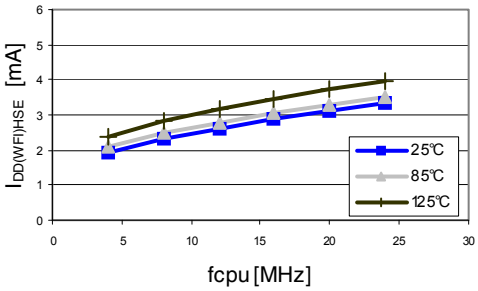
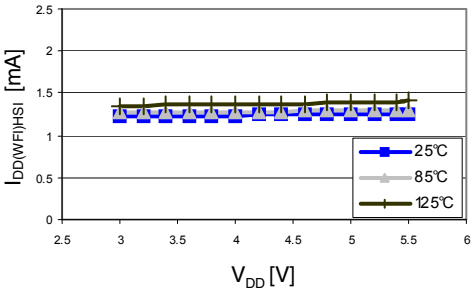


Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST high-level input voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST low-level output voltage(1)	I_{OL} = 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Figure 36. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

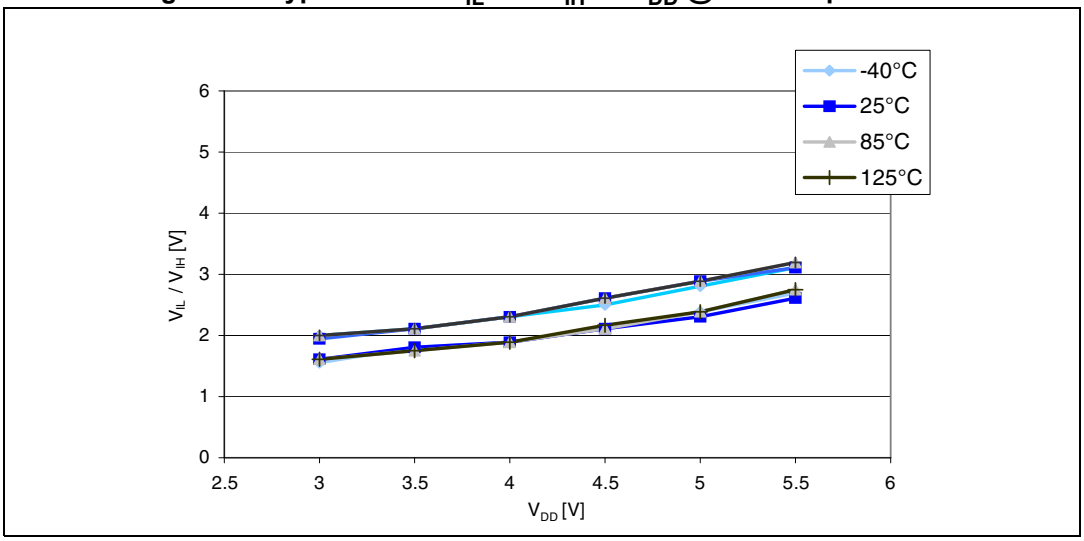
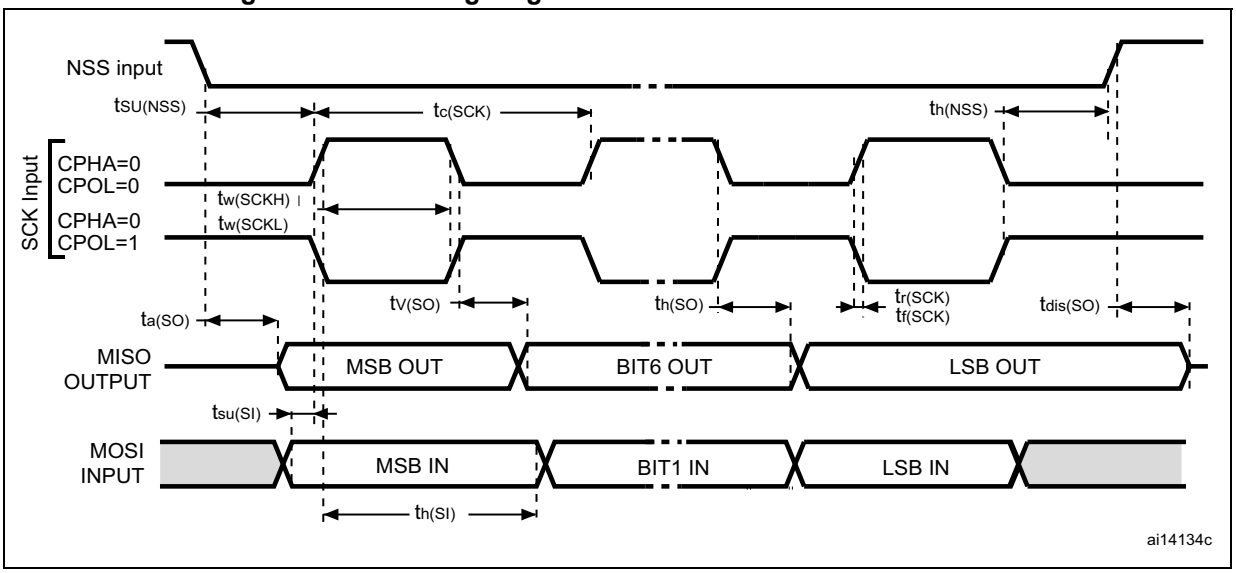
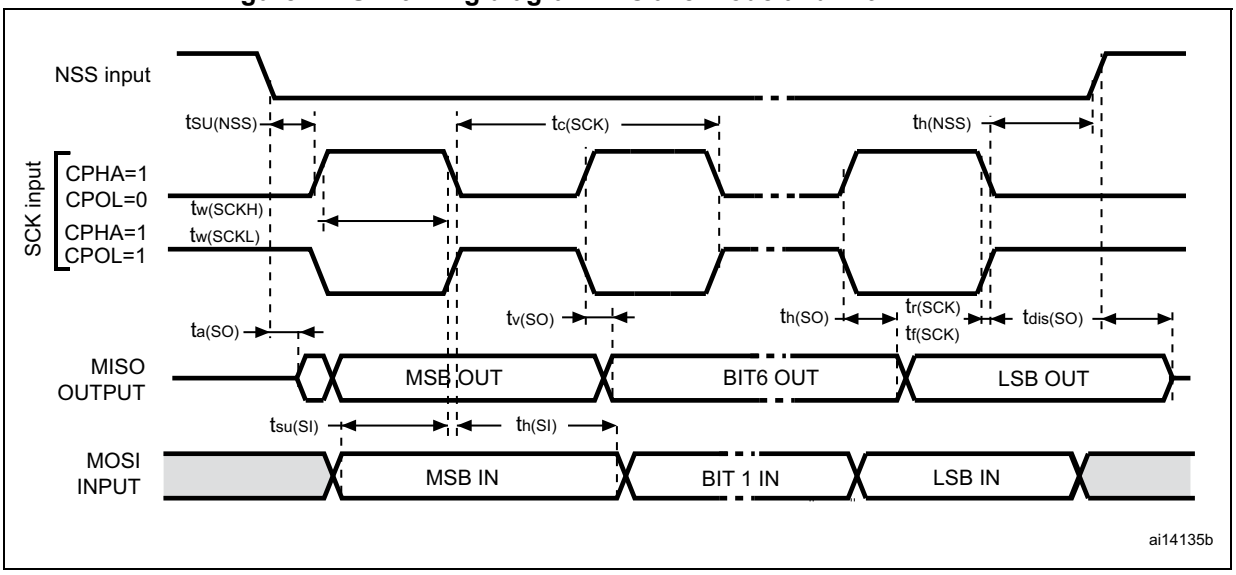


Figure 40. SPI timing diagram in slave mode and with CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



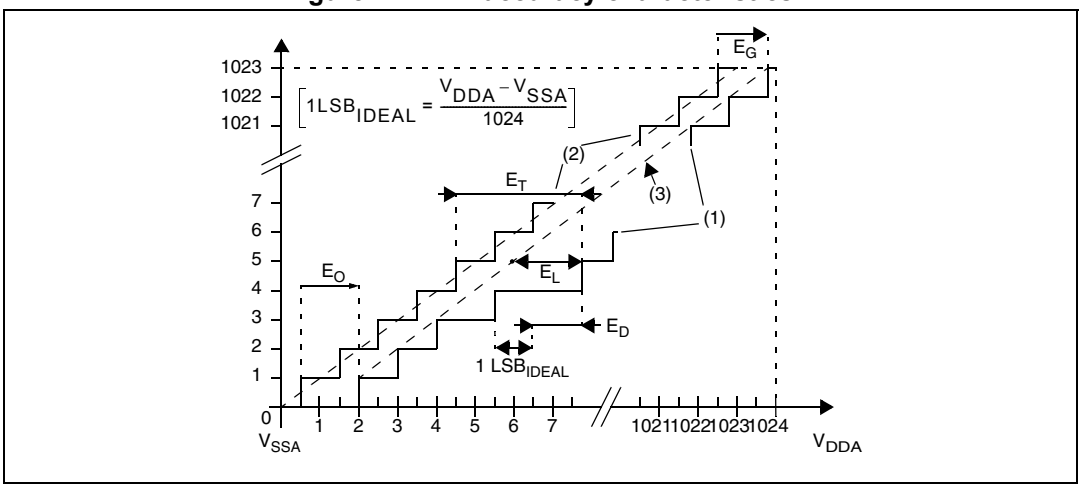
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 44. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

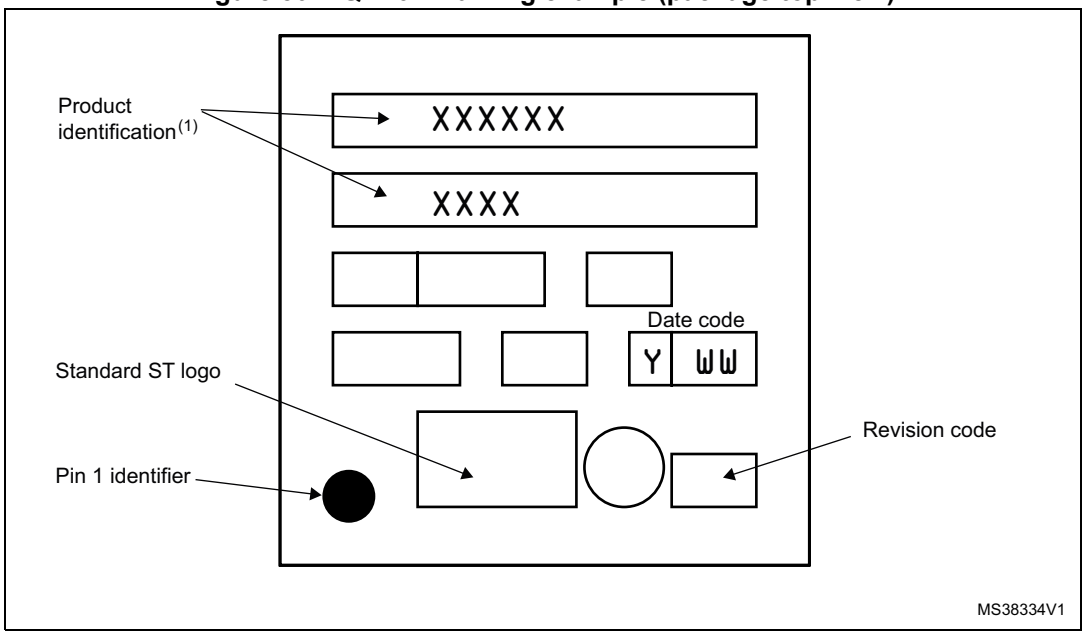
1. Guaranteed by characterization results, not tested in production

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP64 marking example (package top view)



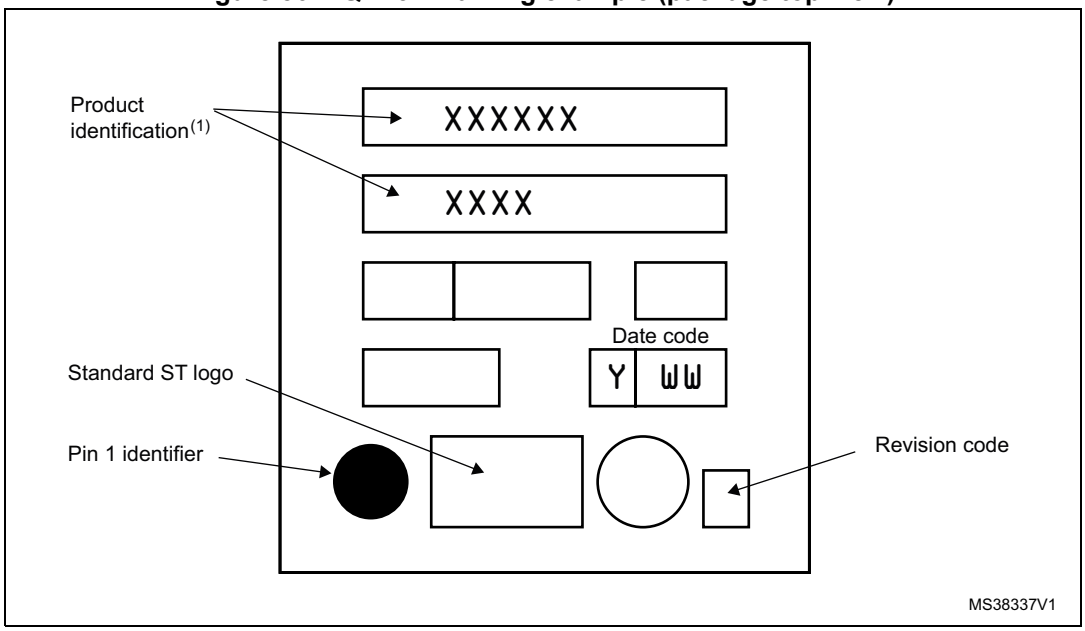
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 55. Document revision history (continued)

Date	Revision	Changes
01-Jul-2009	4 (continued)	Removed table*: Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 3.3 V.* Added *Table 28: Oscillator current consumption.* Added *Table 29: Programming current consumption.* Updated *Table 30: Typical peripheral current consumption VDD = 5.0 V* Updated *Table 31: HSE external clock characteristics.* Updated *Table 32: HSE oscillator characteristics.* *Table 20: HSE oscillator circuit diagram:* changed 'consumption control' to 'current control' *Section : HSE oscillator critical gm formula:* clarified formula Updated *Table 33: HSI oscillator characteristics.* Removed *'RAM and hardware registers'* Removed *Table: RAM and hardware registers.* Updated *Table 35: Flash program memory/data EEPROM memory* Added *Table 36: Flash program memory.* Added *Table 37: Data memory.* Updated *Table 38: I/O static characteristics.* Updated *Table 39: NRST pin characteristics.* Updated *Table 40: TIM 1, 2, 3, and 4 electrical specifications* *Section 10.3.9: SPI interface:* changed title from "SPI serial peripheral interface". Updated *Table 41: SPI characteristics.* *Figure 40: SPI timing diagram in slave mode and with CPHA = 0*: Changed title and added footnote. *Figure 41: SPI timing diagram in slave mode and with CPHA = 1:* changed the title. Updated *Table 43: ADC characteristics.* Updated *Figure 43: Typical application with ADC.* Removed *Table: ADC accuracy for VDDA = 3.3 V.* Updated *Table 44: ADC accuracy for VDDA = 5 V.* Updated *Table 46: EMI data.* Updated *Table 48: Electrical sensitivities.* Added text about Ecopack in the *Section 11: Package information.* *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline:* deleted footnote. Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added *Section 13: STM8 development tools.*
22-Oct-2009	5	Updated *Table 1: Device summary*: added STM8AF5178, STM8AF519A and STM8AF619A.