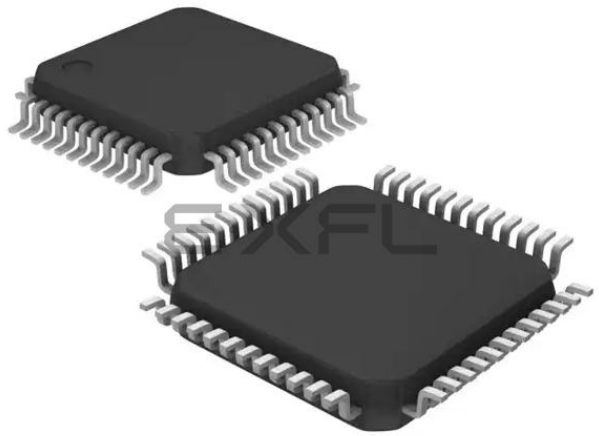

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a8tdy

Contents

2 Description

The STM8AF526x/8x/Ax and STM8AF6269/8x/Ax automotive 8-bit microcontrollers described in this datasheet offer from 32 Kbyte to 128 Kbyte of non volatile memory and integrated true data EEPROM. They are referred to as high density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

The STM8AF52 series features a CAN interface.

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, wtachdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map, and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5.5 V operating supply.

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
  - Mask mode permitting ID range filtering
  - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC positive reference voltage		-
23	19	13	9	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
24	20	14	10	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
25	21	-	-	-	V_{REF-}	S	-	-	-	-	-	-	-	ADC negative reference voltage		-
26	22	-	-	-	PF0/AIN10	I/O	**X**	X	-	-	O1	X	X	**Port F0**	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X	-	-	O1	X	X	**Port H4**	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X	-	-	O1	X	X	**Port H5**	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X	-	-	O1	X	X	**Port H6**	Timer 1 - inverted channel 2	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
55	46	-	-	-	PG3	I/O	**X**	X	-	-	O1	X	X	**Port G3**	-	-
56	47	-	-	-	PG4	I/O	**X**	X	-	-	O1	X	X	**Port G4**	-	-
57	48	-	-	-	PI0	I/O	**X**	X	-	-	O1	X	X	**Port I0**	-	-
58	-	-	-	-	PI1	I/O	**X**	X	-	-	O1	X	X	**Port I1**	-	-
59	-	-	-	-	PI2	I/O	**X**	X	-	-	O1	X	X	**Port I2**	-	-
60	-	-	-	-	PI3	I/O	**X**	X	-	-	O1	X	X	**Port I3**	-	-
61	-	-	-	-	PI4	I/O	**X**	X	-	-	O1	X	X	**Port I4**	-	-
62	-	-	-	-	PI5	I/O	**X**	X	-	-	O1	X	X	**Port I5**	-	-
63	49	-	-	-	PG5	I/O	**X**	X	-	-	O1	X	X	**Port G5**	-	-
64	50	-	-	-	PG6	I/O	**X**	X	-	-	O1	X	X	**Port G6**	-	-
65	51	-	-	-	PG7	I/O	**X**	X	-	-	O1	X	X	**Port G7**	-	-
66	52	-	-	-	PE4	I/O	**X**	X	X	-	O1	X	X	**Port E4**	-	-
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
68	54	38	-	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port E2**	I^2C data	-
69	55	39	-	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port E1**	I^2C clock	-
70	56	40	-	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
71	-	-	-	-	PI6	I/O	**X**	X	-	-	O1	X	X	**Port I6**	-	-
72	-	-	-	-	PI7	I/O	**X**	X	-	-	O1	X	X	**Port I7**	-	-
73	57	41	25	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
75	59	43	27	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	28	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART	UART1_SR	USART status register	0xC0
0x00 5231		UART1_DR	USART data register	0xXX
0x00 5232		UART1_BRR1	USART baud rate register 1	0x00
0x00 5233		UART1_BRR2	USART baud rate register 2	0x00
0x00 5234		UART1_CR1	USART control register 1	0x00
0x00 5235		UART1_CR2	USART control register 2	0x00
0x00 5236		UART1_CR3	USART control register 3	0x00
0x00 5237		UART1_CR4	USART control register 4	0x00
0x00 5238		UART1_CR5	USART control register 5	0x00
0x00 5239		UART1_GTR	USART guard time register	0x00
0x00 523A		UART1_PSCR	USART prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	LINUART	UART3_SR	LINUART status register	0xC0
0x00 5241		UART3_DR	LINUART data register	0xXX
0x00 5242		UART3_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART3_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART3_CR1	LINUART control register 1	0x00
0x00 5245		UART3_CR2	LINUART control register 2	0x00
0x00 5246		UART3_CR3	LINUART control register 3	0x00
0x00 5247		UART3_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5437	beCAN	CAN_PF	CAN paged register F	0xXX(3)
0x00 5438 to 0x00 57FF	Reserved area (968 bytes)			

1. Depends on the previous reset source.
2. Write only register.
3. If the bootloader is enabled, it is initialized to 0x00.

Table 15. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17(2)
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00

Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

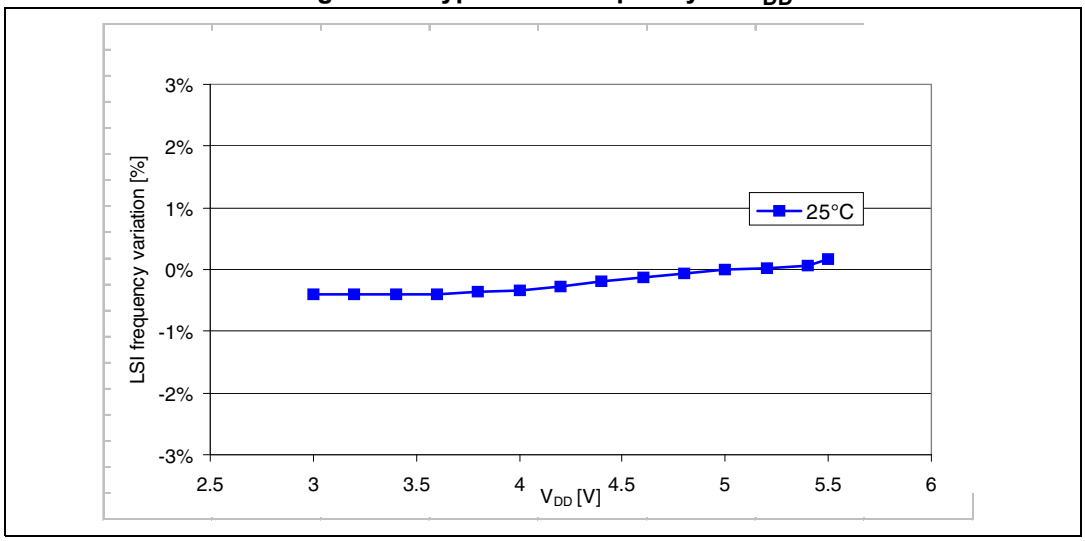


Table 37. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

2. Guaranteed by design.
3. Guaranteed by characterization results, not tested in production.

Figure 23. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

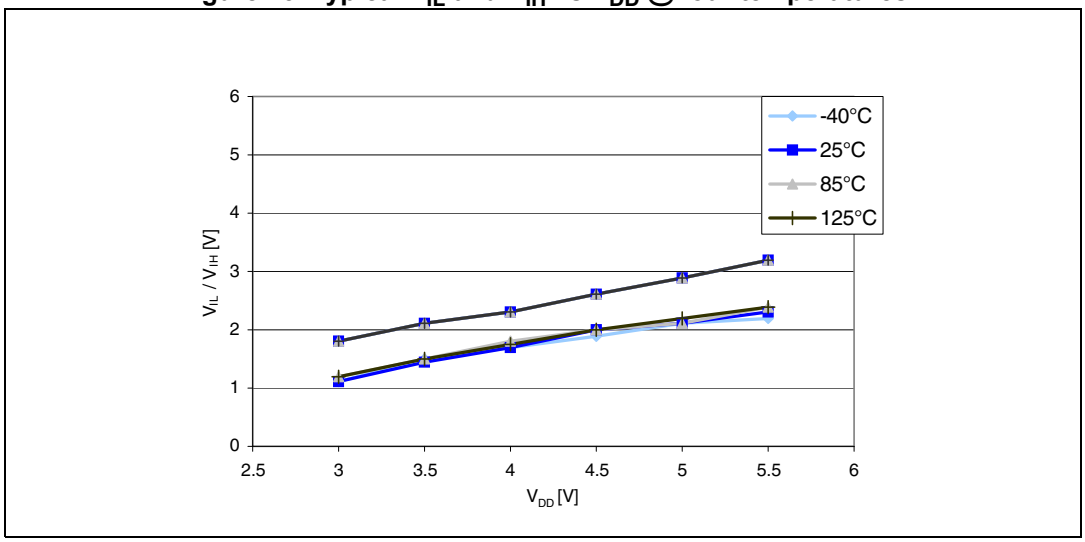


Figure 24. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures

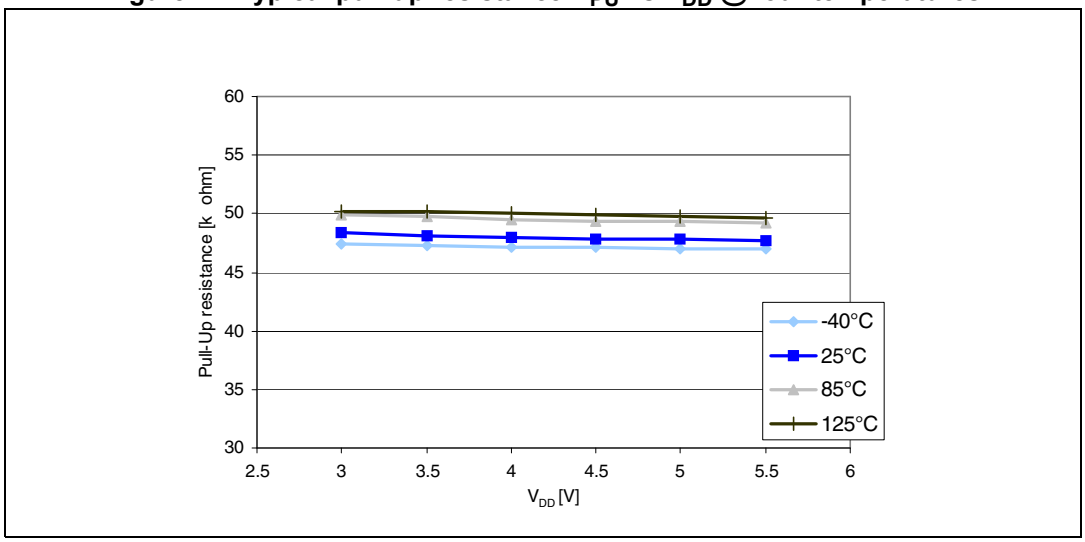
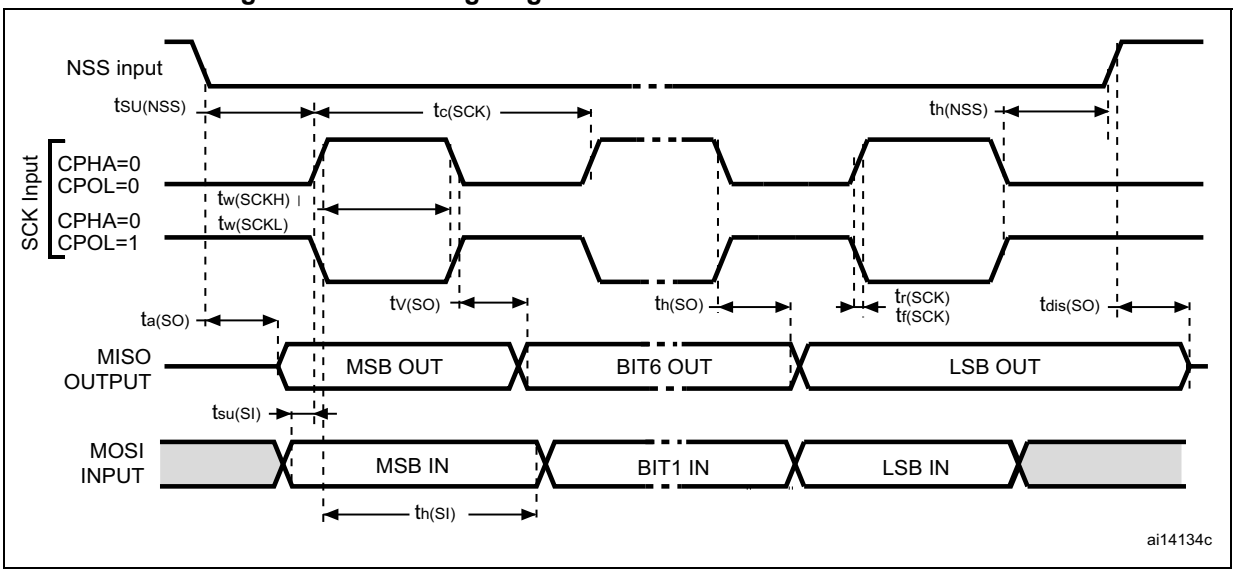
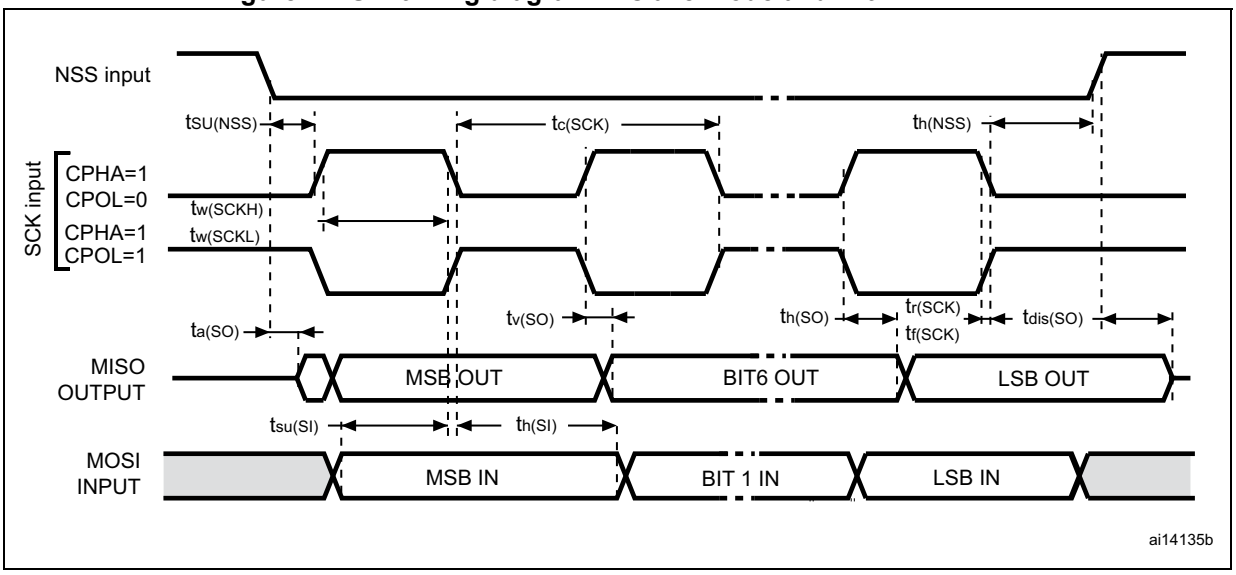


Figure 40. SPI timing diagram in slave mode and with CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- ***ESD***: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- ***FTB***: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

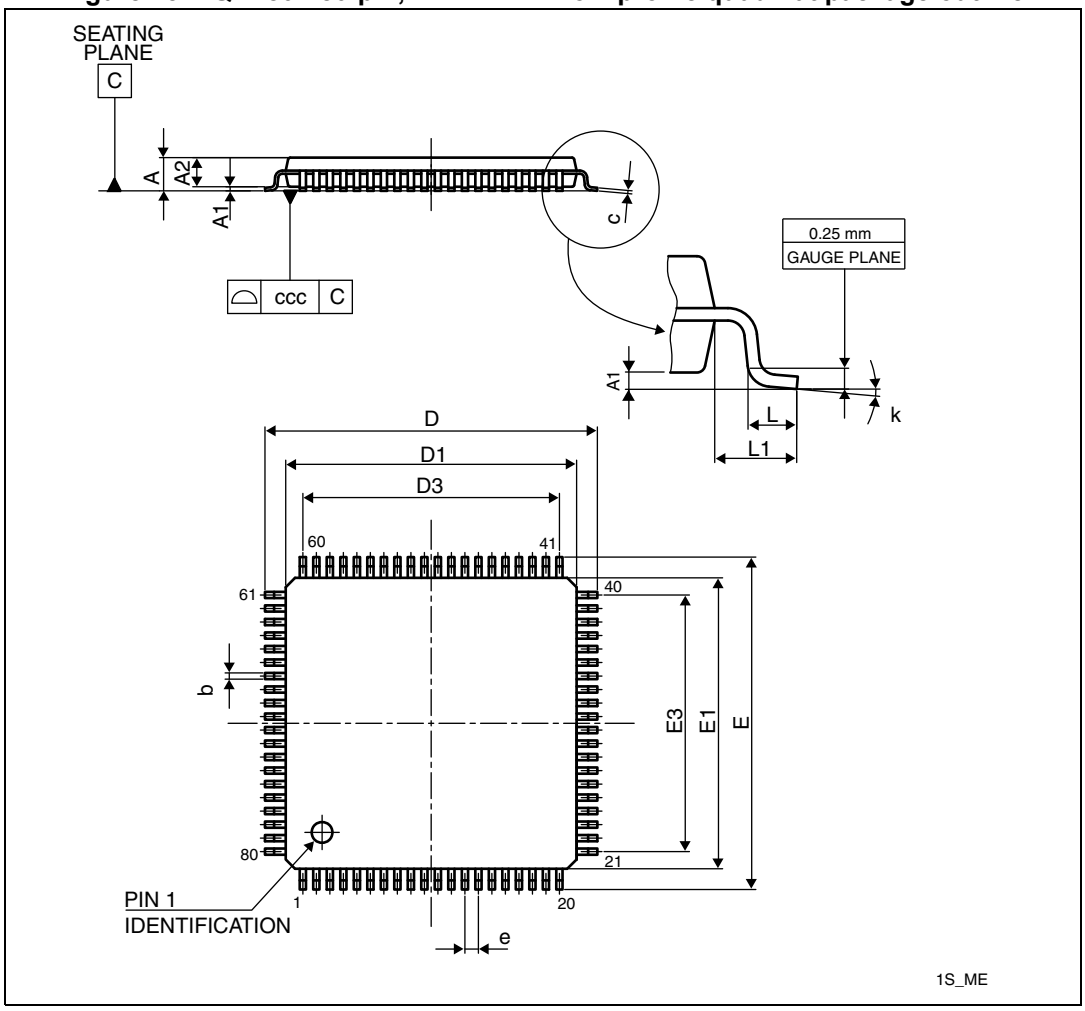
Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

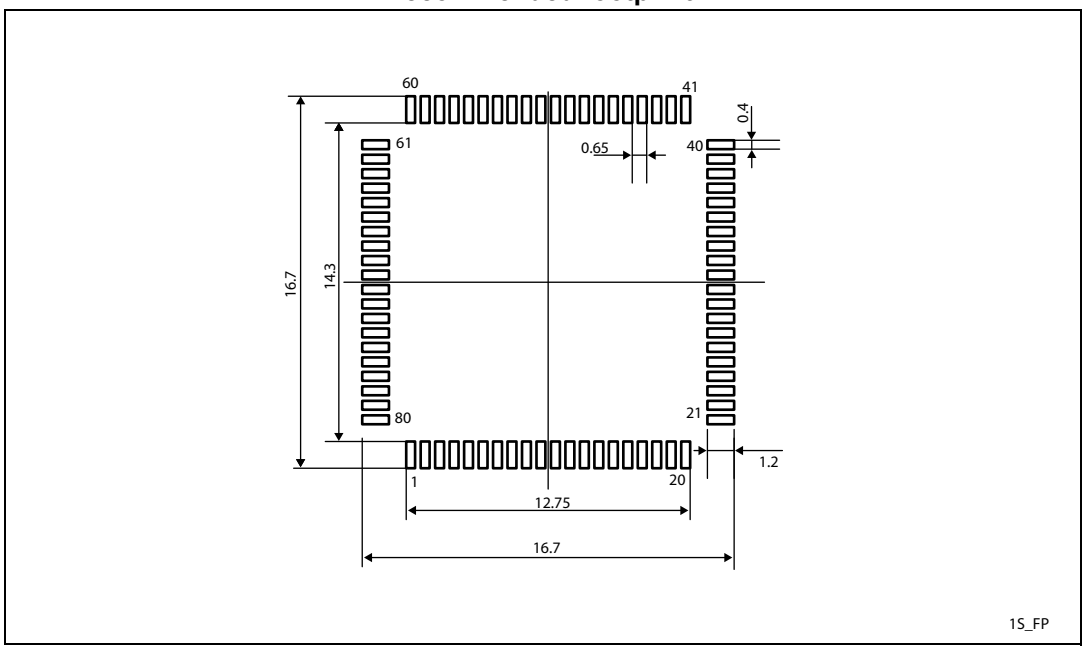
11.1 LQFP80 package information

Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



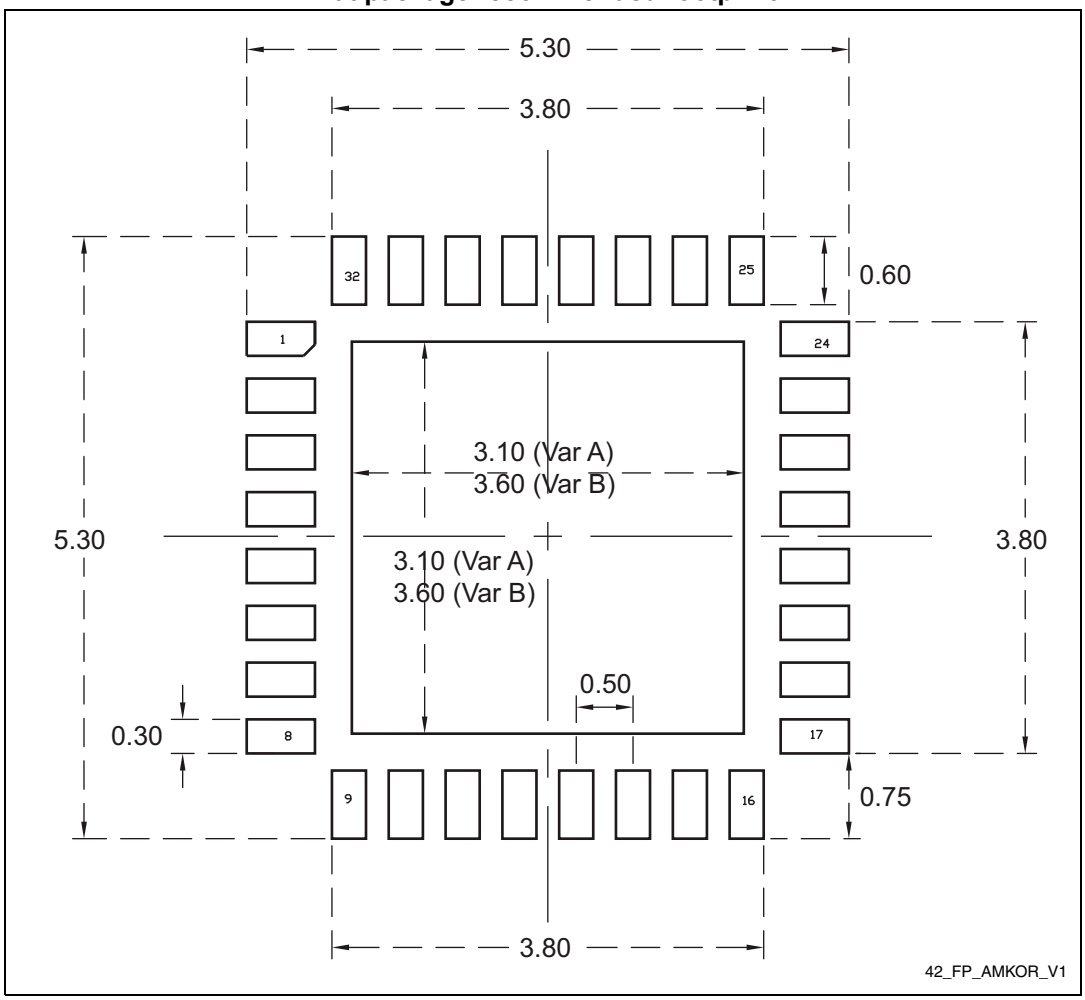
1. Dimensions are expressed in millimeters.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Oct-2016	14	Updated: – Title of *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout*, (previously STM8AF5286UC VFQFPN32 32-pin pinout) – Footnotes of *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1* – *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* replaced “STM8AF5286UC VQFPN32” with “STM8AF52x6 VQFPN32” at header row – *Section 10.2: Absolute maximum ratings* – *Section : Device marking on page 93* – *Section : Device marking on page 96* – *Section : Device marking on page 99* – *Section : Device marking on page 104* – *Section : Device marking on page 108* Added: – Footnote on *Figure 47: LQFP80 marking example (package top view)*, *Figure 50: LQFP64 marking example (package top view)*, *Figure 56: LQFP32 marking example (package top view)*, *Figure 59: VFQFPN32 marking example (package top view)*.
10-Nov-2016	15	Updated header row and PA6/USART_CK pin row on *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*.