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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a9tcy

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1 Introduction

This datasheet refers to the STM8AF526x/8x/Ax and STM8AF6269/8x/Ax products with 32 to 128 Kbyte of program memory.

In the order code, the letter 'F' refers to product versions with Flash and data EEPROM and 'P' to product versions with FASTROM. The identifiers 'F' and 'P' do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S and STM8A Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I ² C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	128 K	1 K						10
STM8AF/P5289	64 K							
STM8AF/P5269	LQFP64 (10x10)	32 K						
STM8AF/P52A8		128 K		2 K	6			1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)
STM8AF/P5288		64 K						
STM8AF/P5268	32 K							
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I ² C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I ² C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	128 K	2 K						10
STM8AF/P6289	64 K							
STM8AF/P6269	LQFP64 (10x10)	32 K						
STM8AF/P62A8		128 K		2 K	7			1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)
STM8AF/P6288		64 K						
STM8AF/P6286	LQFP32 (7x7)							
STM8AF/P62A6	VFQFPN32 (5x5)	128 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I ² C	25/24
STM8AF/P6286	LQFP32 (7x7)	64 K						

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

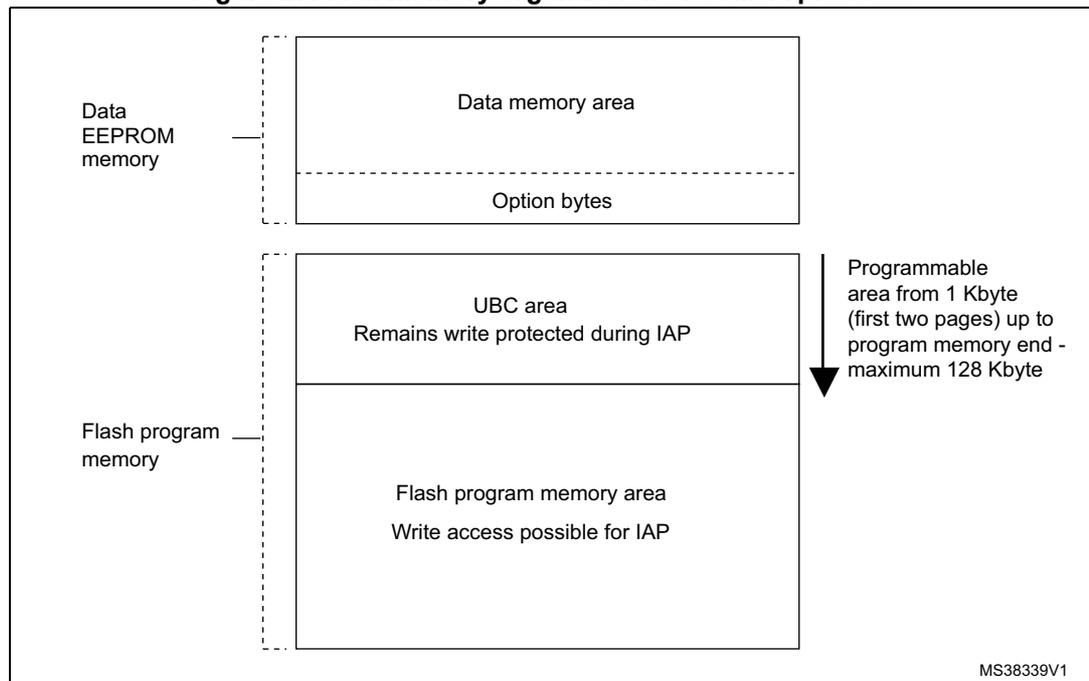
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see [Section 9: Option bytes on page 54](#)).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
 - 16 MHz high-speed internal RC oscillator (HSI)
 - 128 kHz low-speed internal RC (LSI)
 - 1-24 MHz high-speed external crystal (HSE)
 - Up to 24 MHz high-speed user-external clock (HSE user-ext)
- **Reset:** After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching:** Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wakeup:** In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS):** The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO):** This feature permits to output a clock signal for use by the application.

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with two trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

Table 6. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

TIM1 - advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1...32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.5 Basic timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

Table 7. TIM4

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM4	8-bit	Up	2^n n = 0 to 7	0	None	No	No	No	No

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update



5.9.2 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

LIN mode

Master mode

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

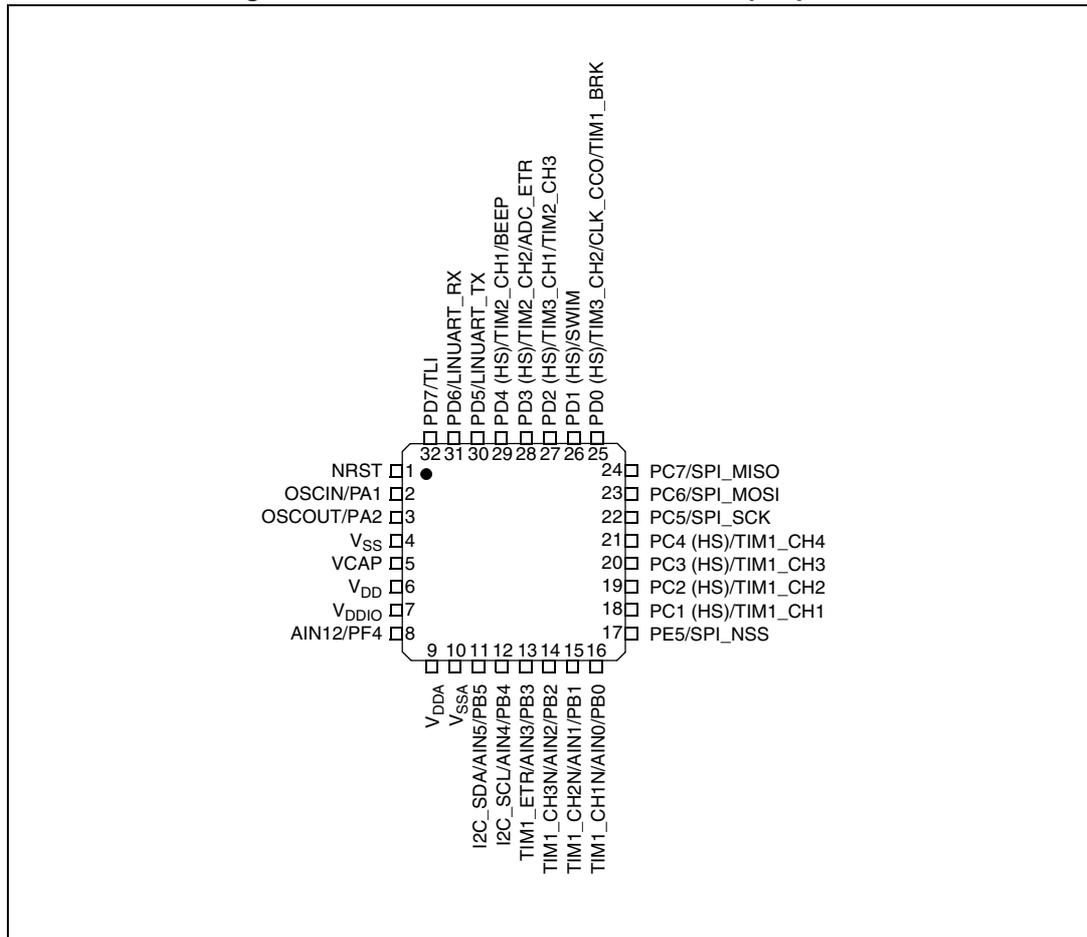
Slave mode

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
 - Delimiter too short
 - Synch field error
 - Deviation error (if automatic resynchronization is enabled)
 - Framing error in synch field or identifier field
 - Header time-out

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
 - A common programmable transmit and receive baud rates up to $f_{\text{MASTER}}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout

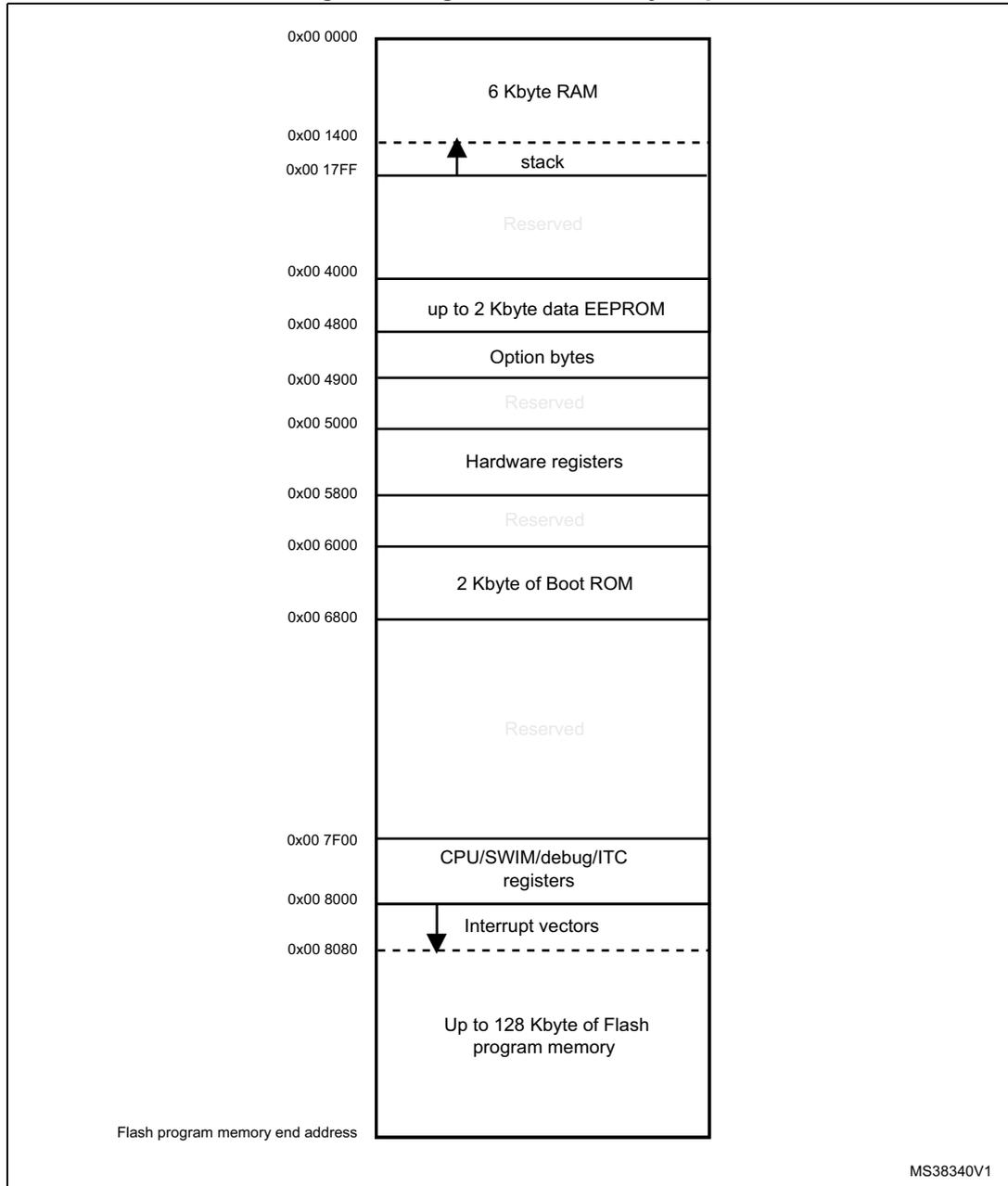


1. HS stands for high sink capability.

7 Memory and register map

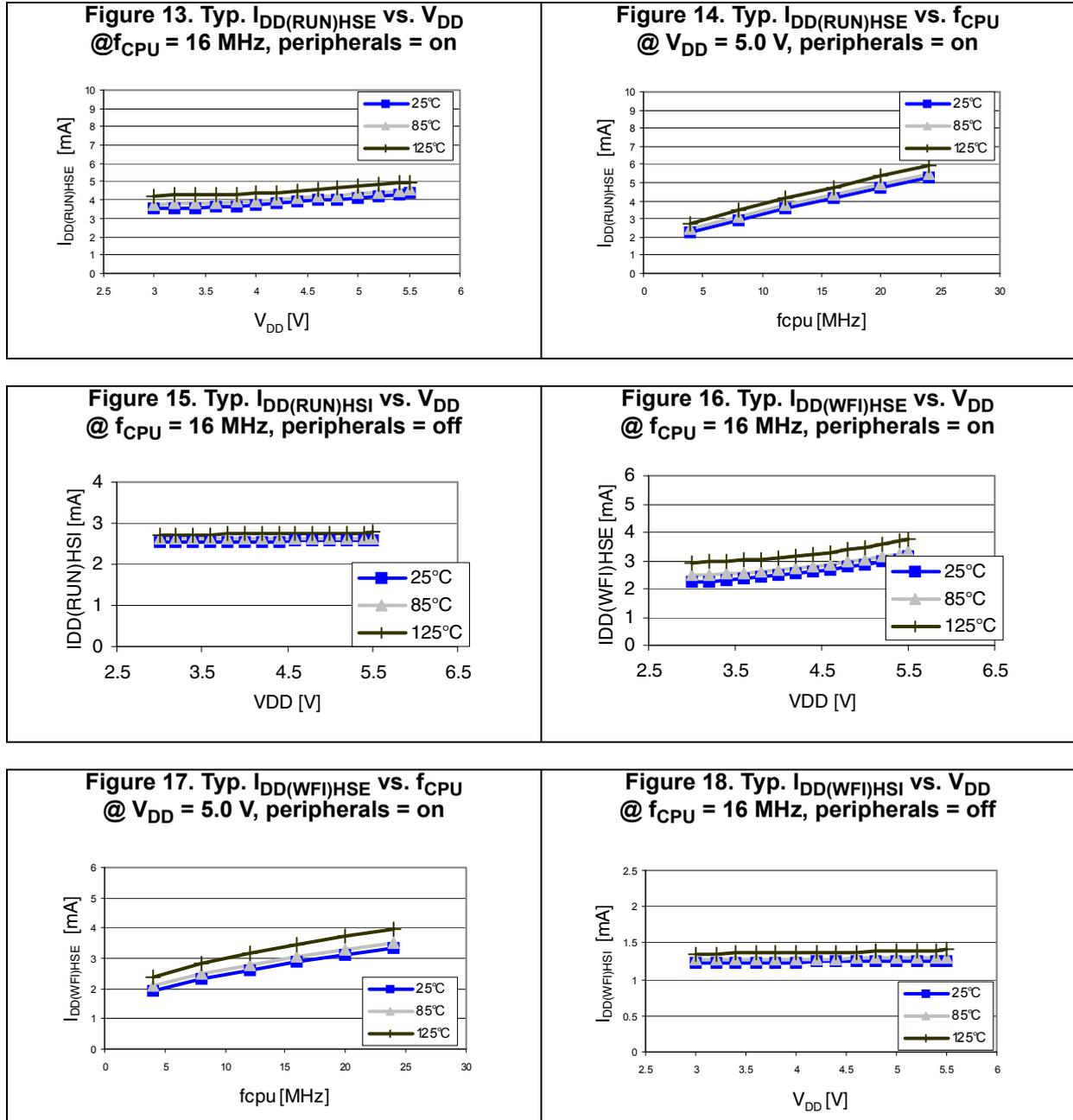
7.1 Memory map

Figure 8. Register and memory map



Current consumption curves

Figure 13 to Figure 18 show typical current consumption measured with code executing in RAM.



10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-4	4/A

Table 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data⁽¹⁾

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 53. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see [Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme 1 on page 111](#)).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax} = 82\text{ °C}$ (measured according to JESD51-2)
- $I_{DDmax} = 8\text{ mA}$
- $V_{DD} = 5\text{ V}$
- maximum 20 I/Os used at the same time in output at low-level with $I_{OL} = 8\text{ mA}$
- $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 8\text{ mA} \times 5\text{ V} = 400\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:

$$P_{INTmax} = 400\text{ mW} \text{ and } P_{IOmax} = 64\text{ mW}$$

$$P_{Dmax} = 400\text{ mW} + 64\text{ mW}$$

Thus:

$$P_{Dmax} = 464\text{ mW}.$$

Using the values obtained in [Table 54: Thermal characteristics](#) T_{Jmax} is calculated as follows:

For LQFP64 46 °C/W

$$T_{Jmax} = 82\text{ °C} + (46\text{ °C/W} \times 464\text{ mW}) = 82\text{ °C} + 21\text{ °C} = 103\text{ °C}$$

This is within the range of the suffix C version parts ($-40\text{ °C} < T_j < 125\text{ °C}$).

Parts must be ordered at least with the temperature range suffix C.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	<p>Added 'H' products to the datasheet (Flash no EEPROM).</p> <p>Section : Features on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1.</p> <p>Table 1: Device summary: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166.</p> <p>Section 1: Introduction, Section 5: Product overview, Section 9: Option bytes, Section 6.2: Alternate function remapping, Table 21: Current characteristics: Updated reference documentation: RM0009, PM0047, and UM0470.</p> <p>Section 2: Description: added information about peak performance.</p> <p>Section 3: Product line-up: Removed <i>STM8A common features</i> table.</p> <p>Table 4: Peripheral clock gating bits (CLK_PCKENR1): Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T.</p> <p>Table 5: Peripheral clock gating bits (CLK_PCKENR2): Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T.</p> <p>Section 5: Product overview: Made minor content changes and improved readability and layout.</p> <p>Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI): Major modification, TMU included.</p> <p>Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI): User trimming updated.</p> <p>Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI): LSI as CPU clock added.</p> <p>Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE), Section 5.5.5: External clock input: Maximum frequency conditional 32 Kbyte/128 Kbyte.</p> <p>Section 5.8: Analog to digital converter (ADC): Scan for 128 Kbyte removed.</p> <p>Section 5.9: Communication interfaces, Section 5.9.3: Serial peripheral interface (SPI): SPI 10 Mb/s.</p> <p>Figure 3: LQFP 80-pin pinout, Figure 4: LQFP 64-pin pinout, Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout: Amended footnote 1.</p> <p>Table 12: Memory model 128K: HS output changed from 20 mA to 8 mA.</p> <p>Section 7: Memory and register map: Corrected Table 8: Register and memory map; removed address list; added Table 14: General hardware register map.</p> <p>Section 10.3.2: Supply current characteristics Note on typical/WC values added.</p>

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	<p>Replaced the salestype 'STM8H61xx' with 'STM8AH61xx' on the first page.</p> <p>Added 'part numbers' to heading rows of Table 1: Device summary.</p> <p>Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD.</p> <p>Table 18: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]'</p> <p>Section 9: Updated introductory text concerning option bytes which do not need to be saved in a complementary form.</p> <p>Table 18: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively.</p> <p>Table 21: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'.</p> <p>Updated 80-pin package information in line with POA 0062342-revD in Figure 45 and Table 53.</p>
01-Jul-2009	4	<p>Added 'STM8AH61xx' and 'STM8AH51xx' to document header.</p> <p>Updated : Features on page 1 (memories, timers, operating temperature, ADC and I/Os).</p> <p>Updated Table 1: Device summary</p> <p>Updated Kbyte value of program memory in Section: Introduction</p> <p>Changed the first two lines from the top in Section: Description.</p> <p>Updated Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram</p> <p>Updated Section 5: Product overview</p> <p>In Figure 5: LQFP 48-pin pinout, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively.</p> <p>Section 6: Pinouts and pin description: deleted the text below the Table 10: Legend/abbreviation for the pin description table</p> <p>Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description: 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote.</p> <p>Updated Figure 8: Register and memory map.</p> <p>Table 12: Memory model 128K: updated footnote</p> <p>Deleted the Table: Stack and RAM partitioning</p> <p>Table 17: STM8A interrupt table: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote</p> <p>Updated Section 7: Memory and register map</p> <p>Updated Table: Data memory, Table: I/O static characteristics, and Table 39: NRST pin characteristics.</p> <p>Section 10.1.1: Minimum and maximum values: added ambient temperature $T_A = -40\text{ }^{\circ}\text{C}$</p> <p>Updated Table 20: Voltage characteristics.</p> <p>Updated Table 21: Current characteristics.</p> <p>Updated Table 22: Thermal characteristics.</p> <p>Updated Table 24: General operating conditions.</p>

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Apr-2010	6	<p>Updated title on cover page.</p> <p>Modified cover page header to clarify the part numbers covered by the datasheets. Updated footnote on Table 1: Device summary to add 'P' order codes.</p> <p>Changed definition of 'P' order codes.</p> <p>'Q' order codes (FASTROM and EEPROM) removed.</p> <p>Reorganized the content of Section 5: Product overview.</p> <p>Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description updated PD7/TLI alternate function, removed caution note for PD6/ LINUART_RX, and added note to PA1/OSCIN.</p> <p>Renamed Section 7: Memory and register map, and merged content with Section: Register map. Updated Figure 8: Register and memory map.</p> <p>Renamed BL_EN and NBL_EN, BL and NBL, respectively, in Table 18: Option bytes.</p> <p>Updated AFR4 definition in Table 19: Option byte description.</p> <p>Added C_{EXT} in Table 24: General operating conditions, and Section 10.3.1: VCAP external capacitor.</p> <p>Updated t_{VDD} in Table 25: Operating conditions at power-up/power-down.</p> <p>Moved Table 30: Typical peripheral current consumption VDD = 5.0 V to Section : Current consumption for on-chip peripherals.</p> <p>Removed V_{ESD(MM)} from Table 47: ESD absolute maximum ratings.</p> <p>Updated Section 12: Ordering information to the devices supported by the datasheet.</p> <p>Updated Section 13: STM8 development tools.</p>
08-Jul-2010	7	<p>Added STM8AF5168 and STM8AF518A part number in Figure 4, and STM8AF618A in Figure 5. Added STM8AF52xx, STM8AF6269, STM8AF628x, and STM8AF62Ax.</p> <p>Updated D temperature range to -40 to 150°C.</p> <p>Updated number of I/Os on cover page.</p> <p>Added Table 23: Operating lifetime.</p> <p>Restored V_{ESD(MM)} from Table 47: ESD absolute maximum ratings.</p> <p>Table 24: General operating conditions: updated V_{CAP} information. ESL parameter, and range D maximum junction temperature (T_J).</p> <p>Added STM8AF52xx and STM8AF62xx, and footnote in Section 12: Ordering information.</p> <p>Updated Section 13: STM8 development tools: added Table: Product evolution summary, and split the beCAN time triggered communication mode limitation in two sections.</p>