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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | STM8A |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 150°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af52a9tdy |

1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

## 5.7 Timers

### 5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

#### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

#### Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

### 5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

### 5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

### 5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

## 5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see *Table 8*).

**Table 8. ADC naming**

| Peripheral name in datasheet | Peripheral name in reference manual (RM0016) |
|---|---|
| ADC | ADC2 |

### ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: $f_{MASTER}$ divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

## 5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 9*).

**Table 9. Communication peripheral naming correspondence**

| Peripheral name in datasheet | Peripheral name in reference manual (RM0016) |
|---|---|
| USART | UART1 |
| LINUART | UART3 |

### 5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

### 5.9.2 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

#### LIN mode

**Master mode**

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

**Slave mode**

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

#### UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

## 5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain ($I^2C$ interface)

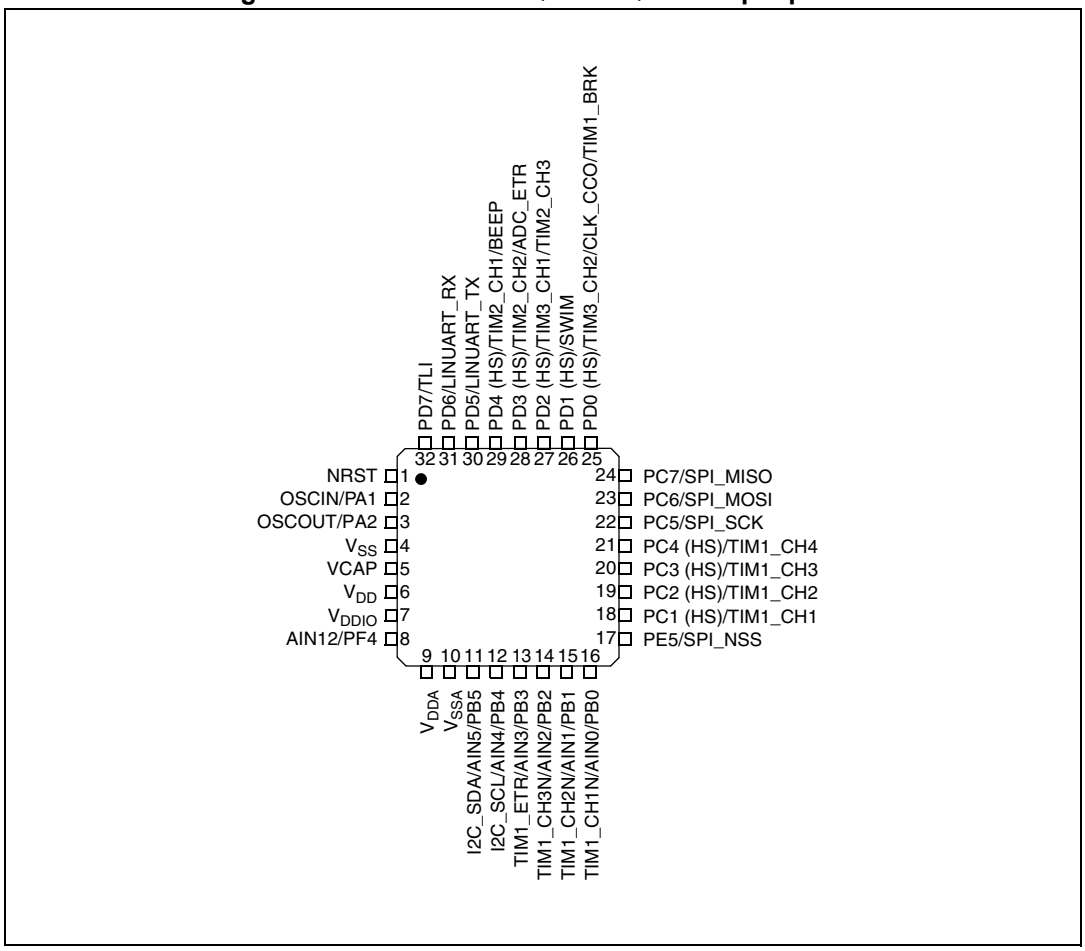
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

**Caution:** In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

**Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout**




1. HS stands for high sink capability.

**Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)**

| Pin number | | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | STM8AF52x6 VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 78 | 62 | 46 | 30 | 30 | PD5/ LINUART_TX | I/O | **X** | X | X | - | O1 | X | X | **Port D5** | LINUART data transmit | - |
| 79 | 63 | 47 | 31 | 31 | PD6/ LINUART_RX | I/O | **X** | X | X | - | O1 | X | X | **Port D6** | LINUART data receive | - |
| 80 | 64 | 48 | 32 | 32 | PD7/TLI(5) | I/O | **X** | X | X | - | O1 | X | X | **Port D7** | Top level interrupt | - |

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. SPI and USTART are not available in STM8AF5286UC, refer to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* for the pin names.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to $V_{DD}$ are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after reset release.
5. If this pin is configured as interrupt pin, it will trigger the TLI.

**Table 14. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x40 |
| 0x00 5060 to 0x005061 | Reserved area (2 bytes) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 bytes) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 bytes) | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX(1) |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 bytes) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |

**Table 15. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 bytes) | | | |
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | DM debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | Reserved area (5 bytes) | | | |

1. Accessible by debug module only
2. Product dependent value, see *Figure 8: Register and memory map*.

**Table 16. Temporary memory unprotection registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5800 | TMU | TMU_K1 | Temporary memory unprotection key register 1 | 0x00 |
| 0x00 5801 | | TMU_K2 | Temporary memory unprotection key register 2 | 0x00 |
| 0x00 5802 | | TMU_K3 | Temporary memory unprotection key register 3 | 0x00 |
| 0x00 5803 | | TMU_K4 | Temporary memory unprotection key register 4 | 0x00 |
| 0x00 5804 | | TMU_K5 | Temporary memory unprotection key register 5 | 0x00 |
| 0x00 5805 | | TMU_K6 | Temporary memory unprotection key register 6 | 0x00 |
| 0x00 5806 | | TMU_K7 | Temporary memory unprotection key register 7 | 0x00 |
| 0x00 5807 | | TMU_K8 | Temporary memory unprotection key register 8 | 0x00 |
| 0x00 5808 | | TMU_CSR | Temporary memory unprotection control and status register | 0x00 |

**Table 19. Option byte description (continued)**

| Option byte no. | Description |
|---|---|
| OPT12 | **TMU_KEY 5 [7:0]: Temporary unprotection key 4**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT13 | **TMU_KEY 6 [7:0]: Temporary unprotection key 5**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT14 | **TMU_KEY 7 [7:0]: Temporary unprotection key 6**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT15 | **TMU_KEY 8 [7:0]: Temporary unprotection key 7**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT16 | **TMU_MAXATT [7:0]: TMU access failure counter**<br>TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte).<br>When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter.<br>When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased. |
| OPT17 | **BL[7:0]: Bootloader enable**<br>If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560). |

**Figure 30. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

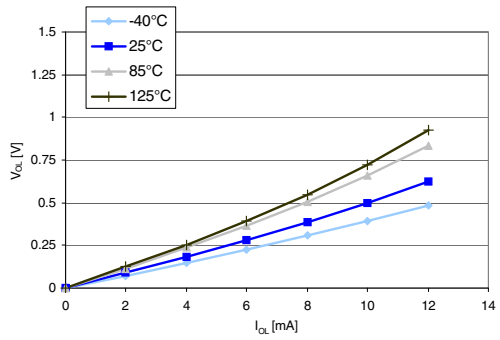



**Figure 31. Typ. $V_{OL}$ @ $V_{DD}$ = 5.0 V (high sink ports)**

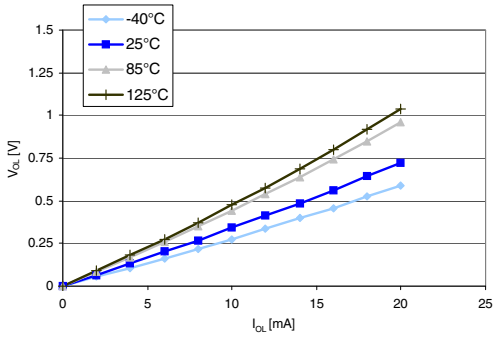



**Figure 32. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (standard ports)**

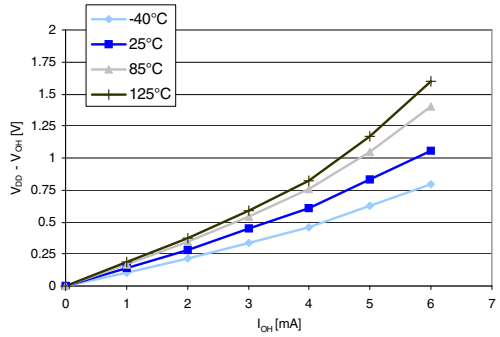



**Figure 33. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (standard ports)**

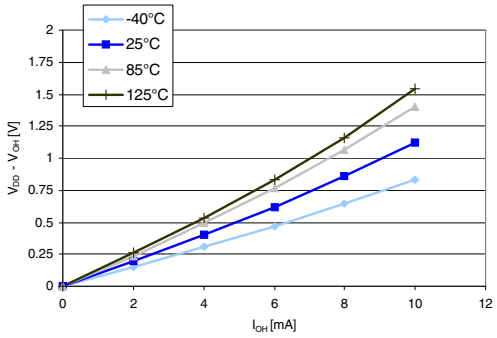



**Figure 34. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

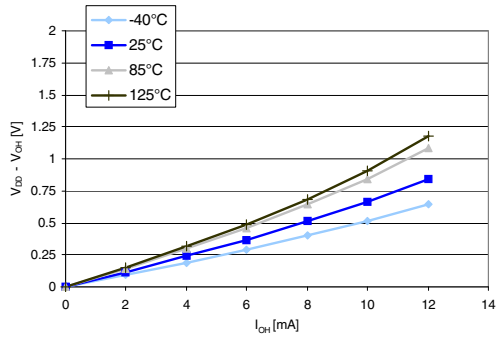



**Figure 35. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (high sink ports)**

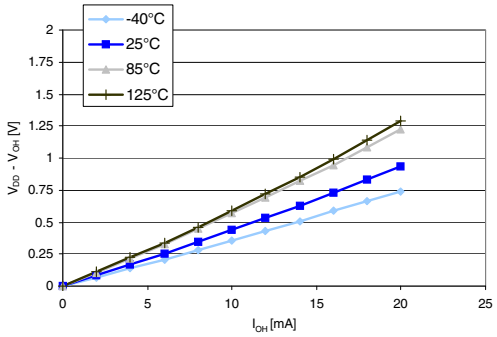
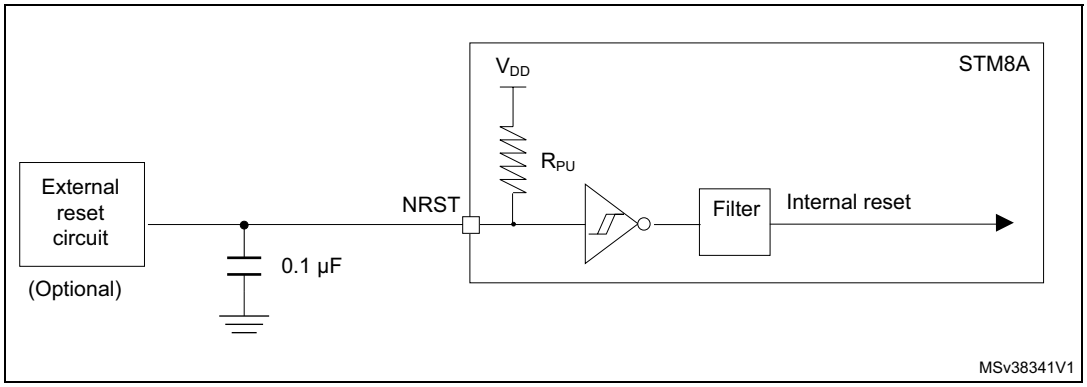


**Figure 39. Recommended reset pin protection**




### 10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for $V_{DD}$, $f_{MASTER}$ and $T_A$.

**Table 40. TIM 1, 2, 3, and 4 electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{EXT}$ | Timer external clock frequency(1) | - | - | - | 24 | MHz |

1. Not tested in production.

### 10.3.11 10-bit ADC characteristics

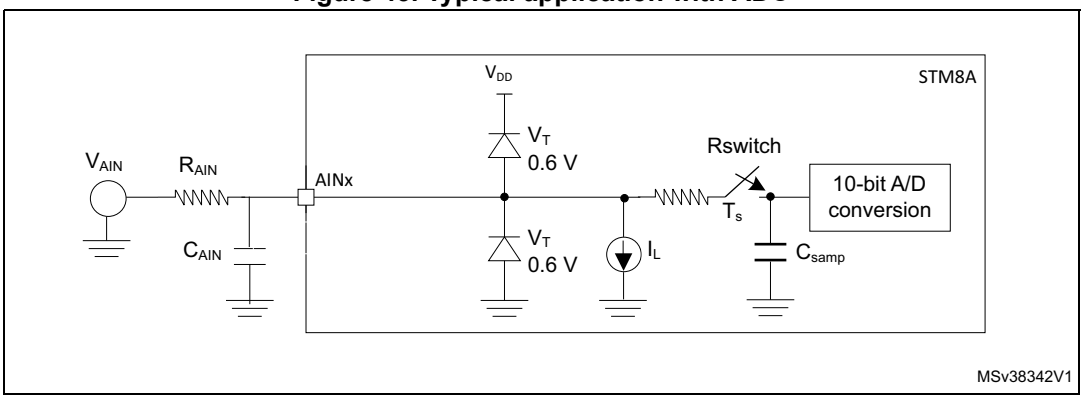
Subject to general operating conditions for $V_{DDA}$, $f_{MASTER}$ and $T_A$ unless otherwise specified.

**Table 43. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | - | 111 kHz | - | 4 MHz | kHz/MHz |
| $V_{DDA}$ | Analog supply | - | 3 | - | 5.5 | V |
| $V_{REF+}$ | Positive reference voltage | - | 2.75 | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | $V_{SSA}$ | - | 0.5 | |
| $V_{AIN}$ | Conversion voltage range(1) | - | $V_{SSA}$ | - | $V_{DDA}$ | |
| | | Devices with external $V_{REF+}$/ $V_{REF-}$ pins | $V_{REF-}$ | - | $V_{REF+}$ | |
| $C_{samp}$ | Internal sample and hold capacitor | - | - | - | 3 | pF |
| $t_S$(1) | Sampling time (3 x 1/$f_{ADC}$) | $f_{ADC}$ = 2 MHz | - | 1.5 | - | µs |
| | | $f_{ADC}$ = 4 MHz | - | 0.75 | - | |
| $t_{STAB}$ | Wakeup time from standby | $f_{ADC}$ = 2 MHz | - | 7 | - | |
| | | $f_{ADC}$ = 4 MHz | - | 3.5 | - | |
| $t_{CONV}$ | Total conversion time including sampling time (14 x 1/$f_{ADC}$) | $f_{ADC}$ = 2 MHz | - | 7 | - | |
| | | $f_{ADC}$ = 4 MHz | - | 3.5 | - | |
| $R_{switch}$ | Equivalent switch resistance | - | - | - | 30 | kΩ |

1. During the sample time, the sampling capacitance, $C_{samp}$ (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_S$. After the end of the sample time $t_S$, changes of the analog input voltage have no effect on the conversion result.

**Figure 43. Typical application with ADC**




1. Legend: $R_{AIN}$ = external resistance, $C_{AIN}$ = capacitors, $C_{samp}$ = internal sample and hold capacitor.

### Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

**Table 46. EMI data**

| Symbol | Parameter | Conditions | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | General conditions | Monitored frequency band | Max $f_{CPU}$(1) | | | |
| | | | | 8 MHz | 16 MHz | 24 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP80 package conforming to IEC 61967-2 | 0.1 MHz to 30 MHz | 15 | 17 | 22 | dBµV |
| | | | 30 MHz to 130 MHz | 18 | 22 | 16 | |
| | | | 130 MHz to 1 GHz | -1 | 3 | 5 | |
| | EMI level | | - | 2 | 2.5 | 2.5 | |

1. Guaranteed by characterization results, not tested in production.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**Table 47. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = 25 °C, conforming to JESD22-A114 | 3A | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-C101 | 3 | 500 | |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-A115 | B | 200 | |

1. Guaranteed by characterization results, not tested in production

### Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 48. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = 25 °C | A |
| | | $T_A$ = 85 °C | |
| | | $T_A$ = 125 °C | |
| | | $T_A$ = 150 °C | |

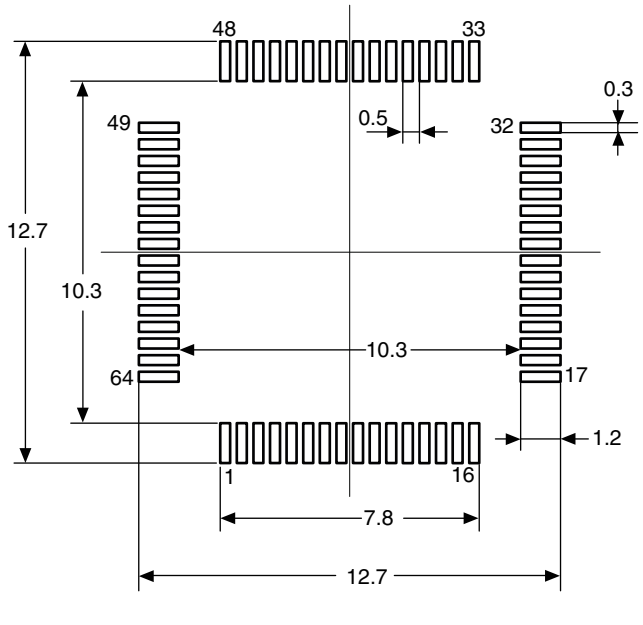
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

**Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

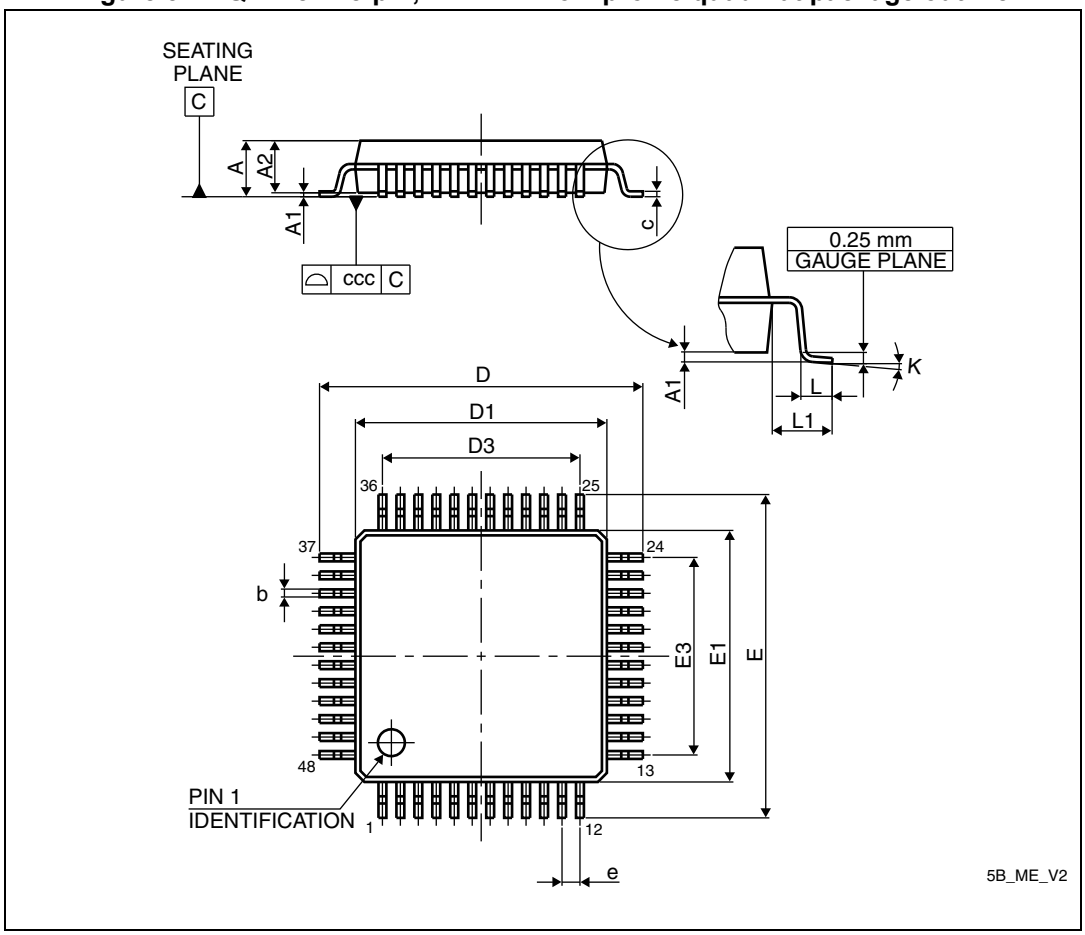
**Figure 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 11.3 LQFP48 package information

**Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 22-Aug-2008 | 2 (continued) | *Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers.<br>*Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL)<br>*Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU).<br>*Table 23: Operating lifetime:* Amended footnotes.<br>*Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'.<br>*Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes.<br>*Table 28: Oscillator current consumption*: Replaced.<br>*Table 29: Programming current consumption*: Amended maximum data and footnotes.<br>*Table 21: Current characteristics*: Replaced.<br>*Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes.<br>*Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes.<br>*Figure 13* to *Figure 18*: info on peripheral activity added.<br>*Table 33: HSI oscillator characteristics*: Modified $f_{HSE\_ext}$ data and added $V_{HSEdhl}$ data.<br>*Table 35: Flash program memory/data EEPROM memory*: Removed $ACC_{HSI}$ parameters and replaced with $ACC_{HS}$ parameters; amended data and footnotes.<br>Amended data of '*RAM and hardware registers*' table.<br>*Table 37: Data memory*: Updated names and data of $N_{RW}$ and $t_{RET}$ parameters.<br>*Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added $V_{OH}$ and $V_{OL}$ parameters; Updated $I_{lkg\ ana}$ parameter.<br>Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*.<br>*Table 46: EMI data*: Updated $f_{ADC}$, $t_S$, and $t_{CONV}$ data.<br>*Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters.<br>*Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2.<br>*Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for $T_A$ = 145 °C.<br>*Figure 53*: Updated memory size, pin count and package type information. |

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 13-Apr-2010 | 6 | Updated title on cover page.<br>Modified cover page header to clarify the part numbers covered by the datasheets. Updated footnote on *Table 1: Device summary* to add 'P' order codes.<br>Changed definition of 'P' order codes.<br>'Q' order codes (FASTROM and EEPROM) removed.<br>Reorganized the content of *Section 5: Product overview*.<br>*Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* updated PD7/TLI alternate function, removed caution note for PD6/ LINUART_RX, and added note to PA1/OSCIN.<br>Renamed *Section 7: Memory and register map*, and merged content with *Section: Register map*. Updated *Figure 8: Register and memory map*.<br>Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table 18: Option bytes*.<br>Updated AFR4 definition in *Table 19: Option byte description*.<br>Added $C_{EXT}$ in *Table 24: General operating conditions*, and *Section 10.3.1: VCAP external capacitor*.<br>Updated $t_{VDD}$ in *Table 25: Operating conditions at power-up/power-down*.<br>Moved *Table 30: Typical peripheral current consumption VDD = 5.0 V* to *Section : Current consumption for on-chip peripherals*.<br>Removed $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*.<br>Updated *Section 12: Ordering information* to the devices supported by the datasheet.<br>Updated *Section 13: STM8 development tools*. |
| 08-Jul-2010 | 7 | Added STM8AF5168 and STM8AF518A part number in *Figure 4*, and STM8AF618A in *Figure 5*. Added STM8AF52xx, STM8AF6269, STM8AF628x, and STM8AF62Ax.<br>Updated D temperature range to -40 to 150°C.<br>Updated number of I/Os on cover page.<br>Added *Table 23: Operating lifetime*.<br>Restored $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*.<br>*Table 24: General operating conditions*: updated $V_{CAP}$ information.<br>ESL parameter, and range D maximum junction temperature ($T_J$).<br>Added STM8AF52xx and STM8AF62xx, and footnote in *Section 12: Ordering information*.<br>Updated *Section 13: STM8 development tools*: added *Table: Product evolution summary*, and split the beCAN time triggered communication mode limitation in two sections. |