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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6269tcy

1 Introduction

This datasheet refers to the STM8AF526x/8x/Ax and STM8AF6269/8x/Ax products with 32 to 128 Kbyte of program memory.

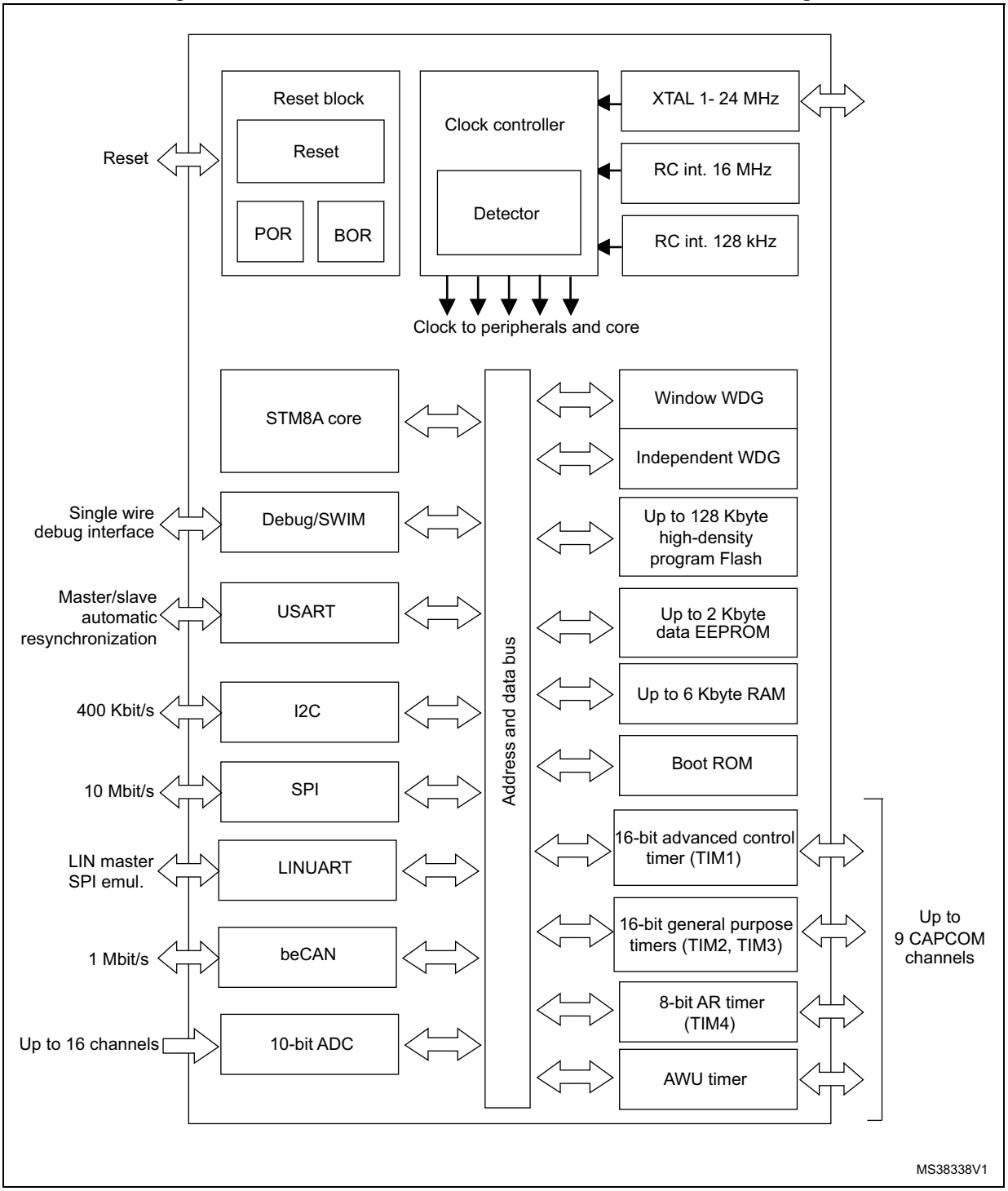
In the order code, the letter ‘F’ refers to product versions with Flash and data EEPROM and ‘P’ to product versions with FASTROM. The identifiers ‘F’ and ‘P’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S and STM8A Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5 Product overview

This section is intended to describe the family features that are actually implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 4. Peripheral clock gating bits (CLK_PCKENR1)

Control bit	Peripheral
PCKEN17	TIM1
PCKEN16	TIM3
PCKEN15	TIM2
PCKEN14	TIM4
PCKEN13	LINUART
PCKEN12	USART
PCKEN11	SPI
PCKEN10	I^2C

5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ for master, 8 Mbit/s or f_{MASTER} /2 for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

5.9.4 Inter integrated circuit (I^2C) interface

The devices covered by this datasheet contain one I^2C interface. The interface is available on all the supported packages.

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Table 13. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX(1)
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX(1)
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX(1)
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

1. Depends on the external circuitry.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			

Table 15. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only
2. Product dependent value, see *Figure 8: Register and memory map*.

Table 16. Temporary memory unprotection registers

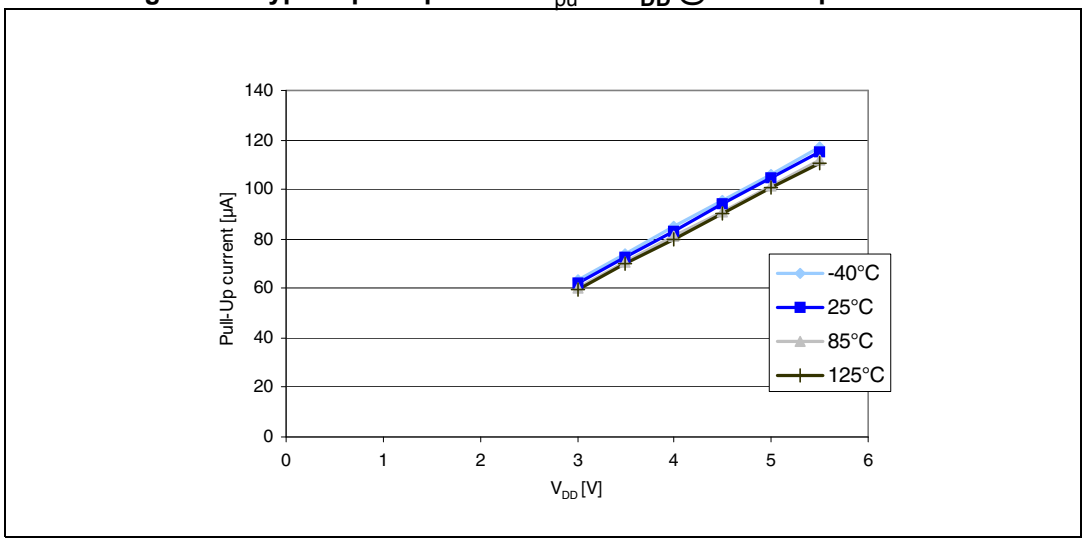
Address	Block	Register label	Register name	Reset status
0x00 5800	TMU	TMU_K1	Temporary memory unprotection key register 1	0x00
0x00 5801		TMU_K2	Temporary memory unprotection key register 2	0x00
0x00 5802		TMU_K3	Temporary memory unprotection key register 3	0x00
0x00 5803		TMU_K4	Temporary memory unprotection key register 4	0x00
0x00 5804		TMU_K5	Temporary memory unprotection key register 5	0x00
0x00 5805		TMU_K6	Temporary memory unprotection key register 6	0x00
0x00 5806		TMU_K7	Temporary memory unprotection key register 7	0x00
0x00 5807		TMU_K8	Temporary memory unprotection key register 8	0x00
0x00 5808		TMU_CSR	Temporary memory unprotection control and status register	0x00

Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 °C to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 24 MHz 1 ws	8.7	16.8(2)	mA
			f_{CPU} = 16 MHz	7.4	14	
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	f_{CPU} = 24 MHz	4.4	6.0(2)	
			f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 24 MHz	2.4	3.1(2)	
			f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

Figure 25. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures(1)



1. The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 26 to *Figure 35* show typical output level curves measured with output on a single pin.

Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

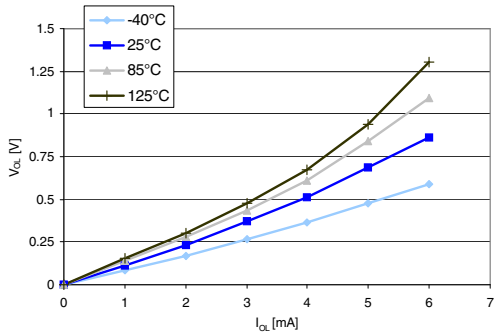


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

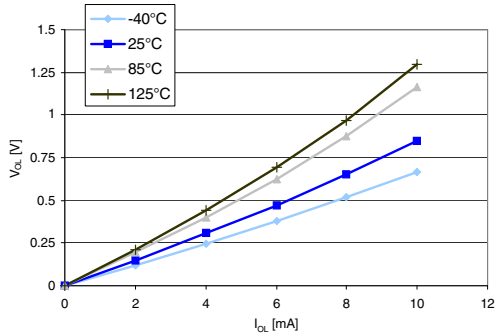


Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

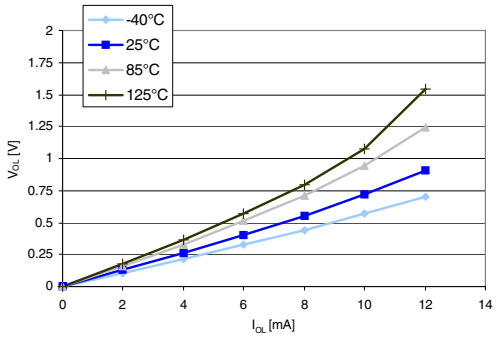


Figure 29. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

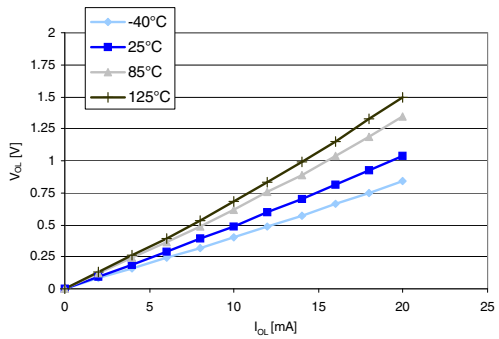
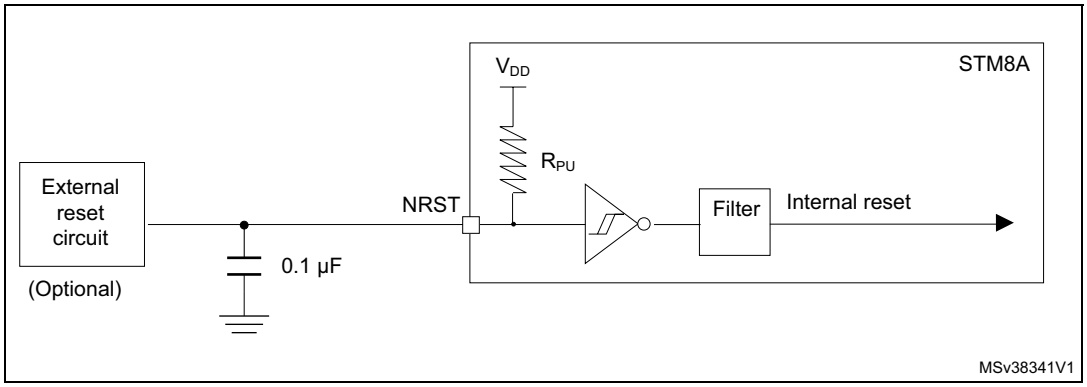


Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

1. Not tested in production.

10.3.11 10-bit ADC characteristics

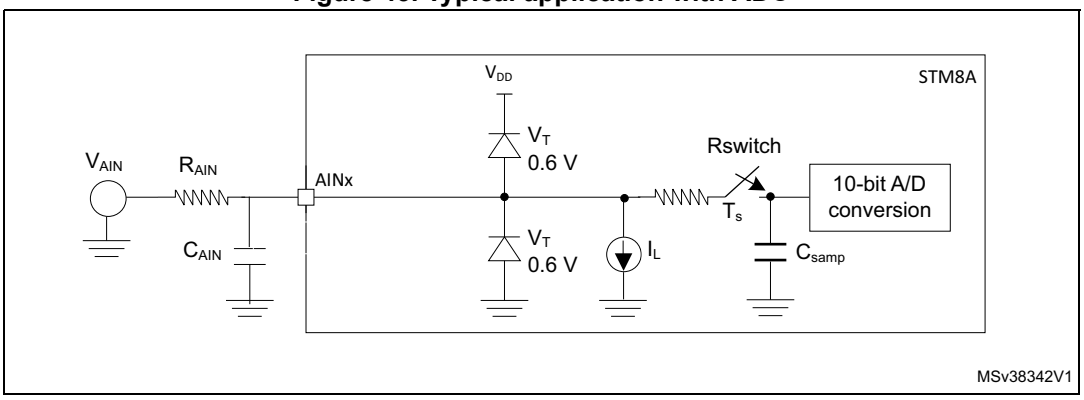
Subject to general operating conditions for V_{DDA}, f_{MASTER} and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 43. Typical application with ADC



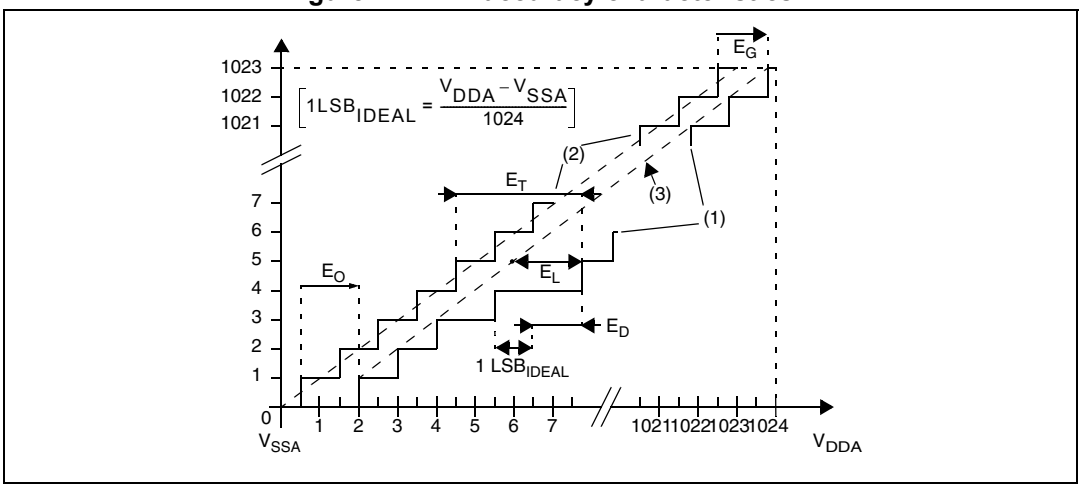
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Table 44. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

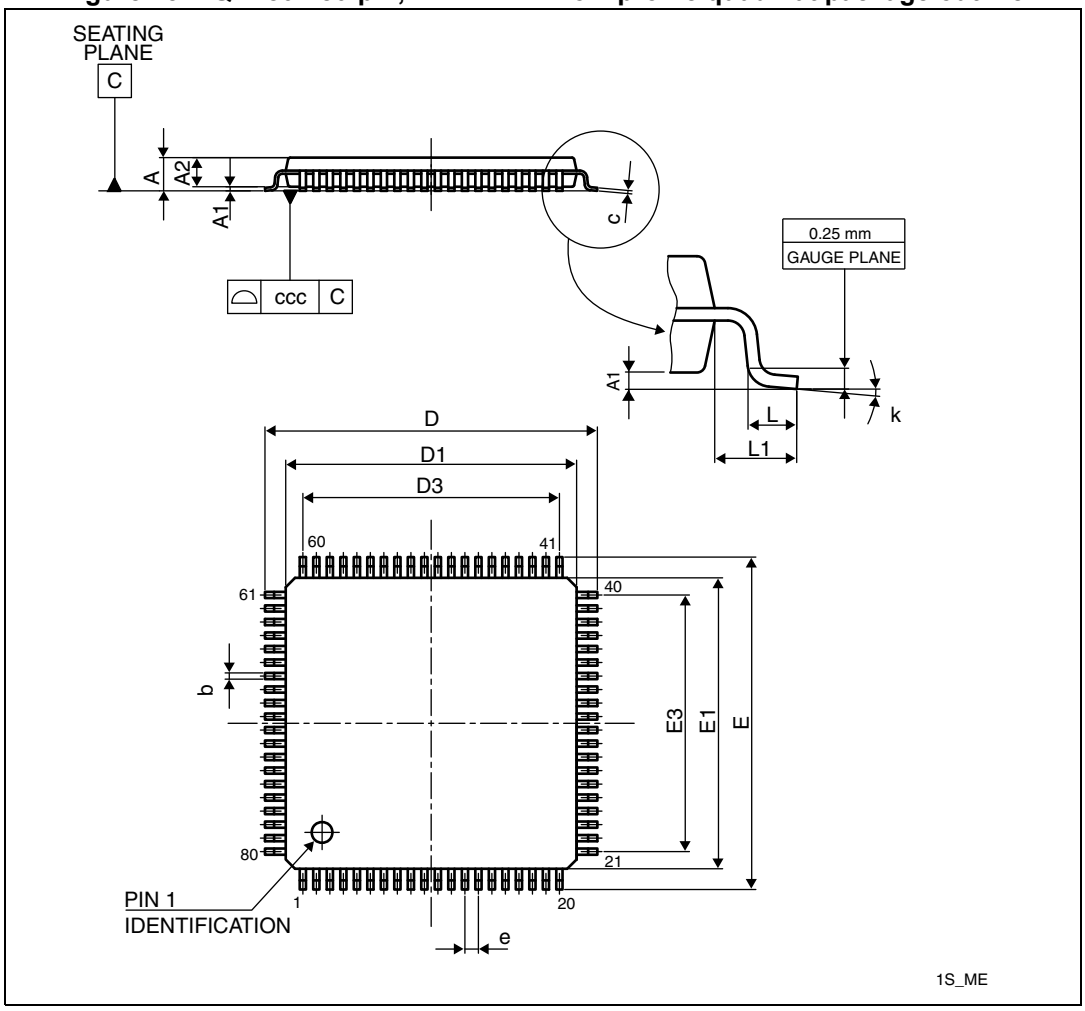
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

11.1 LQFP80 package information

Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Aug-2008	2 (continued)	*Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers. *Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL) *Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU). *Table 23: Operating lifetime:* Amended footnotes. *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'. *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes. *Table 28: Oscillator current consumption*: Replaced. *Table 29: Programming current consumption*: Amended maximum data and footnotes. *Table 21: Current characteristics*: Replaced. *Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes. *Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes. *Figure 13* to *Figure 18*: info on peripheral activity added. *Table 33: HSI oscillator characteristics*: Modified f_{HSE_ext} data and added V_{HSEdhl} data. *Table 35: Flash program memory/data EEPROM memory*: Removed ACC_{HSI} parameters and replaced with ACC_{HS} parameters; amended data and footnotes. Amended data of '*RAM and hardware registers*' table. *Table 37: Data memory*: Updated names and data of N_{RW} and t_{RET} parameters. *Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added V_{OH} and V_{OL} parameters; Updated $I_{lkg\ ana}$ parameter. Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*. *Table 46: EMI data*: Updated f_{ADC}, t_S, and t_{CONV} data. *Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters. *Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2. *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for T_A = 145 °C. *Figure 53*: Updated memory size, pin count and package type information.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8 (continued)	Removed note 1 in *Table 24: General operating conditions* and note 1 below *Figure 11: fCPUmax versus VDD*. Removed note 3 in *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C*. Removed note 2 in *Table 31: HSE external clock characteristics* and *Table 35: Flash program memory/data EEPROM memory* Removed note 1 in *Table 37: Data memory*. Modified T_{WE} maximum value in *Table 36: Flash program memory* and *Table 37: Data memory*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table 39: NRST pin characteristics*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 39: Recommended reset pin protection,* and updated external capacitor value. Updated *Note 1* in *Table 40: TIM 1, 2, 3, and 4 electrical specifications.* Updated *Note 1* in *Table 41: SPI characteristics.* Moved know limitations to separate errata sheet. Added “not recommended for new design” note to device family 51, memory size 7 and 9, and temperature range B, in *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added Raisonance compiler in *Section 13.2: Software tools.*
18-Jul-2012	9	Updated wildcards of document part numbers. Added VFQFPN package. Added STM8AF62A6 part number. *Table 1: Device summary* updated footnote *1* and added footnote *2*. *Table: STM8AF52xx product line-up with CAN* and *Table: STM8AF62xx product line-up without CAN*: added “P” version for all order codes; updated size of data EEPROM for 64K devices to 2K instead of 1.5K; updated RAM. *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram*: updated POR, BOR and WDG; removed PDR; added legend. *Section 5.4: Flash program and data EEPROM*: removed non relevant bullet points and added a sentence about the factory program. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)* and updated *Table 5: Peripheral clock gating bits (CLK_PCKENR2)* *Section : ADC features*: updated ADC input range. *Table 12: Memory model 128K:* updated RAM size, RAM end addresses, and stack roll-over addresses; updated footnote *1* *Table 18: Option bytes:* updated factory default setting for NOPT17; updated footnotes. *Table 20: Voltage characteristics:* updated V_{DDX} - V_{DD} to V_{DDX} - V_{SS}. *Table 24: General operating conditions:* updated V_{CAP}.