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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6288tay

2 Description

The STM8AF526x/8x/Ax and STM8AF6269/8x/Ax automotive 8-bit microcontrollers described in this datasheet offer from 32 Kbyte to 128 Kbyte of non volatile memory and integrated true data EEPROM. They are referred to as high density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

The STM8AF52 series features a CAN interface.

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, wtachdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map, and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5.5 V operating supply.

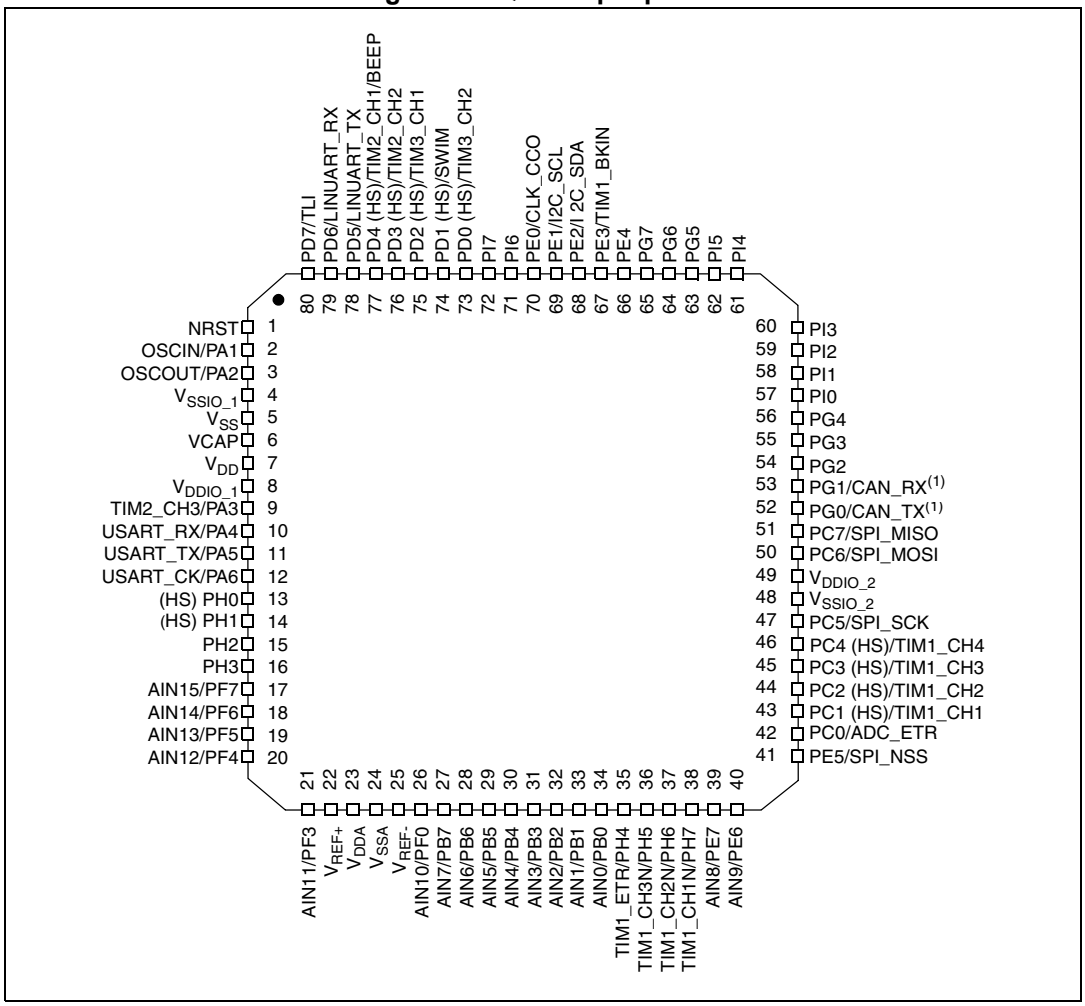
All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. (HS) stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC positive reference voltage		-
23	19	13	9	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
24	20	14	10	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
25	21	-	-	-	V_{REF-}	S	-	-	-	-	-	-	-	ADC negative reference voltage		-
26	22	-	-	-	PF0/AIN10	I/O	**X**	X	-	-	O1	X	X	**Port F0**	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X	-	-	O1	X	X	**Port H4**	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X	-	-	O1	X	X	**Port H5**	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X	-	-	O1	X	X	**Port H6**	Timer 1 - inverted channel 2	-

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			

Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 °C to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 24 MHz 1 ws	8.7	16.8(2)	mA
			f_{CPU} = 16 MHz	7.4	14	
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	f_{CPU} = 24 MHz	4.4	6.0(2)	
			f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 24 MHz	2.4	3.1(2)	
			f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 °C to 150 °C.

Table 35. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 16 to 24 MHz with 1 ws f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 16 to 24 MHz with 1 ws f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	

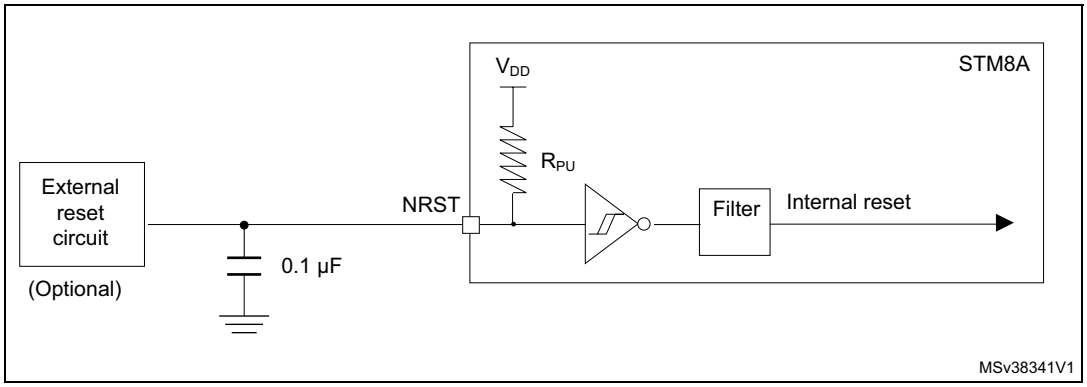
1. Guaranteed by characterization results, not tested in production.

Table 36. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

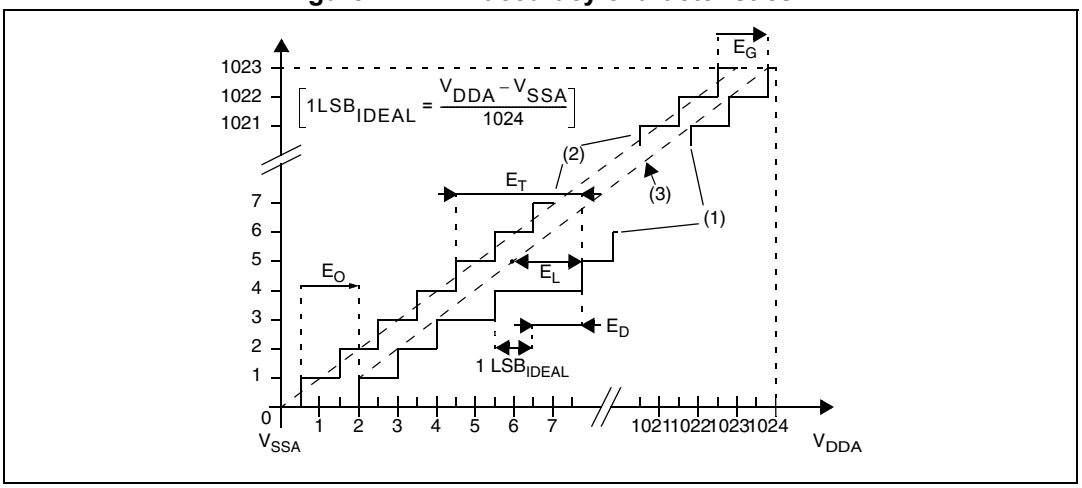
1. Not tested in production.

Table 44. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

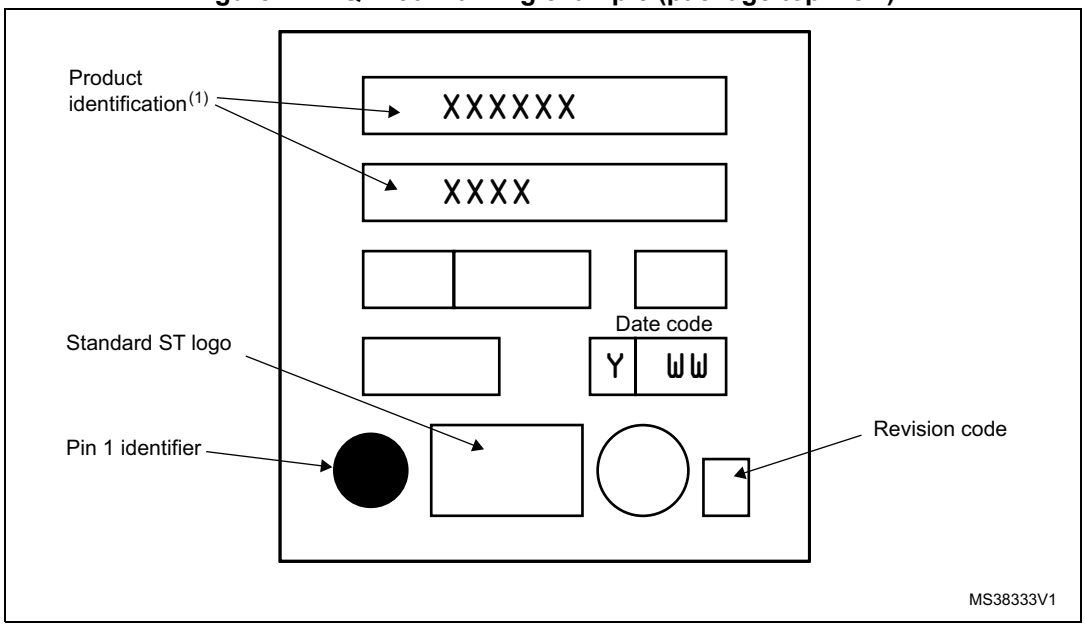
1. Guaranteed by characterization results, not tested in production

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP80 marking example (package top view)



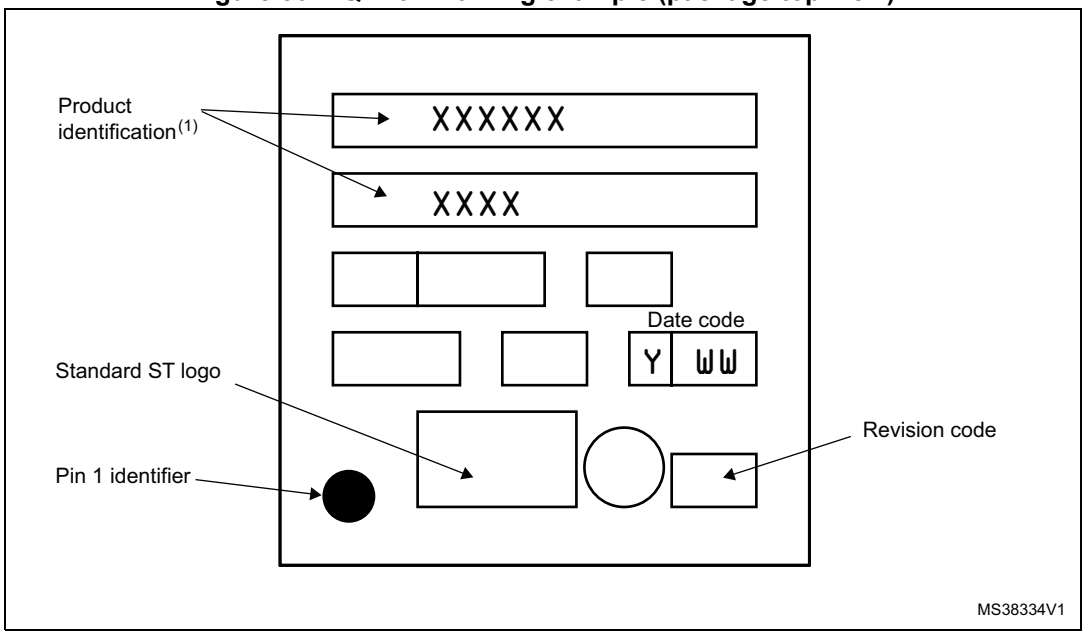
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP64 marking example (package top view)



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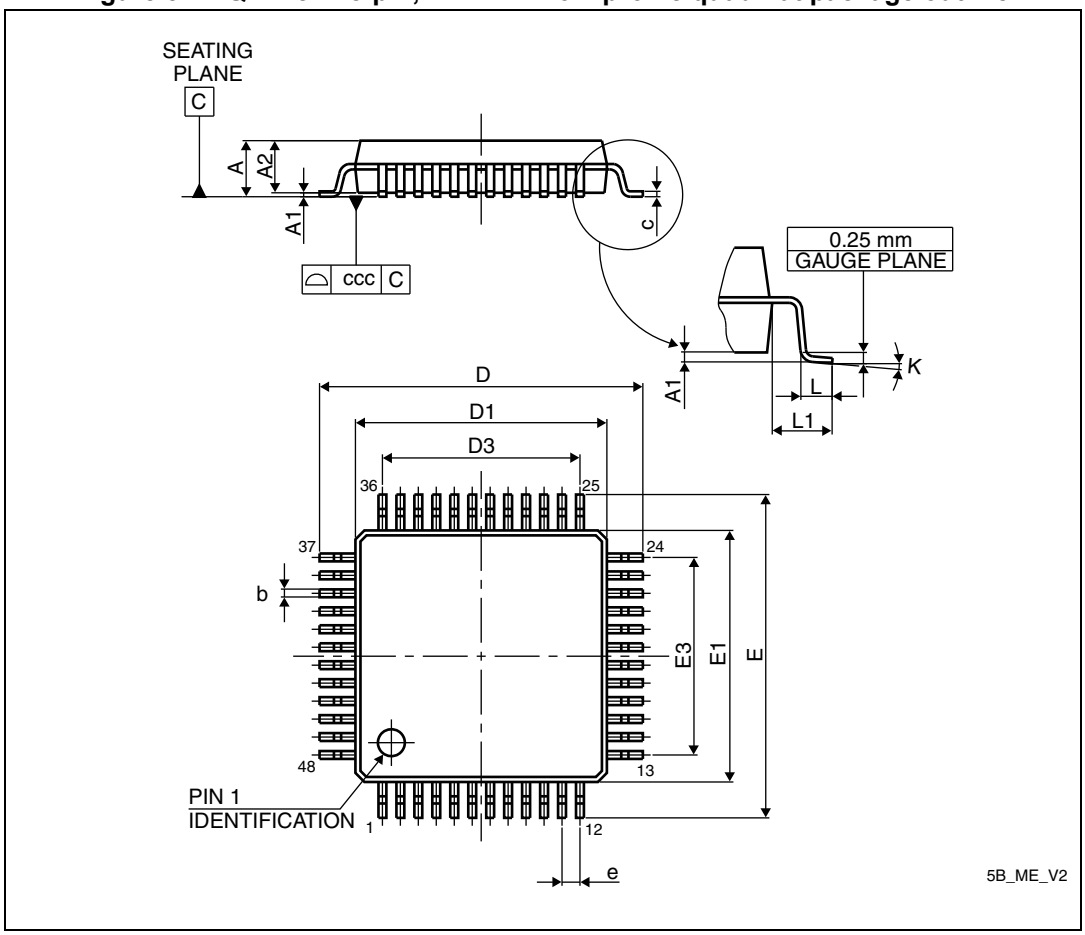
11.3 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



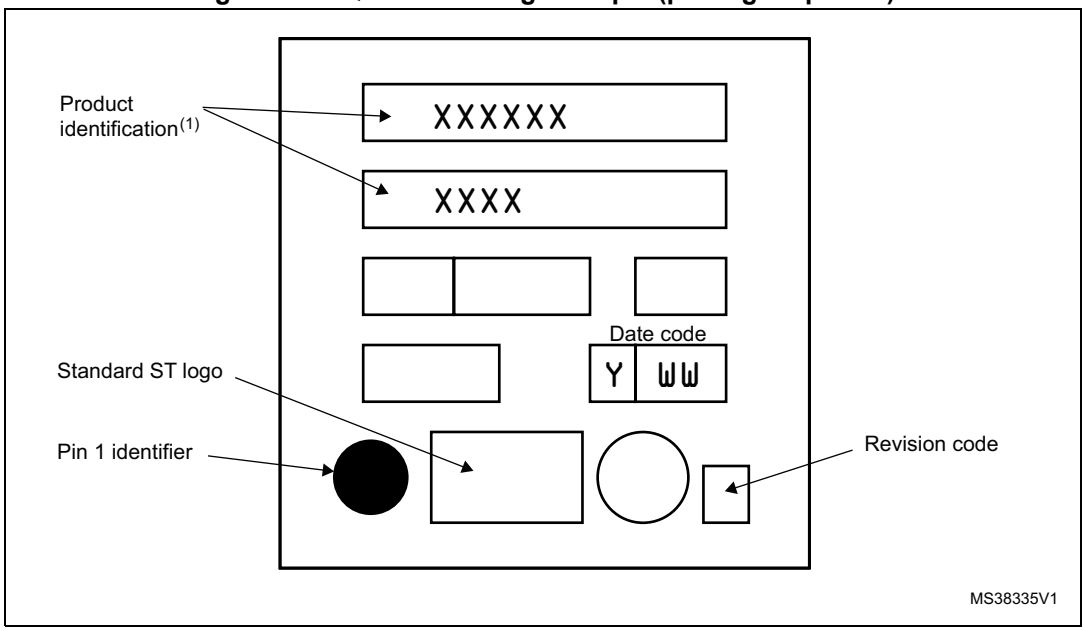
1. Drawing is not to scale.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. LQFP48 marking example (package top view)



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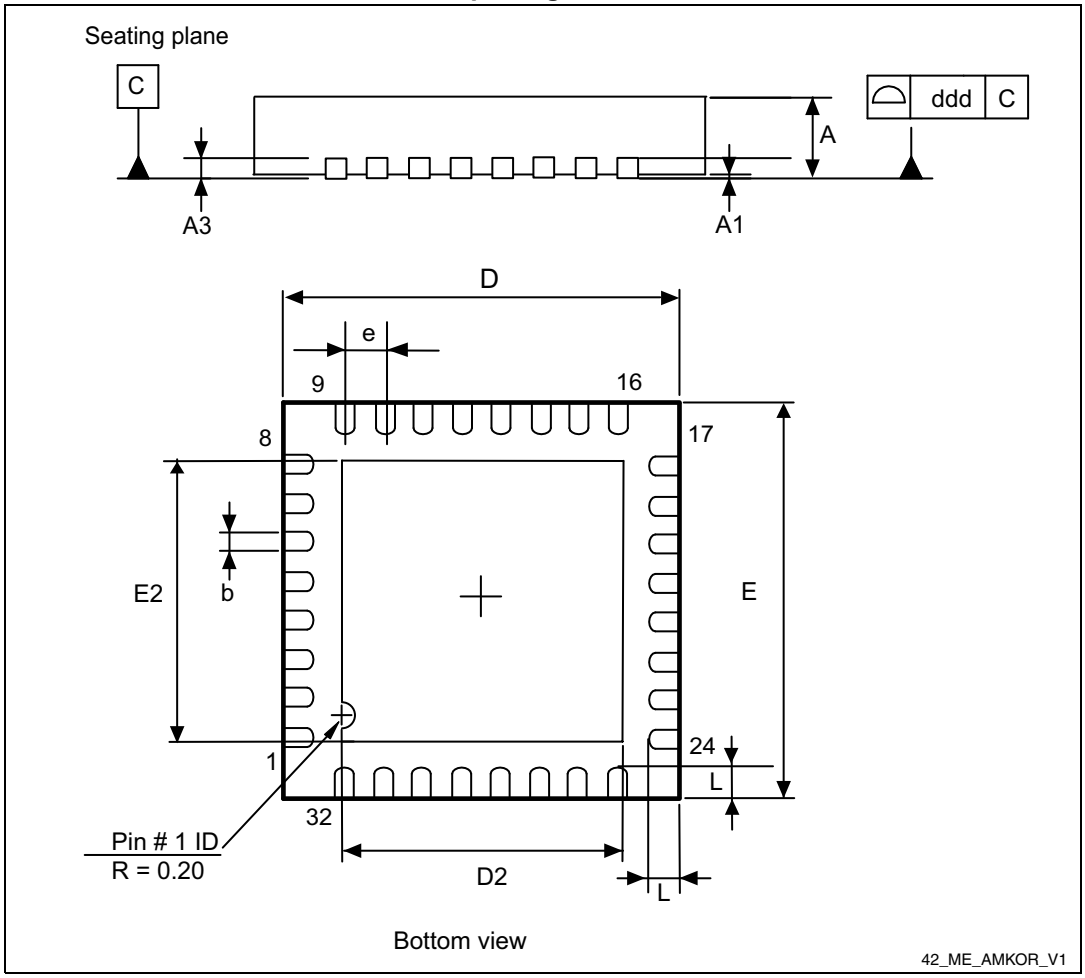
11.5 VFQFPN32 package information

Figure 57. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



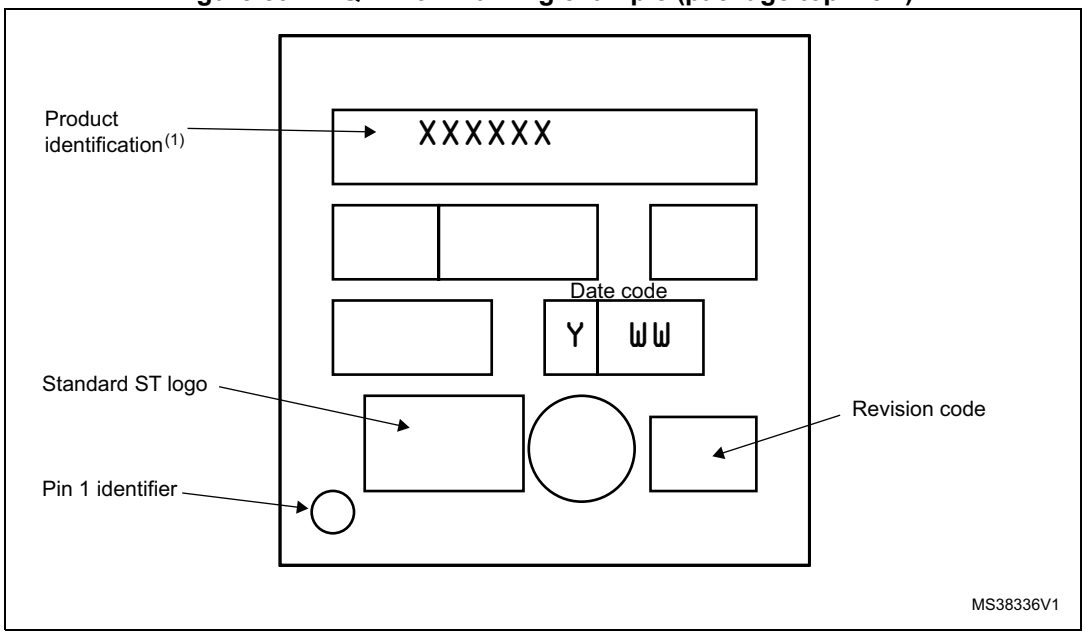
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. VFQFPN32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

14 Revision history

Table 55. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release
22-Aug-2008	2	Added 'H' products to the datasheet (Flash no EEPROM). *Section : Features* on cover page: Updated Memories, Reset and supply management, Communication interfaces and I/Os; reduced wakeup pins by 1. *Table 1: Device summary*: Removed STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF5168, STM8AF5186, STM8AF5176, and STM8AF5166. *Section 1: Introduction*, *Section 5: Product overview*, *Section 9: Option bytes*, *Section 6.2: Alternate function remapping*, *Table 21: Current characteristics:* Updated reference documentation: RM0009, PM0047, and UM0470. *Section 2: Description*: added information about peak performance. *Section 3: Product line-up*: Removed *STM8A common features* table. *Table 4: Peripheral clock gating bits (CLK_PCKENR1):* Removed STM8AF5186T, STM8AF5176T, STM8AF5168T, and STM8AF5166T. *Table 5: Peripheral clock gating bits (CLK_PCKENR2)*: Removed STM8AF6168T, STM8AF6166T, STM8AF6148T, and STM8AF6146T. *Section 5: Product overview*: Made minor content changes and improved readability and layout. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: Major modification, TMU included. *Section 5.5.2: 16 MHz high-speed internal RC oscillator (HSI)*: User trimming updated. *Section 5.5.3: 128 kHz low-speed internal RC oscillator (LSI)*: LSI as CPU clock added. *Section 5.5.4: 24 MHz high-speed external crystal oscillator (HSE)*, *Section 5.5.5: External clock input*: Maximum frequency conditional 32 Kbyte/128 Kbyte. *Section 5.8: Analog to digital converter (ADC)*: Scan for 128 Kbyte removed. *Section 5.9: Communication interfaces*, *Section 5.9.3: Serial peripheral interface (SPI)*: SPI 10 Mb/s. *Figure 3: LQFP 80-pin pinout*, *Figure 4: LQFP 64-pin pinout*, *Figure 6: STM8AF62xx LQFP/VFQFPN 32-pin pinout*: Amended footnote 1. *Table 12: Memory model 128K:* HS output changed from 20 mA to 8 mA. *Section 7: Memory and register map*: Corrected *Table 8: Register and memory map*; removed address list; added *Table 14: General hardware register map*. *Section 10.3.2: Supply current characteristics* Note on typical/WC values added.

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	Replaced the salestype 'STM8H61xx' with 'STM8AH61xx on the first page. Added 'part numbers' to heading rows of *Table 1: Device summary*. Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD. *Table 18*: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]' *Section 9*: Updated introductory text concerning option bytes which do not need to be saved in a complementary form. *Table 18*: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively. *Table 21*: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'. Updated 80-pin package information in line with POA 0062342-revD in *Figure 45* and *Table 53*.
01-Jul-2009	4	Added 'STM8AH61xx' and 'STM8AH51xx to document header. Updated *: Features on page 1* (memories, timers, operating temperature, ADC and I/Os). Updated *Table 1: Device summary* Updated Kbyte value of program memory in *Section: Introduction* Changed the first two lines from the top in *Section: Description*. Updated *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram* Updated *Section 5: Product overview* In *Figure 5: LQFP 48-pin pinout*, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively. *Section 6: Pinouts and pin description:* deleted the text below the *Table 10: Legend/abbreviation for the pin description table* *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description:* 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote. Updated *Figure 8: Register and memory map*. *Table 12: Memory model 128K:* updated footnote Deleted the *Table: Stack and RAM partitioning* *Table 17: STM8A interrupt table*: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote Updated *Section 7: Memory and register map* Updated *Table: Data memory, Table: I/O static characteristics,* and *Table 39: NRST pin characteristics*. *Section 10.1.1: Minimum and maximum values:* added ambient temperature T_A = -40 °C Updated *Table 20: Voltage characteristics*. Updated *Table 21: Current characteristics*. Updated *Table 22: Thermal characteristics*. Updated *Table 24: General operating conditions*.