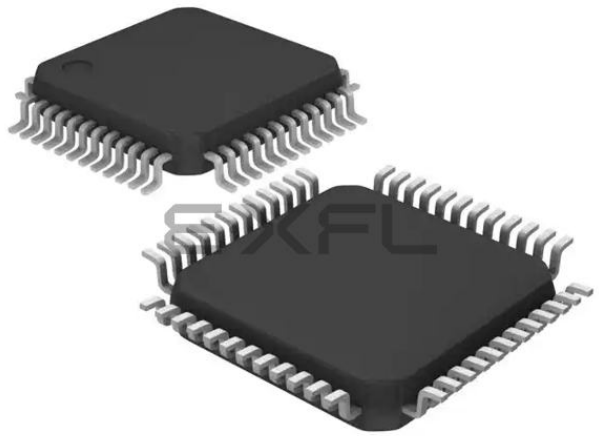

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | STM8A |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6288tcy |

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## 5.2 Single wire interface module (SWIM) and debug module (DM)

### 5.2.1 SWIM

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 bytes/ms.

### 5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-flavored emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

## 5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 24 interrupt vectors with hardware priority
- Five vectors for external interrupts (up to 37 depending on the package)
- Trap and reset interrupts

## 5.4 Flash program and data EEPROM

- 32 Kbytes to 128 Kbytes of high density single voltage Flash program memory
- Up to 2 Kbytes true (not emulated) data EEPROM
- Read while write: writing in the data memory is possible while executing code in the Flash program memory.

The whole Flash program memory and data EEPROM are factory programmed with 0x00.

### 5.4.1 Architecture

- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

### 5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ for master, 8 Mbit/s or $f_{MASTER}$ /2 for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

### 5.9.4 Inter integrated circuit ($I^2C$) interface

The devices covered by this datasheet contain one $I^2C$ interface. The interface is available on all the supported packages.

- $I^2C$ master features:
  - Clock generation
  - Start and stop generation
- $I^2C$ slave features:
  - Programmable $I^2C$ address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - $I^2C$ busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

## 5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain ($I^2C$ interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

**Caution:** In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

**Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description**

| Pin number | | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | STM8AF52x6 VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 1 | 1 | 1 | 1 | 1 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 2 | 2 | 2 | 2 | 2 | PA1/OSCIN(1) | I/O | **X** | X | - | - | O1 | X | X | **Port A1** | Resonator/ crystal in | - |
| 3 | 3 | 3 | 3 | 3 | PA2/OSCOUT | I/O | **X** | X | X | - | O1 | X | X | **Port A2** | Resonator/ crystal out | - |
| 4 | 4 | 4 | - | - | $V_{SSIO\_1}$ | S | - | - | - | - | - | - | - | I/O ground | | - |
| 5 | 5 | 5 | 4 | 4 | $V_{SS}$ | S | - | - | - | - | - | - | - | Digital ground | | - |
| 6 | 6 | 6 | 5 | 5 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 7 | 7 | 7 | 6 | 6 | $V_{DD}$ | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 8 | 8 | 8 | 7 | 7 | $V_{DDIO\_1}$ | S | - | - | - | - | - | - | - | I/O power supply | | - |
| 9 | 9 | 9 | - | - | PA3/TIM2_CH3 | I/O | **X** | X | X | - | O1 | X | X | **Port A3** | Timer 2 - channel 3 | TIM3_CH1 [AFR1] |
| 10 | 10 | 10 | - | - | PA4/USART_RX | I/O | **X** | X | X | - | O3 | X | X | **Port A4** | USART receive | - |
| 11 | 11 | 11 | - | - | PA5/USART_TX | I/O | **X** | X | X | - | O3 | X | X | **Port A5** | USART transmit | - |
| 12 | 12 | 12 | - | 8 | PA6/USART_CK (2) | I/O | **X** | X | X | - | O3 | X | X | **Port A6** | USART synchro nous clock | - |
| 13 | - | - | - | - | PH0 | I/O | X | X | - | HS | O3 | X | X | **Port H0** | - | - |
| 14 | - | - | - | - | PH1 | I/O | **X** | X | - | HS | O3 | X | X | **Port H1** | - | - |
| 15 | - | - | - | - | PH2 | I/O | **X** | X | - | - | O1 | X | X | **Port H2** | - | - |
| 16 | - | - | - | - | PH3 | I/O | **X** | X | - | - | O1 | X | X | **Port H3** | - | - |
| 17 | 13 | - | - | - | PF7/AIN15 | I/O | **X** | X | - | - | O1 | X | X | **Port F7** | Analog input 15 | - |
| 18 | 14 | - | - | - | PF6/AIN14 | I/O | **X** | X | - | - | O1 | X | X | **Port F6** | Analog input 14 | - |
| 19 | 15 | - | - | - | PF5/AIN13 | I/O | **X** | X | - | - | O1 | X | X | **Port F5** | Analog input 13 | - |
| 20 | 16 | - | 8 | - | PF4/AIN12 | I/O | **X** | X | - | - | O1 | X | X | **Port F4** | Analog input 12 | - |
| 21 | 17 | - | - | - | PF3/AIN11 | I/O | **X** | X | - | - | O1 | X | X | **Port F3** | Analog input 11 | - |

**Table 14. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x40 |
| 0x00 5060 to 0x005061 | Reserved area (2 bytes) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 bytes) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 bytes) | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX(1) |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 bytes) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |

**Table 14. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5300 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5301 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5302 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5303 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5304 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5305 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 5306 | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 5307 | | TIM2_CCMR3 | TIM2 capture/compare mode register 3 | 0x00 |
| 0x00 5308 | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 5309 | | TIM2_CCER2 | TIM2 capture/compare enable register 2 | 0x00 |
| 0x00 530A | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 530B | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 00 530C0x | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 530D | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 530E | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 530F | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5310 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5311 | | TIM2_CCR2H | TIM2 capture/compare reg. 2 high | 0x00 |
| 0x00 5312 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5313 | | TIM2_CCR3H | TIM2 capture/compare register 3 high | 0x00 |
| 0x00 5314 | | TIM2_CCR3L | TIM2 capture/compare register 3 low | 0x00 |
| 0x00 5315 to 0x00 531F | Reserved area (11 bytes) | | | |

# 10 Electrical characteristics

## 10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = -40 °C, $T_A$ = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

### 10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

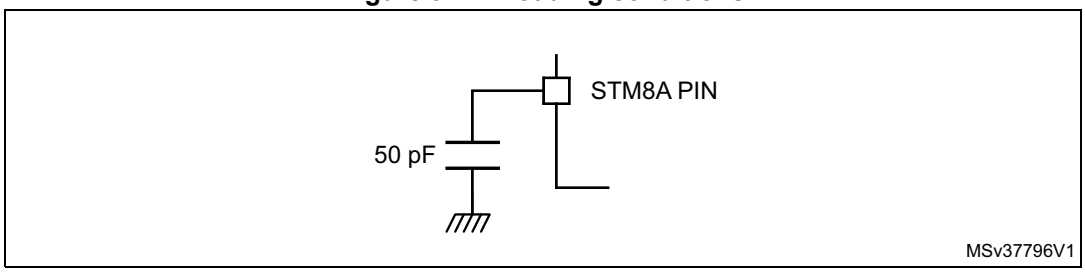
### 10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

**Figure 9. Pin loading conditions**



### 10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$.

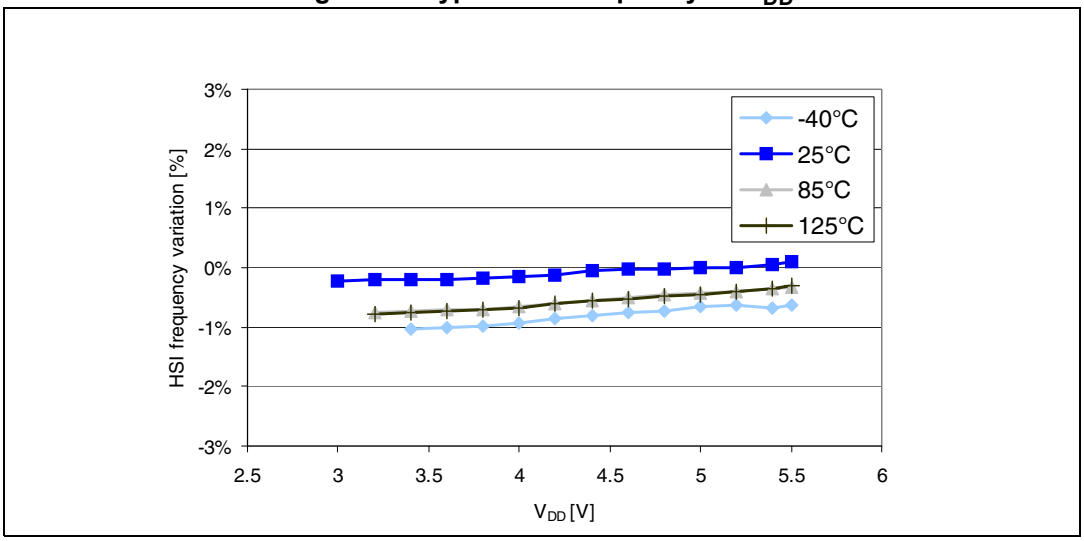
#### High-speed internal RC oscillator (HSI)

**Table 33. HSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HS}$ | HSI oscillator user trimming accuracy | Trimmed by the application for any $V_{DD}$ and $T_A$ conditions | -1 | - | 1 | % |
| | HSI oscillator accuracy (factory calibrated) | $V_{DD} = 3.0\ V \leq V_{DD} \leq 5.5\ V$, $-40\ °C \leq T_A \leq 150\ °C$ | -5 | - | 5 | |
| $t_{su(HSI)}$ | HSI oscillator wakeup time | - | - | - | 2(1) | µs |

1. Guaranteed by characterization results, not tested in production.

**Figure 21. Typical HSI frequency vs $V_{DD}$**



## 10.3.6 I/O port pin characteristics

### General characteristics

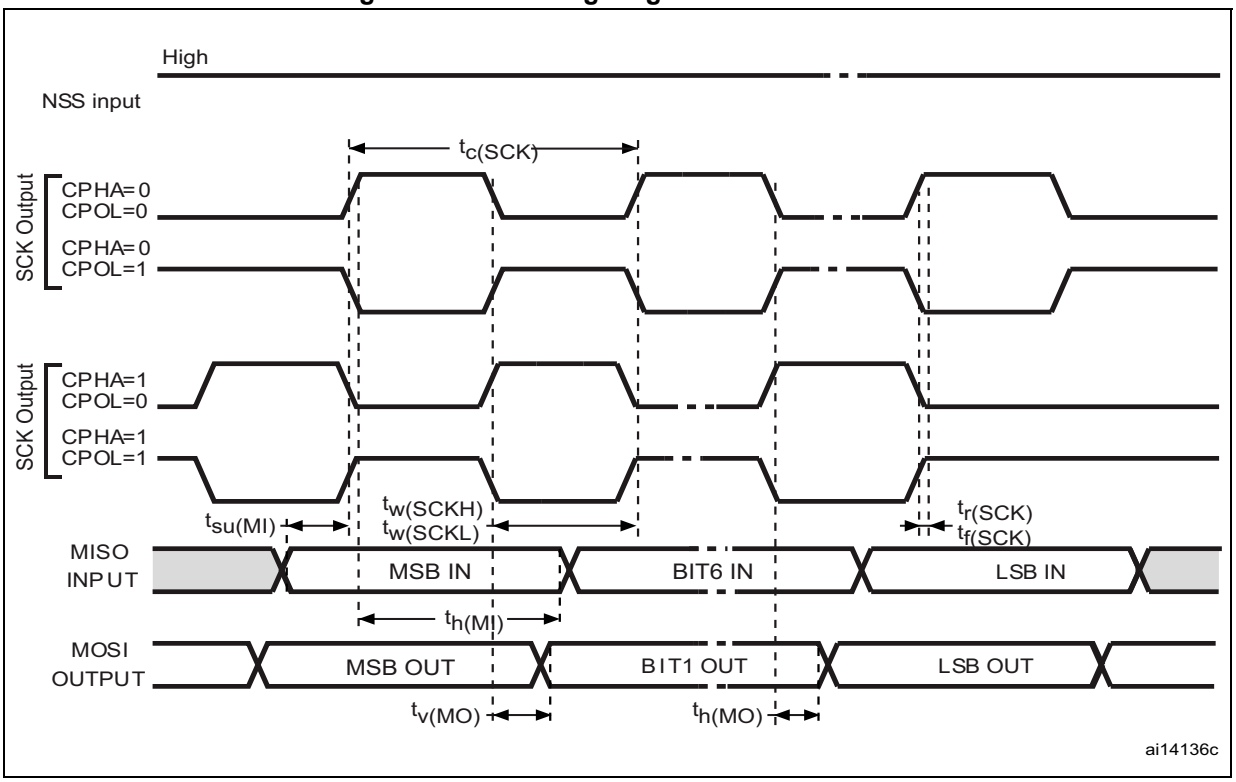
Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 38. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | - | -0.3 V | | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | High-level input voltage | | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 V | |
| $V_{hys}$ | Hysteresis(1) | | - | 0.1 x $V_{DD}$ | - | |
| $V_{OH}$ | High-level output voltage | Standard I/0, $V_{DD}$ = 5 V, I = 3 mA | $V_{DD}$ - 0.5 V | - | - | |
| | | Standard I/0, $V_{DD}$ = 3 V, I = 1.5 mA | $V_{DD}$ - 0.4 V | - | - | |
| $V_{OL}$ | Low-level output voltage | High sink and true open drain I/0, $V_{DD}$ = 5 V I = 8 mA | - | - | 0.5 | V |
| | | Standard I/0, $V_{DD}$ = 5 V I = 3 mA | - | - | 0.6 | |
| | | Standard I/0, $V_{DD}$ = 3 V I = 1.5 mA | - | - | 0.4 | |
| $R_{pu}$ | Pull-up resistor | $V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$ | 35 | 50 | 65 | kΩ |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 35(2) | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125(2) | |
| | | Fast I/Os Load = 20 pF | - | - | 20(2) | |
| | | Standard and high sink I/Os Load = 20 pF | - | - | 50(2) | |
| $I_{lkg}$ | Digital input pad leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |
| $I_{lkg\ ana}$ | Analog input pad leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < $T_A$ < 125 °C | - | - | ±250 | nA |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < $T_A$ < 150 °C | - | - | ±500 | |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O(3) | Injection current ±4 mA | - | - | ±1(3) | µA |
| $I_{DDIO}$ | Total current on either $V_{DDIO}$ or $V_{SSIO}$ | Including injection currents | - | - | 60 | mA |

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

**Figure 42. SPI timing diagram - master mode**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

### 10.3.10 I²C interface characteristics

**Table 42. I²C characteristics**

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max(2) | Min(2) | Max(2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | - | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time ($V_{DD}$ 3 V to 5.5 V) | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time ($V_{DD}$ 3 V to 5.5 V) | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

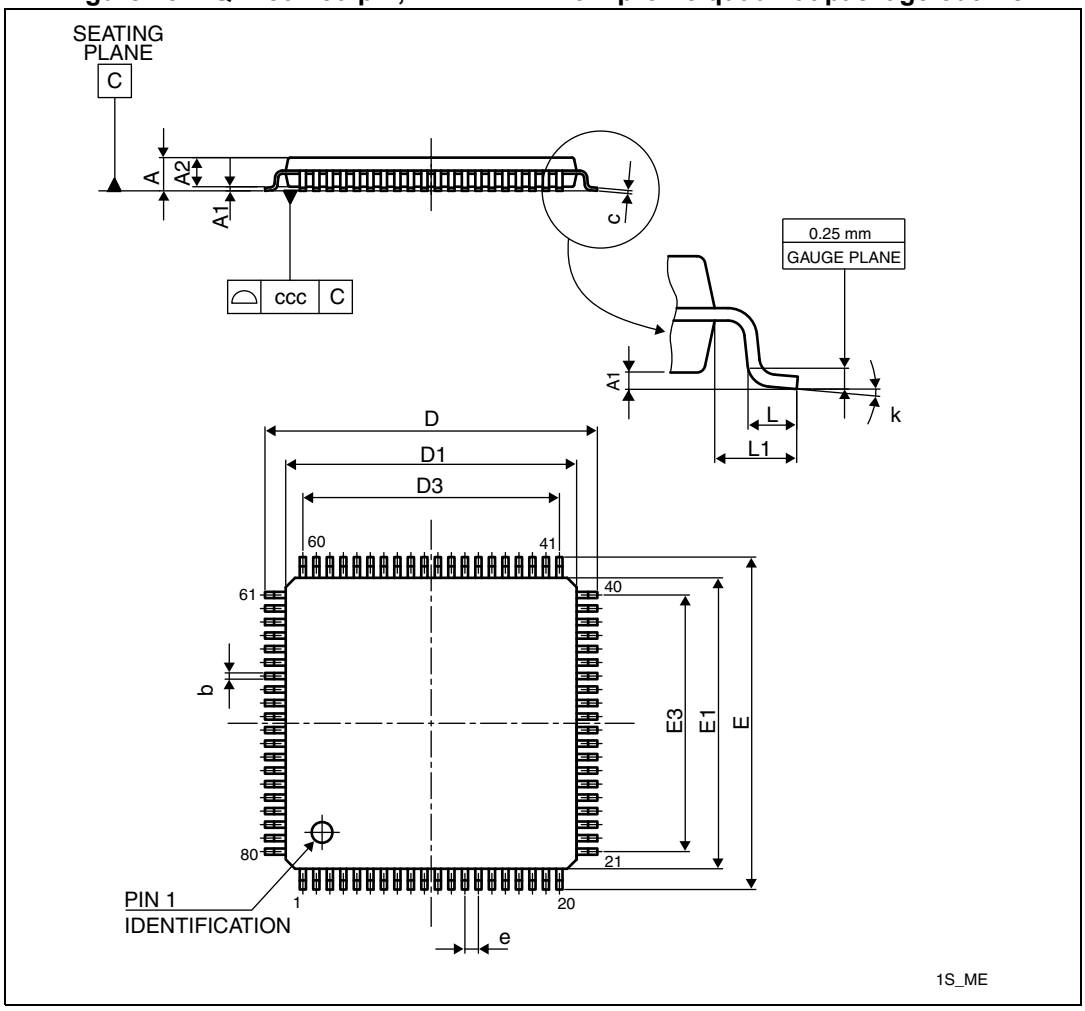
1. $f_{MASTER}$, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

# 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

## 11.1 LQFP80 package information

**Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline**



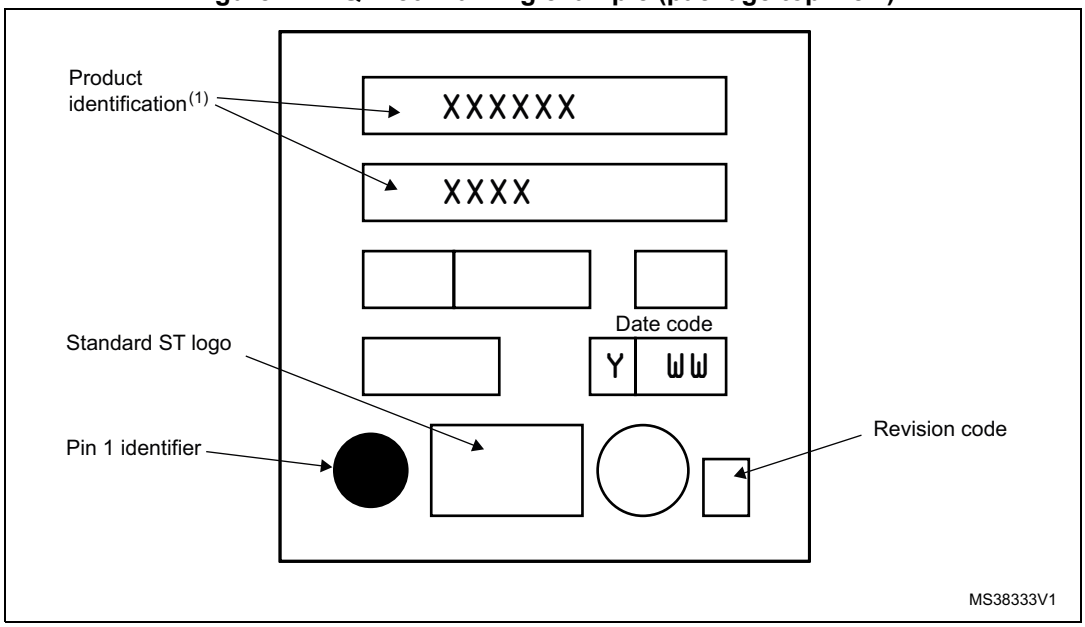

1. Drawing is not to scale.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 47. LQFP80 marking example (package top view)**



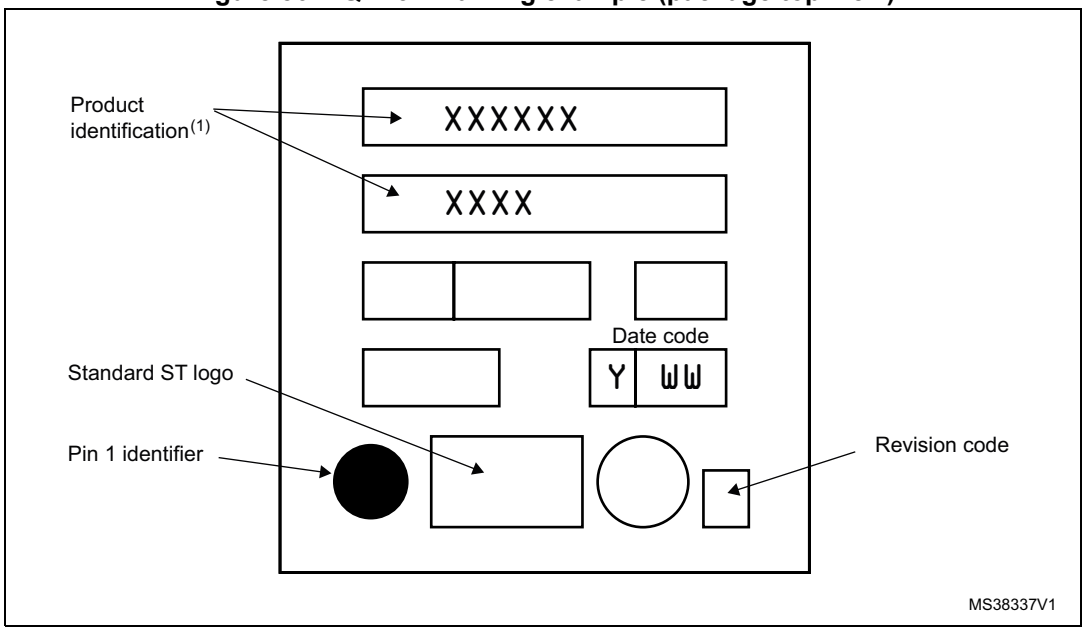

1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 56. LQFP32 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

### 11.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1 on page 111*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2)
- $I_{DDmax}$ = 8 mA
- $V_{DD}$ = 5 V
- maximum 20 I/Os used at the same time in output at low-level with $I_{OL}$ = 8 mA
- $V_{OL}$ = 0.4 V

$P_{INTmax}$ = 8 mA x 5 V = 400 mW

$P_{IOmax}$ = 20 x 8 mA x 0.4 V = 64 mW

This gives:

$P_{INTmax}$ = 400 mW and $P_{IOmax}$ 64 mW

$P_{Dmax}$ = 400 mW + 64 mW

Thus:

$P_{Dmax}$ = 464 mW.

Using the values obtained in *Table 54: Thermal characteristics* $T_{Jmax}$ is calculated as follows:

For LQFP64 46 °C/W

$$T_{jmax} = 82\ °C + (46\ °C/W \times 464\ mW) = 82\ °C + 21\ °C = 103\ °C$$

This is within the range of the suffix C version parts (-40 °C < $T_j$ < 125 ° C).

Parts must be ordered at least with the temperature range suffix C.

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 22-Aug-2008 | 2 (continued) | *Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers.<br>*Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL)<br>*Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU).<br>*Table 23: Operating lifetime:* Amended footnotes.<br>*Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'.<br>*Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes.<br>*Table 28: Oscillator current consumption*: Replaced.<br>*Table 29: Programming current consumption*: Amended maximum data and footnotes.<br>*Table 21: Current characteristics*: Replaced.<br>*Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes.<br>*Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes.<br>*Figure 13* to *Figure 18*: info on peripheral activity added.<br>*Table 33: HSI oscillator characteristics*: Modified $f_{HSE\_ext}$ data and added $V_{HSEdhl}$ data.<br>*Table 35: Flash program memory/data EEPROM memory*: Removed $ACC_{HSI}$ parameters and replaced with $ACC_{HS}$ parameters; amended data and footnotes.<br>Amended data of '*RAM and hardware registers*' table.<br>*Table 37: Data memory*: Updated names and data of $N_{RW}$ and $t_{RET}$ parameters.<br>*Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added $V_{OH}$ and $V_{OL}$ parameters; Updated $I_{lkg\ ana}$ parameter.<br>Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*.<br>*Table 46: EMI data*: Updated $f_{ADC}$, $t_S$, and $t_{CONV}$ data.<br>*Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters.<br>*Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2.<br>*Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for $T_A$ = 145 °C.<br>*Figure 53*: Updated memory size, pin count and package type information. |

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 18-Jul-2012 | 9 (continued) | *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* updated conditions for $I_{DD(RUN)}$.<br>*Table 38: I/O static characteristics:* added new condition and new max values for rise and fall time; updated footnote 2.<br>*Section 10.3.7: Reset pin characteristics:* updated text below *Figure 38: Typical NRST pull-up current Ipu vs VDD*<br>*Figure 39: Recommended reset pin protection:* updated unit of capacitor.<br>*Table 41: SPI characteristics:* updated SCK high and low time conditions and values.<br>*Figure 42: SPI timing diagram - master mode:* replaced 'SCK input' signals with 'SCK output' signals.<br>Updated *Table 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data*<br>Replaced *Figure 48: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*<br>Added *Figure 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint* *and* *Figure 55: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint*<br>Updated *Figure 57: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline*<br>Updated *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*<br>*Section 13.2.2: C and assembly toolchains:* added www.iar.com. |
| 31-Mar-2014 | 10 | Updated:<br>– *Table 1: Device summary*,<br>– *Table: STM8AF52xx product line-up with CAN*,<br>– *Table: STM8AF/H/P51xx product line-up with CAN*,<br>– *Table: STM8AF/H/P61xx product line-up without CAN*,<br>– *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description*,<br>– The maximum speed in *Section 5.9.3: Serial peripheral interface (SPI)*,<br>– $t_{TEMP}$ Reset release delay /VDD rising typical and max values in *Table 25: Operating conditions at power-up/power-down*,<br>– The symbol $t_{IFP(NRST)}$ with $t_{INFP(NRST)}$ in *Table 39: NRST pin characteristics*,<br>– The address and comment for Reset in *Table 17: STM8A interrupt table*. |

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 31-Mar-2014 | 10 (continued) | Added:<br>– *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout;*<br>– the caution in *Section 5.10: Input/output specifications,*<br>– The table footnote “Not recommended for new designs” to *Table: STM8AF/H/P51xx product line-up with CAN* and *Table: STM8AF/H/P61xx product line-up without CAN.*<br>– The figure footnotes to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* and *Figure: VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)* |
| 13-Jun-2014 | 11 | Added STM8AF52A6 part number. |
| 09-Jun-2015 | 12 | Added:<br>– the third table footnote to *Table 25: Operating conditions at power-up/power-down*,<br>– *Figure 47: LQFP80 marking example (package top view)*,<br>– *Figure 50: LQFP64 marking example (package top view)*,<br>– *Figure 53: LQFP48 marking example (package top view)*,<br>– *Figure 56: LQFP32 marking example (package top view)*,<br>– *Figure 59: VFQFPN32 marking example (package top view)*,<br>– the footnote about the device marking to *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*.<br>Removed STM8AF51xx and STM8AF61xx obsolete root part numbers, and consequently “H” products:<br>– *Table 1: Device summary*,<br>– *Section 1: Introduction*,<br>– *Section 2: Description*,<br>– *Section 3: Product line-up*,<br>– *Table 12: Memory model 128K*,<br>– *Section 10.3: Operating conditions*,<br>– *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*.<br>Moved *Section 11.6: Thermal characteristics* to *Section 11: Package information*.<br>Updated:<br>– the product naming in the document headers and captions,<br>– the standard reference for EMI characteristics in *Table 46: EMI data*. |
| 13-Jun-2016 | 13 | Updated *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data* |