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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6289tay

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1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

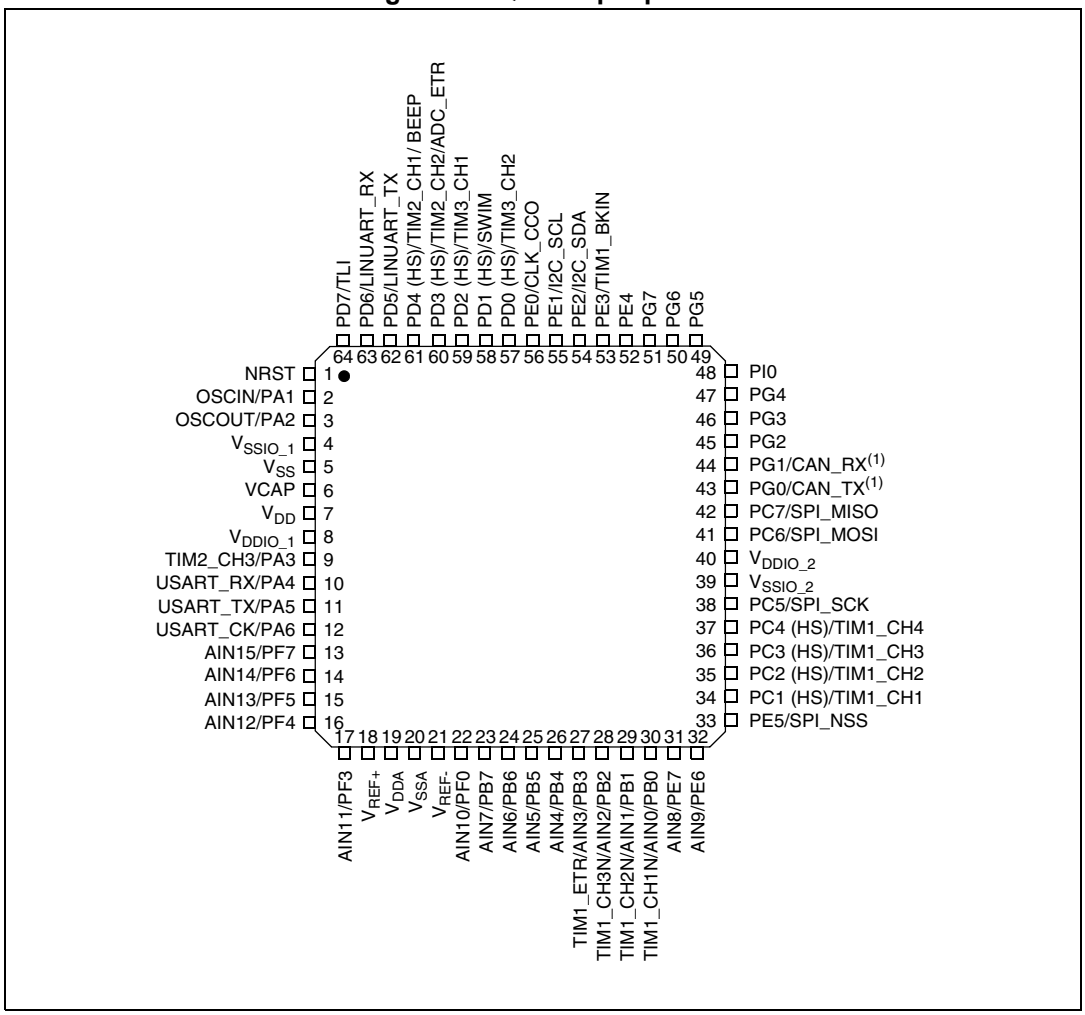
Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
  - Mask mode permitting ID range filtering
  - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

Figure 4. LQFP 64-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC positive reference voltage		-
23	19	13	9	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
24	20	14	10	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
25	21	-	-	-	V_{REF-}	S	-	-	-	-	-	-	-	ADC negative reference voltage		-
26	22	-	-	-	PF0/AIN10	I/O	**X**	X	-	-	O1	X	X	**Port F0**	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X	-	-	O1	X	X	**Port H4**	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X	-	-	O1	X	X	**Port H5**	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X	-	-	O1	X	X	**Port H6**	Timer 1 - inverted channel 2	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
78	62	46	30	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-
79	63	47	31	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
80	64	48	32	32	PD7/TLI(5)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. SPI and USTART are not available in STM8AF5286UC, refer to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* for the pin names.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to V_{DD} are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after reset release.
5. If this pin is configured as interrupt pin, it will trigger the TLI.

9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 18: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be changed in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 18. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
0x00 4801	User boot code (UBC)	OPT1	UBC[7:0]								0x00
0x00 4802		NOPT1	NUBC[7:0]								0xFF
0x00 4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x00 4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x00 4805	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	0x00
0x00 4806		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	0xFF
0x00 4807	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	0x00
0x00 4808		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	0xFF
0x00 4809	HSE clock startup	OPT5	HSECNT[7:0]								0x00
0x00 480A		NOPT5	NHSECNT[7:0]								0xFF

10.3.3 External clock sources and timing characteristics

HSE external clock

An HSE clock can be generated by feeding an external clock signal of up to 24 MHz to the OSCIN pin.

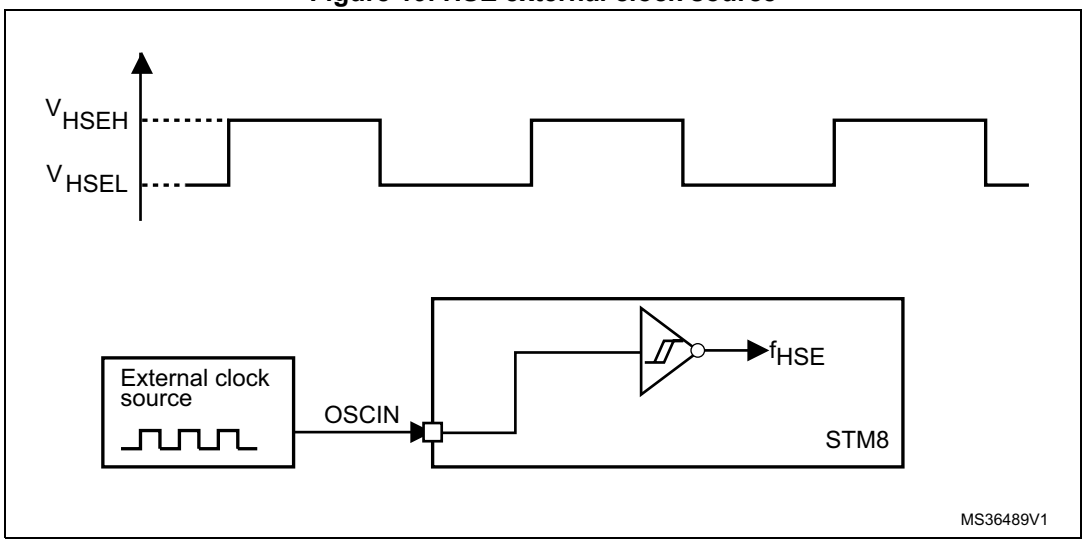
Clock characteristics are subject to general operating conditions for V_{DD} and T_A.

Table 31. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	T_A = -40 °C to 150 °C	0(1)	-	24	MHz
V_{HSEdHL}	Comparator hysteresis	-	0.1 x V_{DD}	-	-	V
V_{HSEH}	OSCIN high-level input pin voltage	-	0.7 x V_{DD}	-	V_{DD}	
V_{HSEL}	OSCIN low-level input pin voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. If CSS is used, the external clock must have a frequency above 500 kHz.

Figure 19. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 24 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

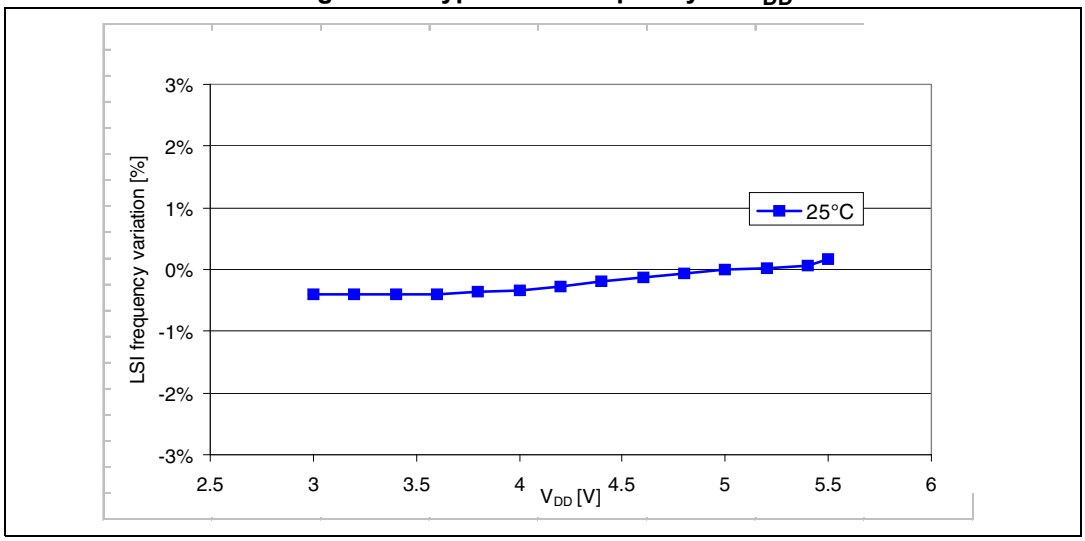


Figure 30. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

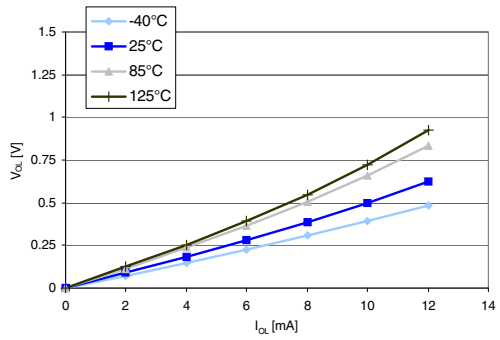


Figure 31. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

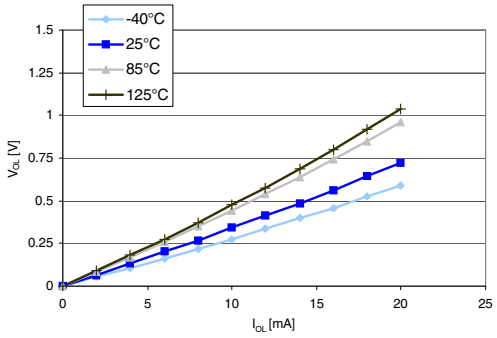


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

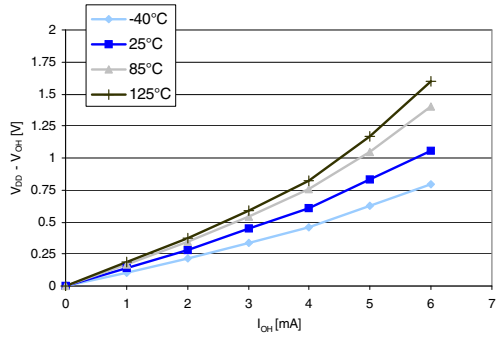


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

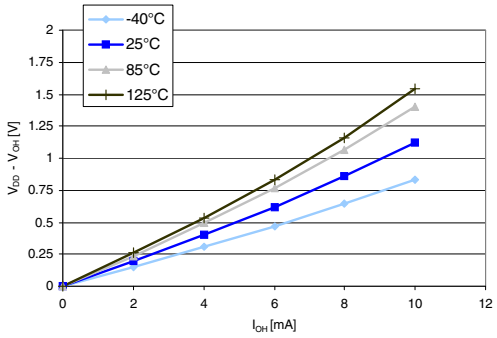


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

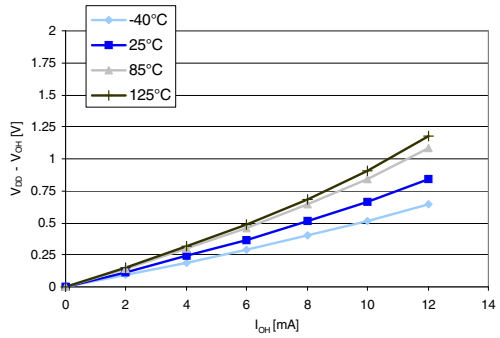
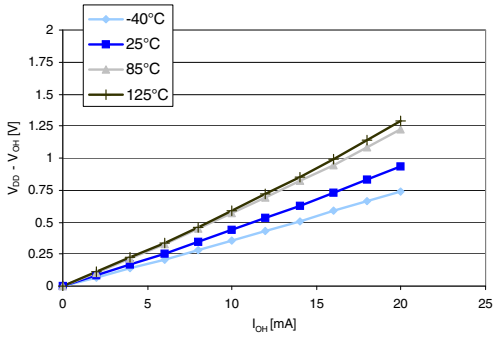


Figure 35. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST high-level input voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST low-level output voltage(1)	I_{OL} = 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Figure 36. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

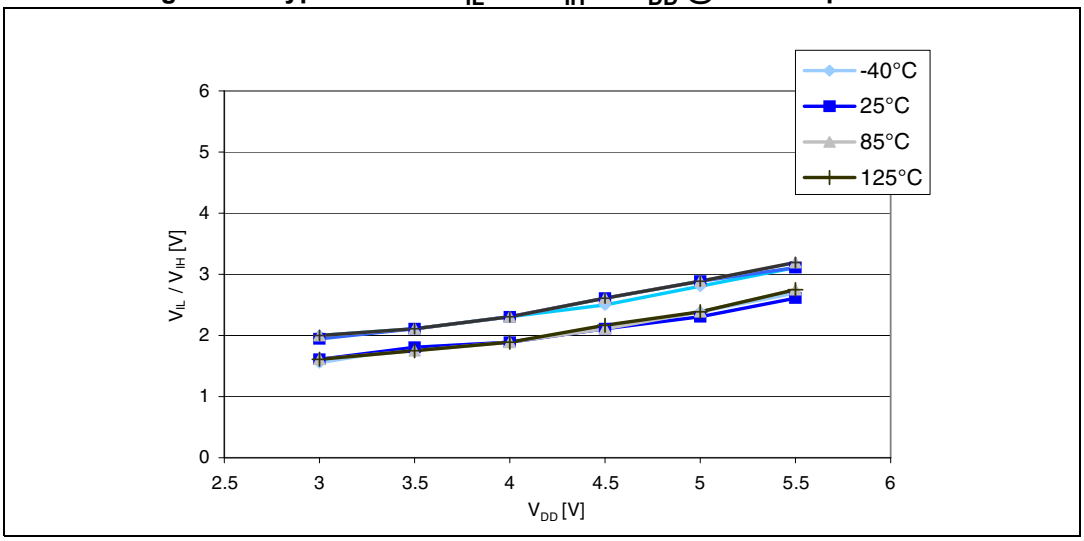
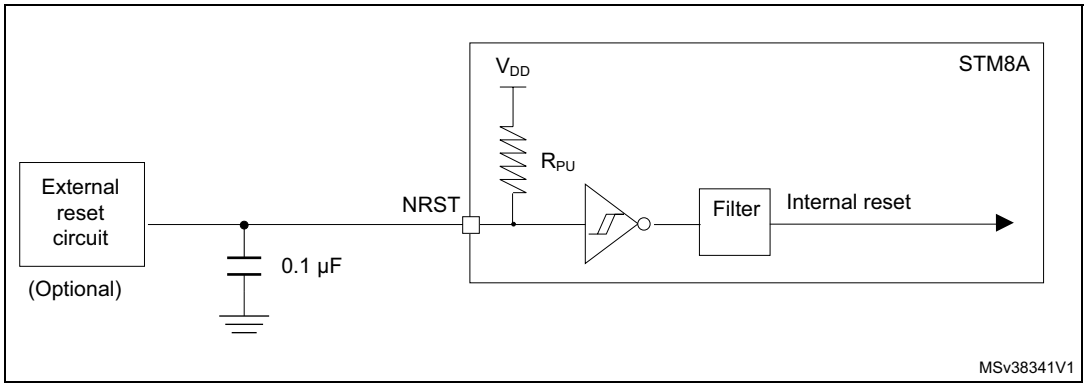


Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

1. Not tested in production.

10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

10.3.11 10-bit ADC characteristics

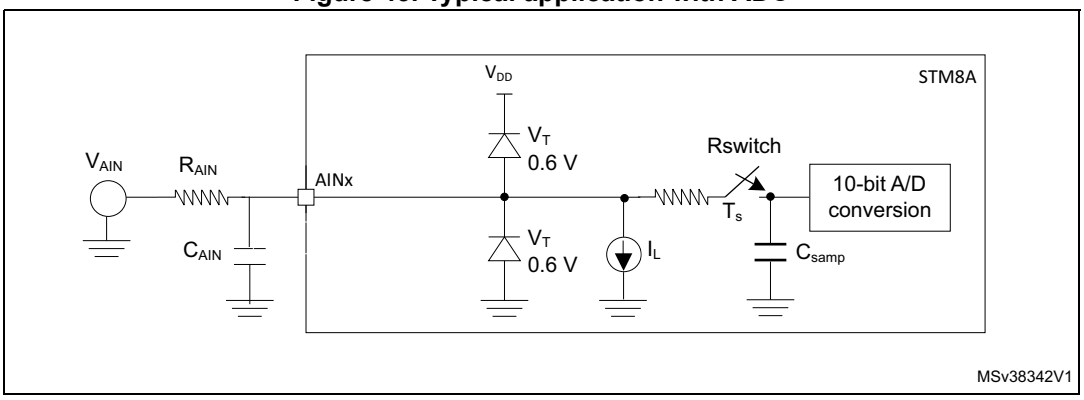
Subject to general operating conditions for V_{DDA}, f_{MASTER} and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 43. Typical application with ADC



1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

1. Guaranteed by characterization results, not tested in production

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

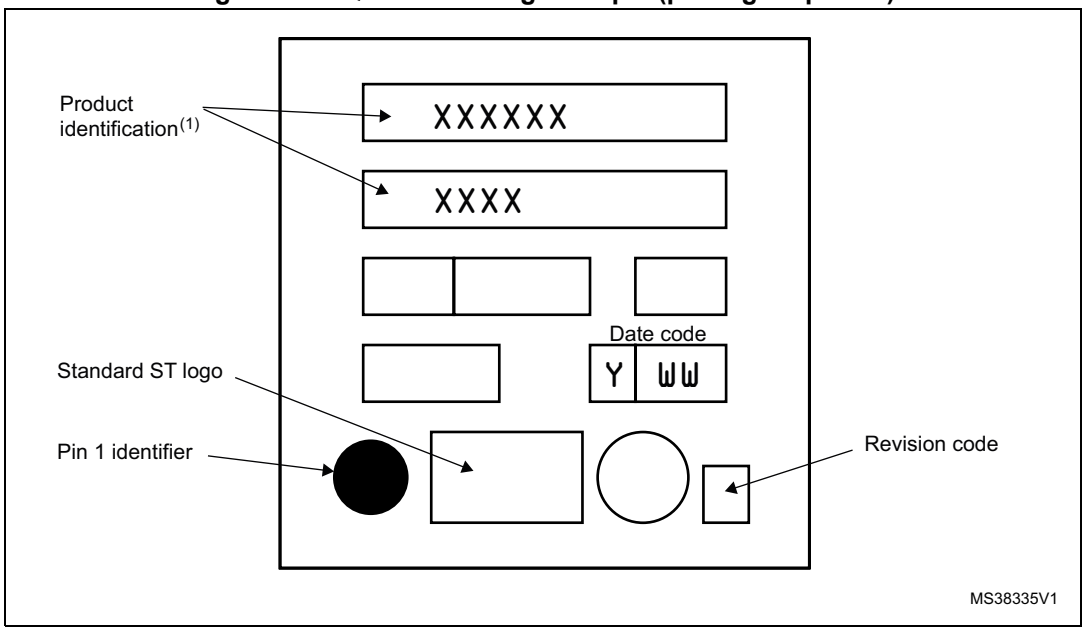
This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

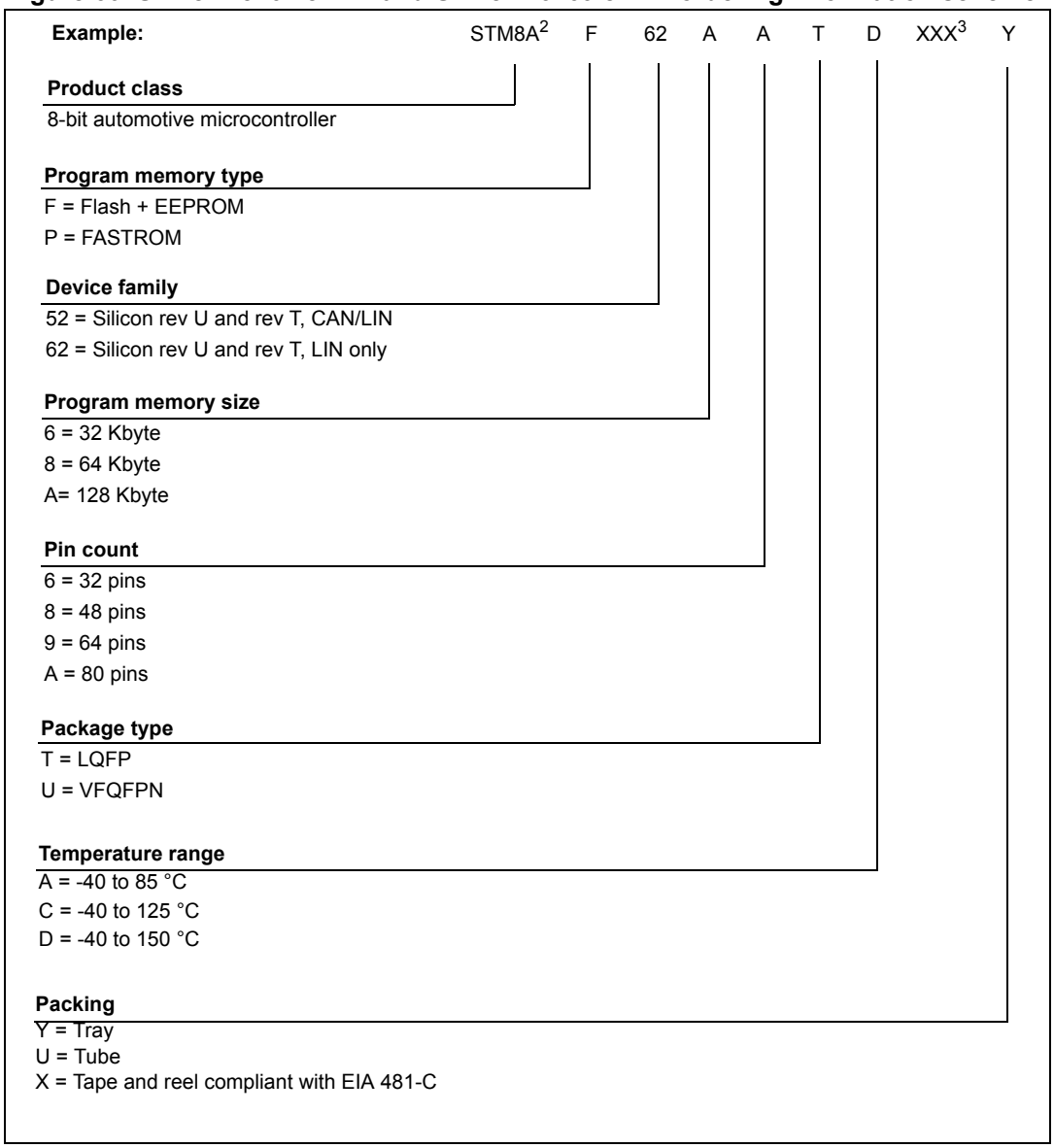
Figure 53. LQFP48 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

12 Ordering information

Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme[1]



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

Table 55. Document revision history (continued)

Date	Revision	Changes
13-Apr-2010	6	Updated title on cover page. Modified cover page header to clarify the part numbers covered by the datasheets. Updated footnote on *Table 1: Device summary* to add 'P' order codes. Changed definition of 'P' order codes. 'Q' order codes (FASTROM and EEPROM) removed. Reorganized the content of *Section 5: Product overview*. *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description* updated PD7/TLI alternate function, removed caution note for PD6/ LINUART_RX, and added note to PA1/OSCIN. Renamed *Section 7: Memory and register map*, and merged content with *Section: Register map*. Updated *Figure 8: Register and memory map*. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table 18: Option bytes*. Updated AFR4 definition in *Table 19: Option byte description*. Added C_{EXT} in *Table 24: General operating conditions*, and *Section 10.3.1: VCAP external capacitor*. Updated t_{VDD} in *Table 25: Operating conditions at power-up/power-down*. Moved *Table 30: Typical peripheral current consumption VDD = 5.0 V* to *Section : Current consumption for on-chip peripherals*. Removed $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*. Updated *Section 12: Ordering information* to the devices supported by the datasheet. Updated *Section 13: STM8 development tools*.
08-Jul-2010	7	Added STM8AF5168 and STM8AF518A part number in *Figure 4*, and STM8AF618A in *Figure 5*. Added STM8AF52xx, STM8AF6269, STM8AF628x, and STM8AF62Ax. Updated D temperature range to -40 to 150°C. Updated number of I/Os on cover page. Added *Table 23: Operating lifetime*. Restored $V_{ESD(MM)}$ from *Table 47: ESD absolute maximum ratings*. *Table 24: General operating conditions*: updated V_{CAP} information. ESL parameter, and range D maximum junction temperature (T_J). Added STM8AF52xx and STM8AF62xx, and footnote in *Section 12: Ordering information*. Updated *Section 13: STM8 development tools*: added *Table: Product evolution summary*, and split the beCAN time triggered communication mode limitation in two sections.