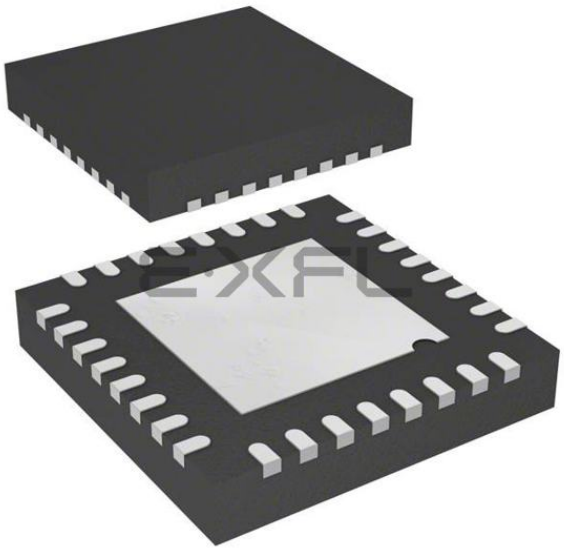

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a6ucx

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 4. Peripheral clock gating bits (CLK_PCKENR1)

Control bit	Peripheral
PCKEN17	TIM1
PCKEN16	TIM3
PCKEN15	TIM2
PCKEN14	TIM4
PCKEN13	LINUART
PCKEN12	USART
PCKEN11	SPI
PCKEN10	I^2C

Table 5. Peripheral clock gating bits (CLK_PCKENR2)

Control bit	Peripheral
PCKEN27	CAN
PCKEN26	Reserved
PCKEN25	Reserved
PCKEN24	Reserved
PCKEN23	ADC
PCKEN22	AWU
PCKEN21	Reserved
PCKEN20	Reserved

5.6 Low-power operating modes

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- Wait mode

  In this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.

- Active-halt mode with regulator on

  In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.

- Active-halt mode with regulator off

  This mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.

- Halt mode

  CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.5 Controller area network interface (beCAN)

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It is equipped with a receive FIFO and a very versatile filter bank. Together with a filter match index, this allows a very efficient message handling in today's car network architectures. The CPU is significantly unloaded. The maximum transmission speed is 1 Mbit/s.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request

Reception

- 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message for quick message association
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID.
- Filtering modes (mixable):
  - Mask mode permitting ID range filtering
  - ID list mode

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Table 12. Memory model 128K

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
128 K	0x00 27FFF	6 K	0x00 17FF	0x00 1400
64 K	0x00 17FFF			
32 K	0x00 0FFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 13. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 13. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX(1)
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX(1)
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX(1)
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

1. Depends on the external circuitry.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

Table 18. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 480B	TMU	OPT6	TMU[3:0]								0x00
0x00 480C		NOPT6	NTMU[3:0]								0xFF
0x00 480D	Flash wait states	OPT7	Reserved							WAIT STATE	0x00
0x00 480E		NOPT7	Reserved							NWAIT STATE	0xFF
0x00 480F	Reserved										
0x00 4810	TMU	OPT8	TMU_KEY 1 [7:0]								0x00
0x00 4811		OPT9	TMU_KEY 2 [7:0]								0x00
0x00 4812		OPT10	TMU_KEY 3 [7:0]								0x00
0x00 4813		OPT11	TMU_KEY 4 [7:0]								0x00
0x00 4814		OPT12	TMU_KEY 5 [7:0]								0x00
0x00 4815		OPT13	TMU_KEY 6 [7:0]								0x00
0x00 4816		OPT14	TMU_KEY 7 [7:0]								0x00
0x00 4817		OPT15	TMU_KEY 8 [7:0]								0x00
0x00 4818		OPT16	TMU_MAXATT [7:0]								0xC7
0x00 4819 to 487D	Reserved										
0x00 487E	Boot-loader(1)	OPT17	BL [7:0]								0x00
0x00 487F		NOPT 17	NBL [7:0]								0xFF

1. This option consists of two bytes that must have a complementary value in order to be valid. If the option is invalid, it has no effect on EMC reset.

Table 19. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN: Low speed internal clock enable** 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on Halt 0: No reset generated on Halt if WWDG active 1: Reset generated on Halt if WWDG active
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of 0xE1, 0xD2, 0xB4, and 0x00.
OPT6	**TMU**[3:0]: Enable temporary memory unprotection 0101: TMU disabled (permanent ROP). Any other value: TMU enabled.
OPT7	**WAIT STATE: Wait state configuration** This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 0: No wait state 1: One wait state
OPT8	**TMU_KEY 1 [7:0]: Temporary unprotection key 0** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT9	**TMU_KEY 2 [7:0]: Temporary unprotection key 1** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT10	**TMU_KEY 3 [7:0]: Temporary unprotection key 2** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT11	**TMU_KEY 4 [7:0]: Temporary unprotection key 3** Temporary unprotection key: Must be different from 0x00 or 0xFF

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

Figure 9. Pin loading conditions

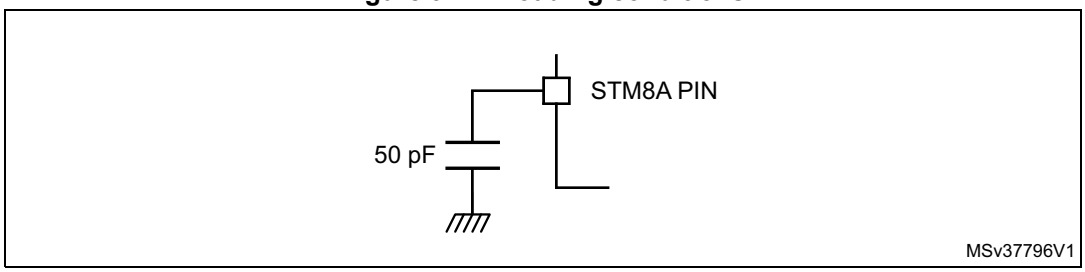


Table 25. Operating conditions at power-up/power-down

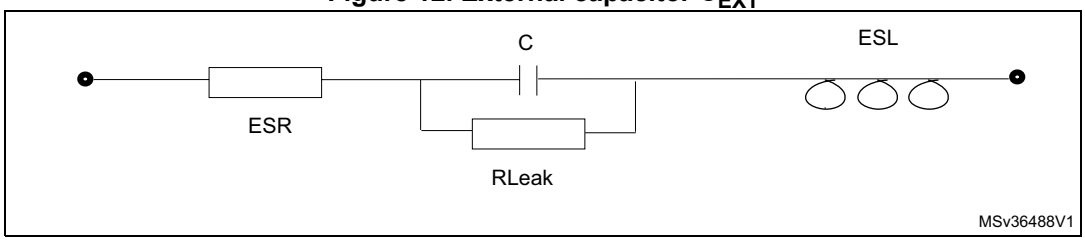
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	1.7	ms
	Reset generation delay	V_{DD} falling	-	3	-	µs
V_{IT+}	Power-on reset threshold(2) (3)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70(1)	-	mV

1. Guaranteed by design, not tested in production.
2. If V_{DD} is below 3 V, the code execution is guaranteed above the V_{IT-} and V_{IT+} thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1 µF requires Q=1 µF x 1.8 V = 1.8 µC.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 24*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 59* and *Figure 10 on page 60*.

If not explicitly stated, general conditions of temperature and voltage apply.

Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 °C to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 24 MHz 1 ws	8.7	16.8(2)	mA
			f_{CPU} = 16 MHz	7.4	14	
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	f_{CPU} = 24 MHz	4.4	6.0(2)	
			f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 24 MHz	2.4	3.1(2)	
			f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

Current consumption curves

Figure 13 to *Figure 18* show typical current consumption measured with code executing in RAM.

Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @f_{CPU} = 16 MHz, peripherals = on

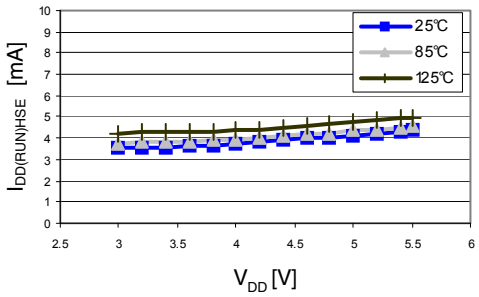


Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

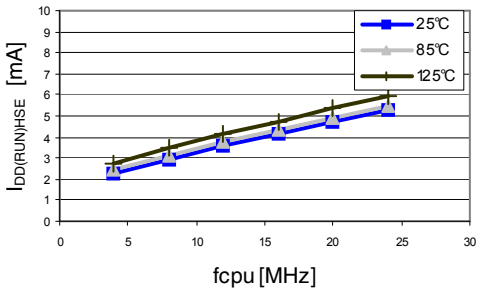


Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off

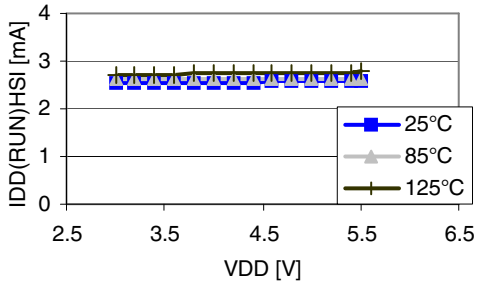


Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = on

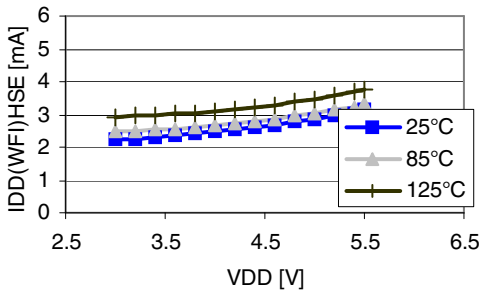


Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripherals = on

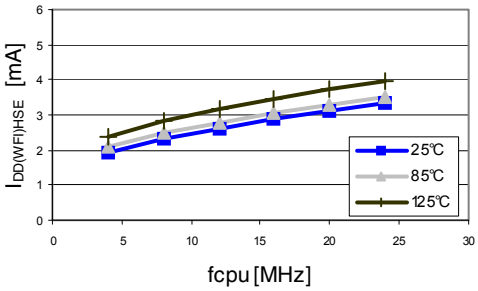


Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripherals = off

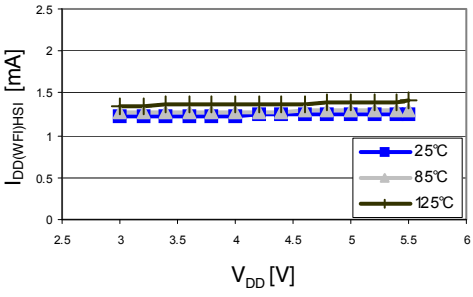
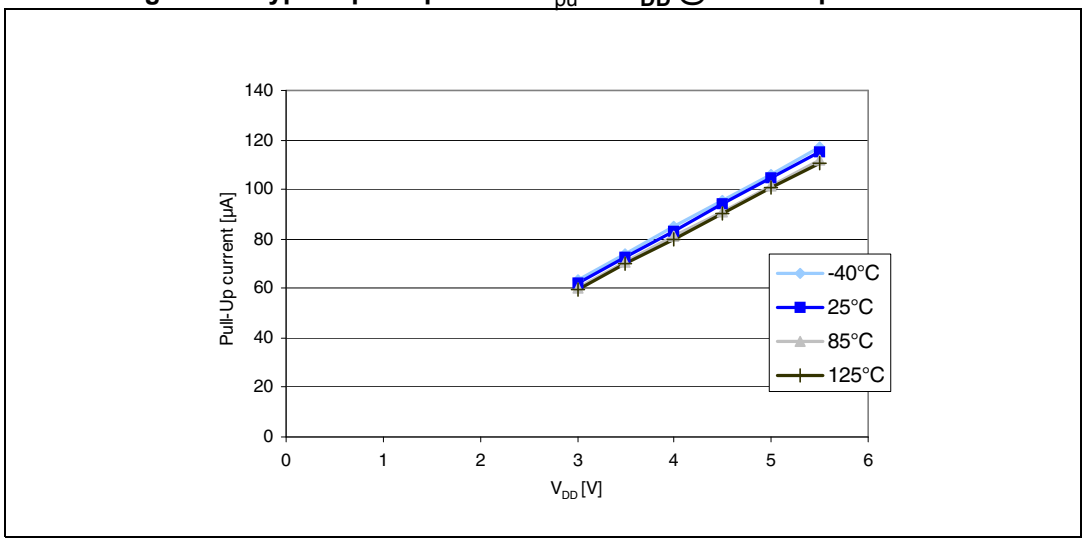


Figure 25. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures(1)



1. The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 26 to *Figure 35* show typical output level curves measured with output on a single pin.

Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

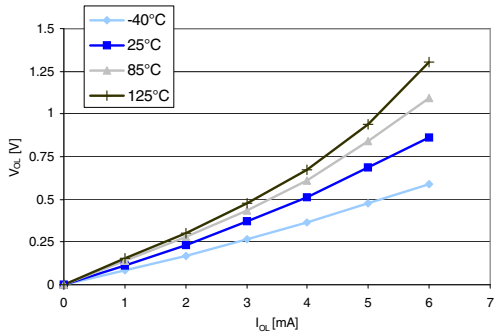


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

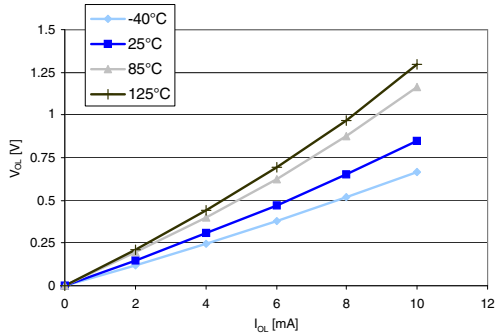


Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

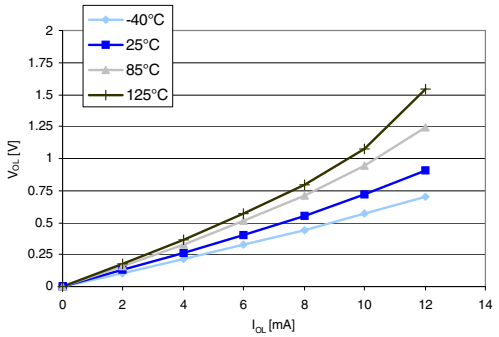
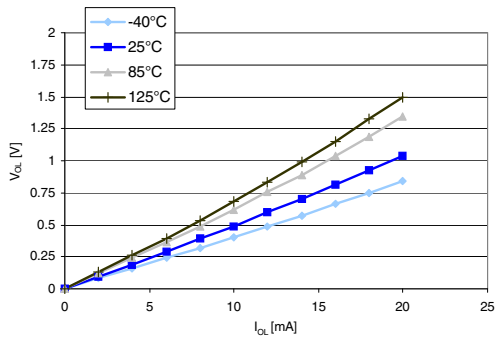


Figure 29. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)



Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

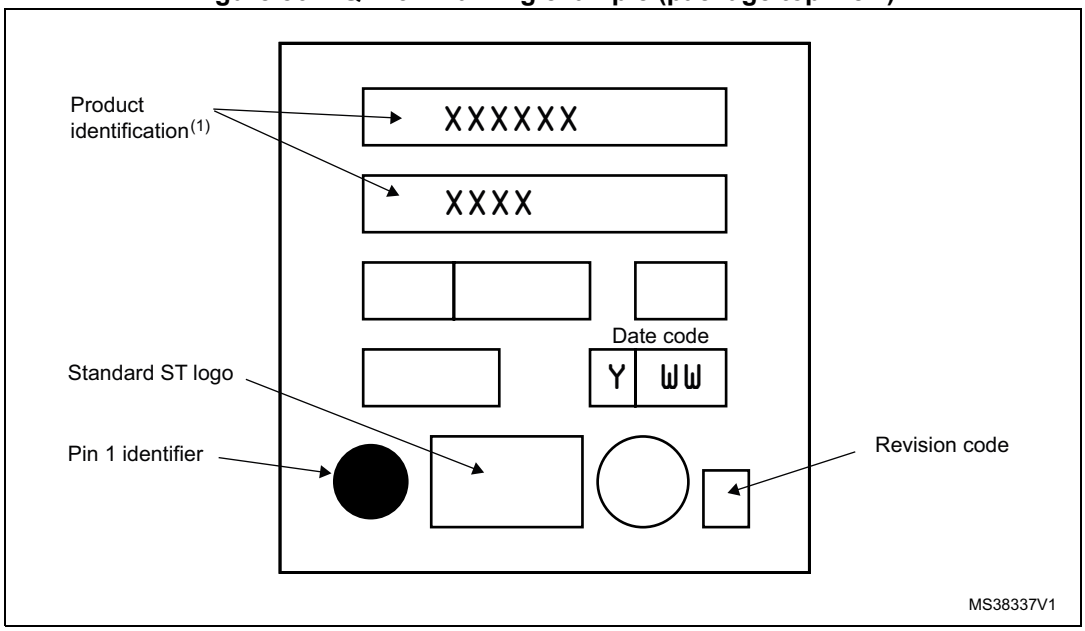
1. Guaranteed by characterization results, not tested in production

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

13 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

13.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

13.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high-speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

Table 55. Document revision history (continued)

Date	Revision	Changes
31-Mar-2014	10 (continued)	Added: – *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout;* – the caution in *Section 5.10: Input/output specifications,* – The table footnote “Not recommended for new designs” to *Table: STM8AF/H/P51xx product line-up with CAN* and *Table: STM8AF/H/P61xx product line-up without CAN.* – The figure footnotes to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* and *Figure: VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)*
13-Jun-2014	11	Added STM8AF52A6 part number.
09-Jun-2015	12	Added: – the third table footnote to *Table 25: Operating conditions at power-up/power-down*, – *Figure 47: LQFP80 marking example (package top view)*, – *Figure 50: LQFP64 marking example (package top view)*, – *Figure 53: LQFP48 marking example (package top view)*, – *Figure 56: LQFP32 marking example (package top view)*, – *Figure 59: VFQFPN32 marking example (package top view)*, – the footnote about the device marking to *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Removed STM8AF51xx and STM8AF61xx obsolete root part numbers, and consequently “H” products: – *Table 1: Device summary*, – *Section 1: Introduction*, – *Section 2: Description*, – *Section 3: Product line-up*, – *Table 12: Memory model 128K*, – *Section 10.3: Operating conditions*, – *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Moved *Section 11.6: Thermal characteristics* to *Section 11: Package information*. Updated: – the product naming in the document headers and captions, – the standard reference for EMI characteristics in *Table 46: EMI data*.
13-Jun-2016	13	Updated *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data*