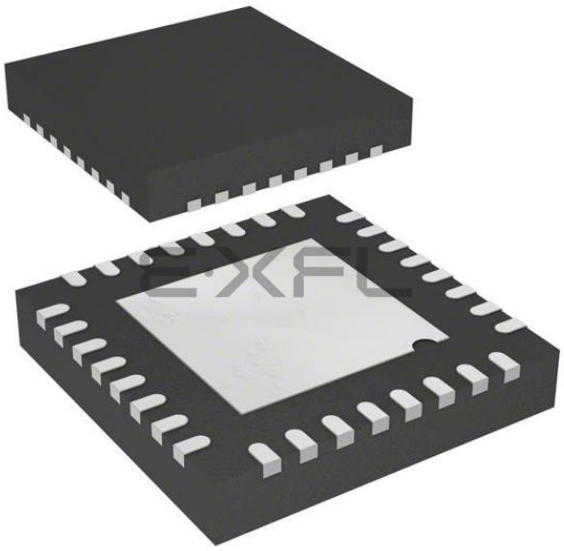

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a6ucy

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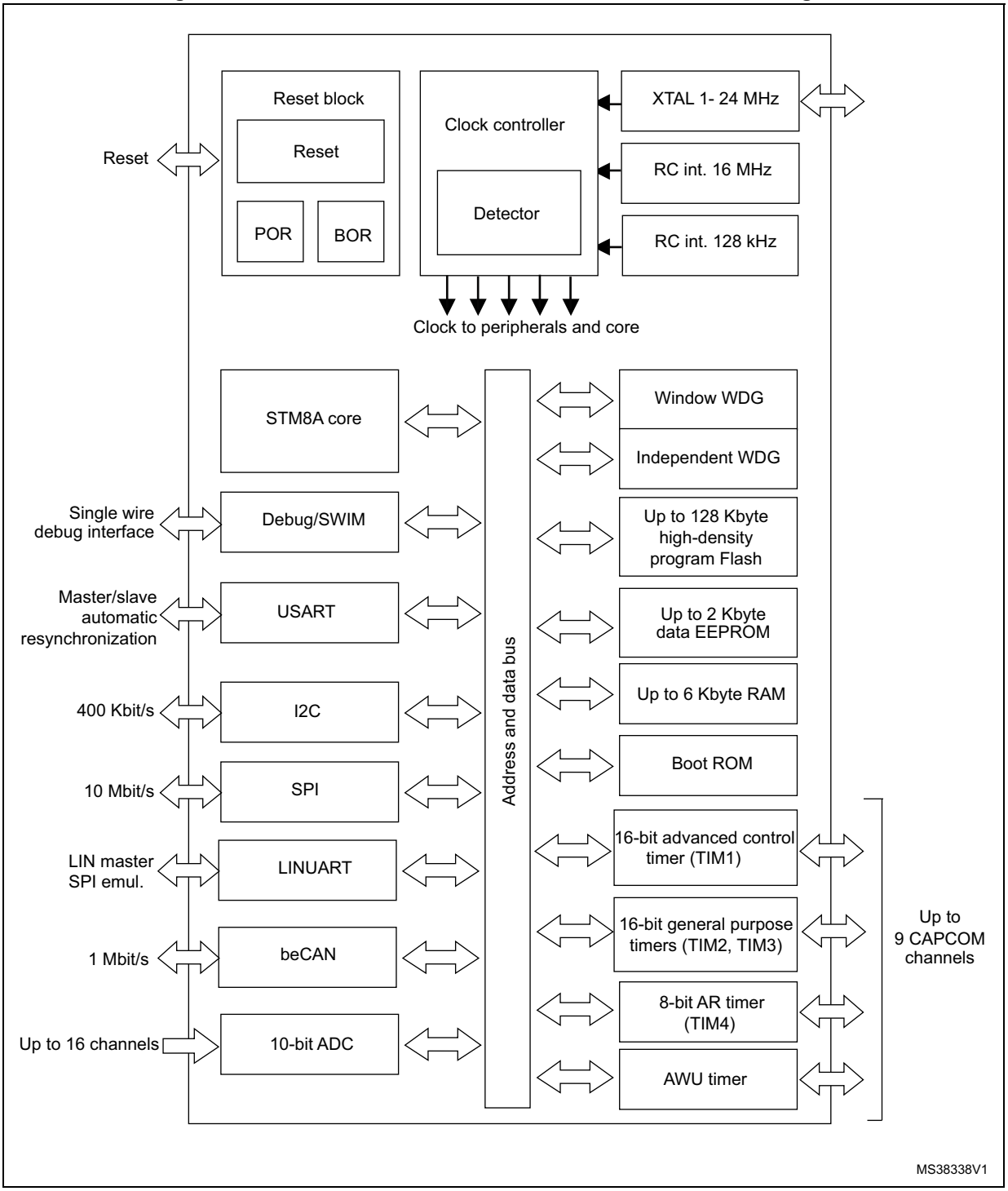
4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5.2 Single wire interface module (SWIM) and debug module (DM)

5.2.1 SWIM

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 bytes/ms.

5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-flavored emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 24 interrupt vectors with hardware priority
- Five vectors for external interrupts (up to 37 depending on the package)
- Trap and reset interrupts

5.4 Flash program and data EEPROM

- 32 Kbytes to 128 Kbytes of high density single voltage Flash program memory
- Up to 2 Kbytes true (not emulated) data EEPROM
- Read while write: writing in the data memory is possible while executing code in the Flash program memory.

The whole Flash program memory and data EEPROM are factory programmed with 0x00.

5.4.1 Architecture

- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 4. Peripheral clock gating bits (CLK_PCKENR1)

Control bit	Peripheral
PCKEN17	TIM1
PCKEN16	TIM3
PCKEN15	TIM2
PCKEN14	TIM4
PCKEN13	LINUART
PCKEN12	USART
PCKEN11	SPI
PCKEN10	I^2C

5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see *Table 8*).

Table 8. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC2

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 9*).

Table 9. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
USART	UART1
LINUART	UART3

5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X	-	-	O1	X	X	**Port H7**	Timer 1 - inverted channel 2	-
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	-	-	O1	X	X	**Port E7**	Analog input 8	-
40	32	24			PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E6**	Analog input 9	-
41	33	25	17	17	PE5/SPI_NSS(2)	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/ slave select	-
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X	-	O1	X	X	**Port C0**	ADC trigger input	-
43	34	26	18	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
44	35	27	19	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
45	36	28	20	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
46	37	29	21	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
47	38	30	22	22	PC5/SPI_SCK(2)	I/O	**X**	X	X	-	O3	X	X	**Port C5**	SPI clock	-
48	39	31	-	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
49	40	32	-	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
50	41	33	23	-	PC6/SPI_MOSI (2)	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
51	42	34	24	-	PC7/SPI_MISO (2)	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
52	43	35	-	23	PG0/CAN_TX	I/O	**X**	X	-	-	O1	X	X	**Port G0**	CAN transmit	-
53	44	36	-	24	PG1/CAN_RX	I/O	**X**	X	-	-	O1	X	X	**Port G1**	CAN receive	-
54	45	-	-	-	PG2	I/O	**X**	X	-	-	O1	X	X	**Port G2**	-	-

Table 14. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x40
0x00 5060 to 0x005061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

Table 15. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only
2. Product dependent value, see *Figure 8: Register and memory map*.

Table 16. Temporary memory unprotection registers

Address	Block	Register label	Register name	Reset status
0x00 5800	TMU	TMU_K1	Temporary memory unprotection key register 1	0x00
0x00 5801		TMU_K2	Temporary memory unprotection key register 2	0x00
0x00 5802		TMU_K3	Temporary memory unprotection key register 3	0x00
0x00 5803		TMU_K4	Temporary memory unprotection key register 4	0x00
0x00 5804		TMU_K5	Temporary memory unprotection key register 5	0x00
0x00 5805		TMU_K6	Temporary memory unprotection key register 6	0x00
0x00 5806		TMU_K7	Temporary memory unprotection key register 7	0x00
0x00 5807		TMU_K8	Temporary memory unprotection key register 8	0x00
0x00 5808		TMU_CSR	Temporary memory unprotection control and status register	0x00

10.3 Operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	1 wait state T_A = -40 °C to 150 °C	16	24	MHz
		0 wait state T_A = -40 °C to 150 °C	0	16	
V_{DD}/V_{DDIO}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
T_A	Ambient temperature	Suffix A	- 40	85	°C
		Suffix C		125	
		Suffix D		150	
T_J	Junction temperature range	Suffix A	- 40	90	
		Suffix C		130	
		Suffix D		155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.

Figure 11. f_{CPUmax} versus V_{DD}

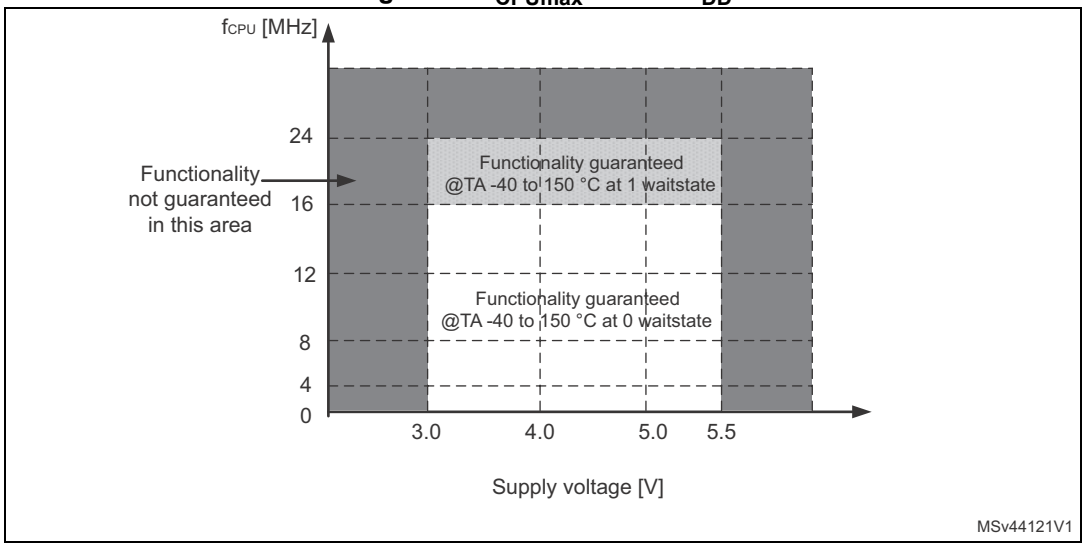
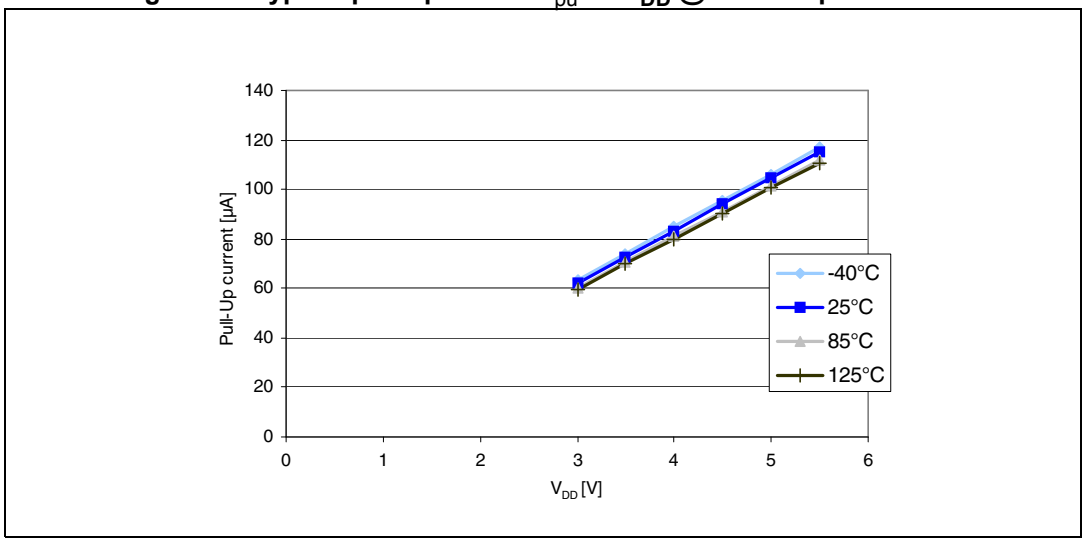


Figure 25. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures(1)



1. The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 26 to *Figure 35* show typical output level curves measured with output on a single pin.

Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

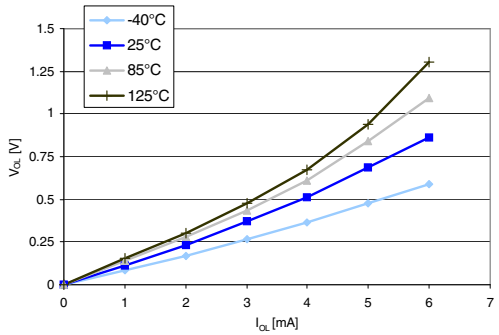


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

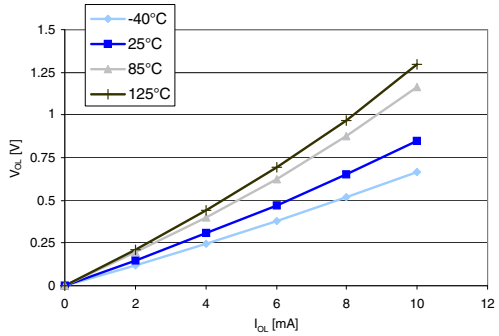


Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

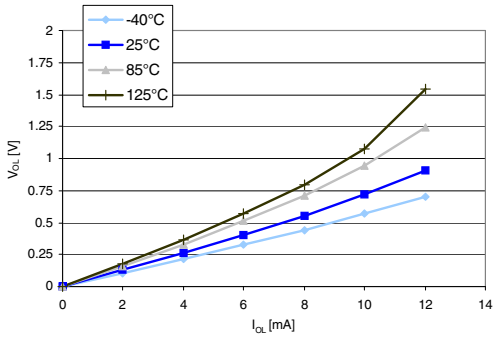


Figure 29. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

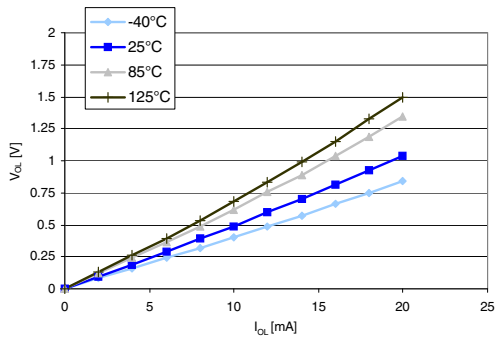


Figure 37. Typical NRST pull-up resistance R_{PU} vs V_{DD}

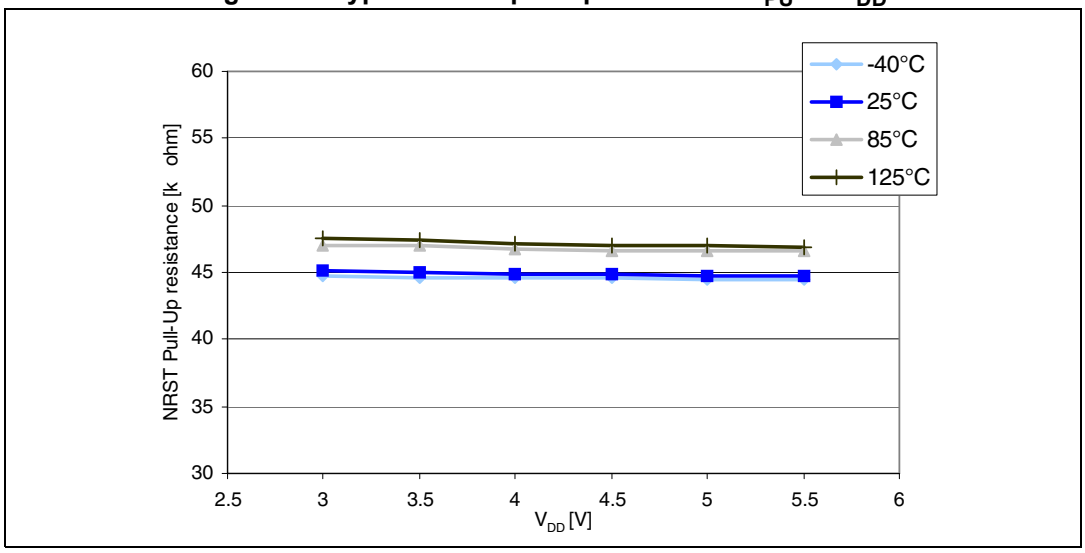
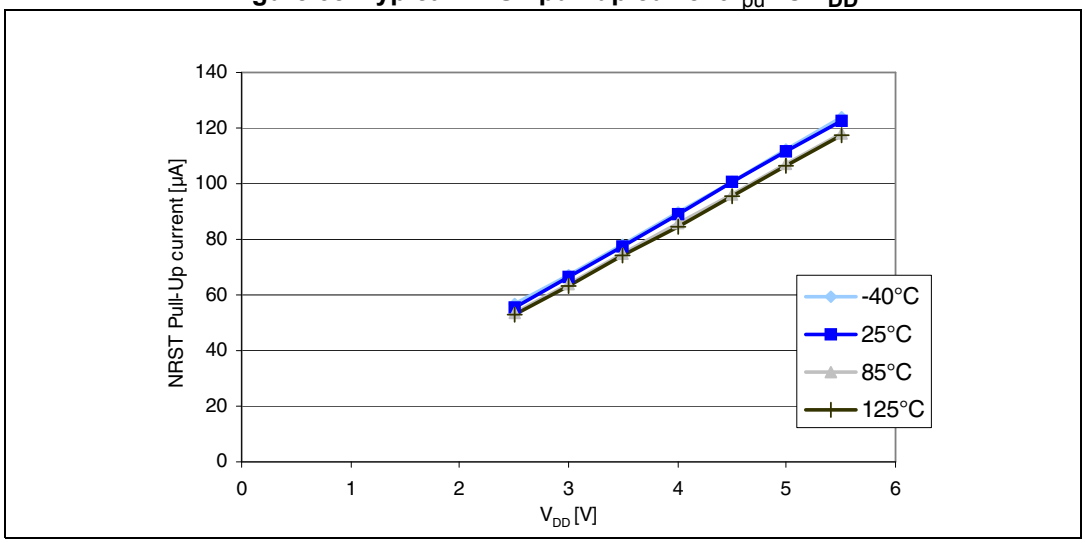


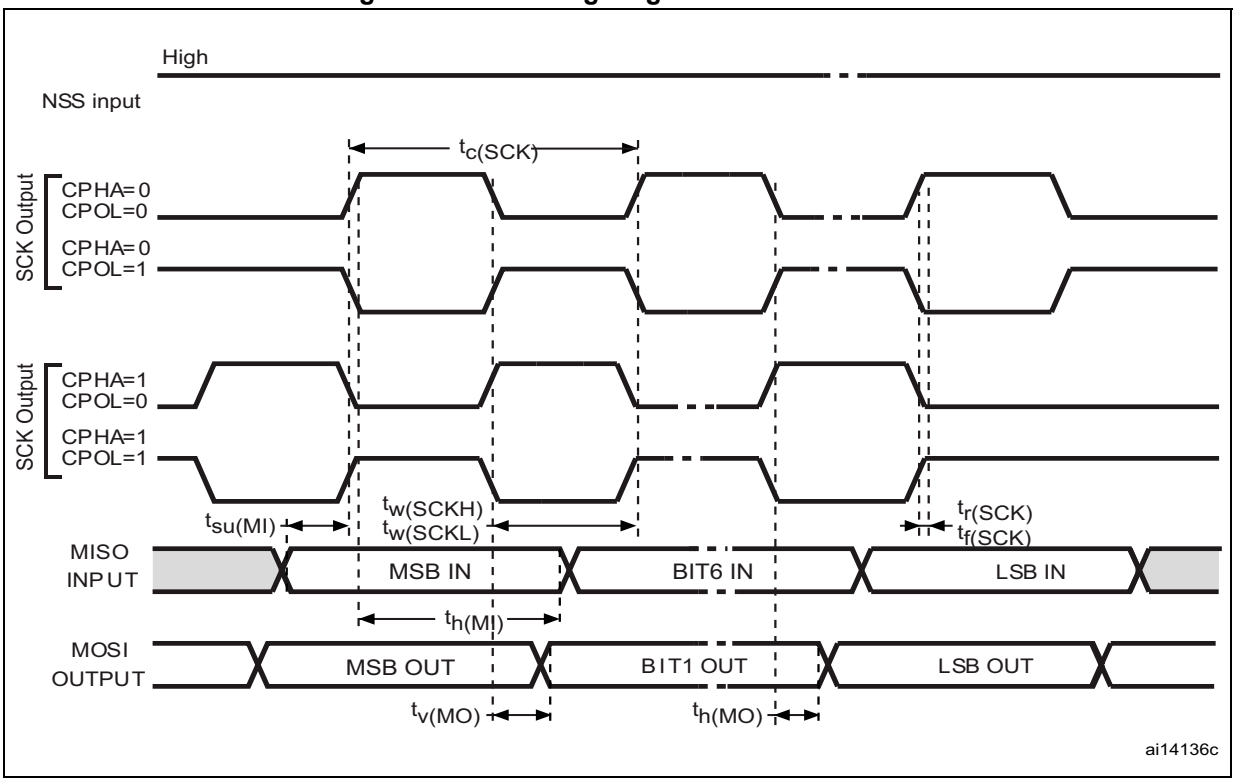
Figure 38. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 39* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 39: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 10 nF.

Figure 42. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	EMI level		-	2	2.5	2.5	

1. Guaranteed by characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-A115	B	200	

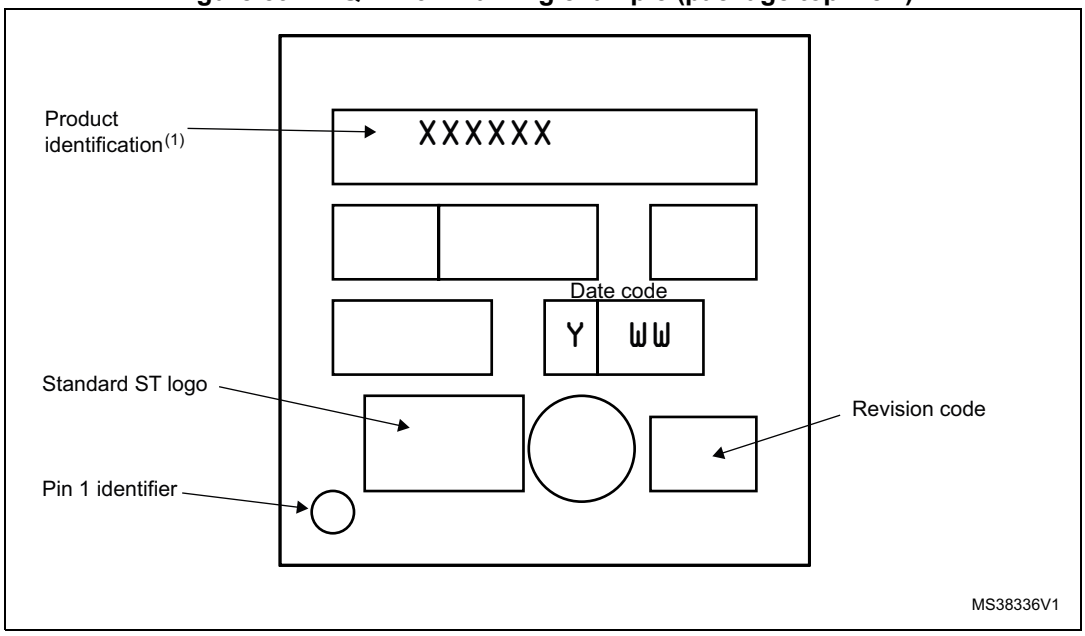
1. Guaranteed by characterization results, not tested in production

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. VFQFPN32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

11.6 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 24: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low- and high-level in the application.

Table 54. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	25	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

11.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1 on page 111*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2)
- I_{DDmax} = 8 mA
- V_{DD} = 5 V
- maximum 20 I/Os used at the same time in output at low-level with I_{OL} = 8 mA
- V_{OL} = 0.4 V

P_{INTmax} = 8 mA x 5 V = 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives:

P_{INTmax} = 400 mW and P_{IOmax} 64 mW

P_{Dmax} = 400 mW + 64 mW

Thus:

P_{Dmax} = 464 mW.

Using the values obtained in *Table 54: Thermal characteristics* T_{Jmax} is calculated as follows:

For LQFP64 46 °C/W

$$T_{jmax} = 82\ °C + (46\ °C/W \times 464\ mW) = 82\ °C + 21\ °C = 103\ °C$$

This is within the range of the suffix C version parts (-40 °C < T_j < 125 ° C).

Parts must be ordered at least with the temperature range suffix C.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 55. Document revision history (continued)

Date	Revision	Changes
16-Sep-2008	3	Replaced the salestype 'STM8H61xx' with 'STM8AH61xx on the first page. Added 'part numbers' to heading rows of *Table 1: Device summary*. Updated the 80-pin package silhouette on cover page in line with POA 0062342-revD. *Table 18*: Renamed 'TMU key registers 0-7 [7:0]' as 'TMU key registers 1-8 [7:0]' *Section 9*: Updated introductory text concerning option bytes which do not need to be saved in a complementary form. *Table 18*: Renamed the option bits 'TMU[0:3]', 'NTMU[0:3]', and 'TMU_KEY 0-7 [7:0]' as 'TMU[3:0]', 'NTMU[3:0]', and 'TMU_KEY 1-8 [7:0]' respectively. *Table 21*: Updated values of option byte 5 (HSECNT[7:0]); inverted the description of option byte 6 (TMU[3:0]); renamed option bytes 8 to 15 'TMU_KEY 0-7 [7:0]', as 'TMU_KEY 1-8 [7:0]'. Updated 80-pin package information in line with POA 0062342-revD in *Figure 45* and *Table 53*.
01-Jul-2009	4	Added 'STM8AH61xx' and 'STM8AH51xx to document header. Updated *: Features on page 1* (memories, timers, operating temperature, ADC and I/Os). Updated *Table 1: Device summary* Updated Kbyte value of program memory in *Section: Introduction* Changed the first two lines from the top in *Section: Description*. Updated *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram* Updated *Section 5: Product overview* In *Figure 5: LQFP 48-pin pinout*, added USART function to pins 10, 11, and 12; added CAN Tx and CAN Rx functions to pins 35 and 36 respectively. *Section 6: Pinouts and pin description:* deleted the text below the *Table 10: Legend/abbreviation for the pin description table* *Table 11: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description:* 68th, 69th pin (LQFP80): replaced X with a dash for PP output and Added a table footnote. Updated *Figure 8: Register and memory map*. *Table 12: Memory model 128K:* updated footnote Deleted the *Table: Stack and RAM partitioning* *Table 17: STM8A interrupt table*: Updated priorities 13, 15, 17, 20 and 24 and changed table footnote Updated *Section 7: Memory and register map* Updated *Table: Data memory, Table: I/O static characteristics,* and *Table 39: NRST pin characteristics*. *Section 10.1.1: Minimum and maximum values:* added ambient temperature T_A = -40 °C Updated *Table 20: Voltage characteristics*. Updated *Table 21: Current characteristics*. Updated *Table 22: Thermal characteristics*. Updated *Table 24: General operating conditions*.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of high density Flash program memory. Updated the number of I/Os for devices in 80-, 64-, and 48-pin packages in *Table: STM8AF52xx product line-up with CAN, Table: STM8AF62xx product line-up without CAN, Table: STM8AF/H/P51xx product line-up with CAN,* and *Table: STM8AF/H/P61xx product line-up without CAN.* Added TMU brief description in *Section 5.4: Flash program and data EEPROM*, updated TMU_MAXATT description in *Table 19: Option byte description*, and TMU_MAWATT reset value in *Table 18: Option bytes.* Updated clock sources in *Section 5.5.1: Features*. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)*. Added calibration using TIM3 in *Section 5.7.2: Auto-wakeup counter.* Added *Table 8: ADC naming* and *Table 9: Communication peripheral naming correspondence*. Updated SPI data rate to $f_{MASTER}/2$ in *Section 5.9.3: Serial peripheral interface (SPI)*. Added reset state in *Table 10: Legend/abbreviation for the pin description table.* *Table: STM8A microcontroller family pin description:* modified footnotes related to PD1/SWIM, corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. *Section: Register map:* Removed CAN register CLK_CANCCR. Removed I2C_PECR register. Added *footnote* for Px_IDR registers in *Table 13: I/O port hardware register map*. Updated register reset values for Px_IDR and PD_CR1 registers. Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, TMU, clock controller, interrupt controller, timers, communication interfaces, and ADC, by *TTable 14: General hardware register map.* Added debug module register map Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off, updated *Section 5.6: Low-power operating modes,* and *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated.* $I_{DD(FAH)}$ and $I_{DD(SAH)}$ renamed $I_{DD(AH)}$; $t_{WU(FAH)}$ and $t_{WU(SAH)}$ renamed $t_{WU(AH)}$.