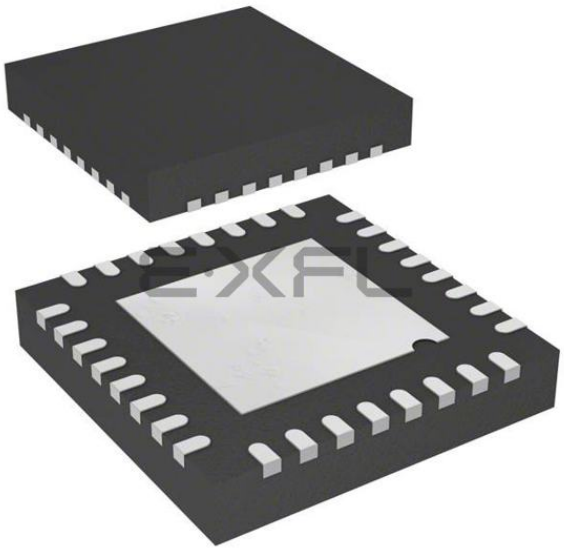

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a6udx

5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see *Table 8*).

Table 8. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC2

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 9*).

Table 9. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
USART	UART1
LINUART	UART3

5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

Table 10. Legend/abbreviation for the pin description table

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = high sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	2	2	2	PA1/OSCIN(1)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/ crystal in	-
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	4	4	-	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	5	5	4	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	6	6	5	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	7	7	6	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	8	7	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	10	10	-	-	PA4/USART_RX	I/O	**X**	X	X	-	O3	X	X	**Port A4**	USART receive	-
11	11	11	-	-	PA5/USART_TX	I/O	**X**	X	X	-	O3	X	X	**Port A5**	USART transmit	-
12	12	12	-	8	PA6/USART_CK (2)	I/O	**X**	X	X	-	O3	X	X	**Port A6**	USART synchro nous clock	-
13	-	-	-	-	PH0	I/O	X	X	-	HS	O3	X	X	**Port H0**	-	-
14	-	-	-	-	PH1	I/O	**X**	X	-	HS	O3	X	X	**Port H1**	-	-
15	-	-	-	-	PH2	I/O	**X**	X	-	-	O1	X	X	**Port H2**	-	-
16	-	-	-	-	PH3	I/O	**X**	X	-	-	O1	X	X	**Port H3**	-	-
17	13	-	-	-	PF7/AIN15	I/O	**X**	X	-	-	O1	X	X	**Port F7**	Analog input 15	-
18	14	-	-	-	PF6/AIN14	I/O	**X**	X	-	-	O1	X	X	**Port F6**	Analog input 14	-
19	15	-	-	-	PF5/AIN13	I/O	**X**	X	-	-	O1	X	X	**Port F5**	Analog input 13	-
20	16	-	8	-	PF4/AIN12	I/O	**X**	X	-	-	O1	X	X	**Port F4**	Analog input 12	-
21	17	-	-	-	PF3/AIN11	I/O	**X**	X	-	-	O1	X	X	**Port F3**	Analog input 11	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X	-	-	O1	X	X	**Port H7**	Timer 1 - inverted channel 2	-
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	-	-	O1	X	X	**Port E7**	Analog input 8	-
40	32	24			PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E6**	Analog input 9	-
41	33	25	17	17	PE5/SPI_NSS(2)	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/ slave select	-
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X	-	O1	X	X	**Port C0**	ADC trigger input	-
43	34	26	18	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
44	35	27	19	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
45	36	28	20	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
46	37	29	21	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
47	38	30	22	22	PC5/SPI_SCK(2)	I/O	**X**	X	X	-	O3	X	X	**Port C5**	SPI clock	-
48	39	31	-	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
49	40	32	-	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
50	41	33	23	-	PC6/SPI_MOSI (2)	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
51	42	34	24	-	PC7/SPI_MISO (2)	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
52	43	35	-	23	PG0/CAN_TX	I/O	**X**	X	-	-	O1	X	X	**Port G0**	CAN transmit	-
53	44	36	-	24	PG1/CAN_RX	I/O	**X**	X	-	-	O1	X	X	**Port G1**	CAN receive	-
54	45	-	-	-	PG2	I/O	**X**	X	-	-	O1	X	X	**Port G2**	-	-

6.2 Alternate function remapping

As shown in the rightmost column of *Table 11*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 54*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		Reserved area (1 byte)		
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			

8 Interrupt table

Table 17. STM8A interrupt table(1)

Priority	Source block	Description	Interrupt vector address	Wakeup from Halt	Comments
-	Reset	Reset	0x00 8000	Yes	-
-	TRAP	SW interrupt	0x00 8004	-	-
0	TLI	External top level interrupt	0x00 8008	-	-
1	AWU	Auto-wakeup from Halt	0x00 800C	Yes	-
2	Clock controller	Main clock controller	0x00 8010	-	-
3	MISC	External interrupt E0	0x00 8014	Yes	Port A interrupts
4	MISC	External interrupt E1	0x00 8018	Yes	Port B interrupts
5	MISC	External interrupt E2	0x00 801C	Yes	Port C interrupts
6	MISC	External interrupt E3	0x00 8020	Yes	Port D interrupts
7	MISC	External interrupt E4	0x00 8024	Yes	Port E interrupts
8	CAN	CAN interrupt Rx	0x00 8028	Yes	-
9	CAN	CAN interrupt TX/ER/SC	0x00 802C	-	-
10	SPI	End of transfer	0x00 8030	Yes	-
11	Timer 1	Update/overflow/ trigger/break	0x00 8034	-	-
12	Timer 1	Capture/compare	0x00 8038	-	-
13	Timer 2	Update/overflow	0x00 803C	-	-
14	Timer 2	Capture/compare	0x00 8040	-	-
15	Timer 3	Update/overflow	0x00 8044	-	-
16	Timer 3	Capture/compare	0x00 8048	-	-
17	USART	Tx complete	0x00 804C	-	-
18	USART	Receive data full reg.	0x00 8050	-	-
19	I^2C	I^2C interrupts	0x00 8054	Yes	-
20	LINUART	Tx complete/error	0x00 8058	-	-
21	LINUART	Receive data full reg.	0x00 805C	-	-
22	ADC	End of conversion	0x00 8060	-	-
23	Timer 4	Update/overflow	0x00 8064	-	-
24	EEPROM	End of programming/ write in not allowed area	0x00 8068	-	-

1. All unused interrupts must be initialized with ‘IRET’ for robust programming.

Table 19. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0xFF: Pages 4 to 255 defined as UBC, memory write-protected *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. **AFR4: Alternate function remapping option 4** 0: Port D7 alternate function = TLI 1: Reserved **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Table 19. Option byte description (continued)

Option byte no.	Description
OPT12	**TMU_KEY 5 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	**TMU_KEY 6 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	**TMU_KEY 7 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	**TMU_KEY 8 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	**BL[7:0]: Bootloader enable** If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

Table 29. Programming current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(PROG)}$	Programming current	V_{DD} = 5 V, -40 °C to 150 °C, erasing and programming data or Flash program memory	1.0	1.7	mA

Table 30. Typical peripheral current consumption V_{DD} = 5.0 V(1)

Symbol	Parameter	Typ. f_{master} = 2 MHz	Typ. f_{master} = 16 MHz	Typ. f_{master} =24 MHz	Unit
$I_{DD(TIM1)}$	TIM1 supply current(2)	0.03	0.23	0.34	mA
$I_{DD(TIM2)}$	TIM2 supply current (2)	0.02	0.12	0.19	
$I_{DD(TIM3)}$	TIM3 supply current(2)	0.01	0.1	0.16	
$I_{DD(TIM4)}$	TIM4 supply current(2)	0.004	0.03	0.05	
$I_{DD(USART)}$	USART supply current(2)	0.03	0.09	0.15	
$I_{DD(LINUART)}$	LINUART supply current(2)	0.03	0.11	0.18	
$I_{DD(SPI)}$	SPI supply current(2)	0.01	0.04	0.07	
$I_{DD(I^2C)}$	I^2C supply current(2)	0.02	0.06	0.91	
$I_{DD(CAN)}$	CAN supply current(3)	0.06	0.30	0.40	
$I_{DD(AWU)}$	AWU supply current(2)	0.003	0.02	0.05	
$I_{DD(TOT\_DIG)}$	All digital peripherals on	0.22	1	2.4	
$I_{DD(ADC)}$	ADC supply current when converting(4)	0.93	0.95	0.96	

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1 MHz. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Low-speed internal RC oscillator (LSI)

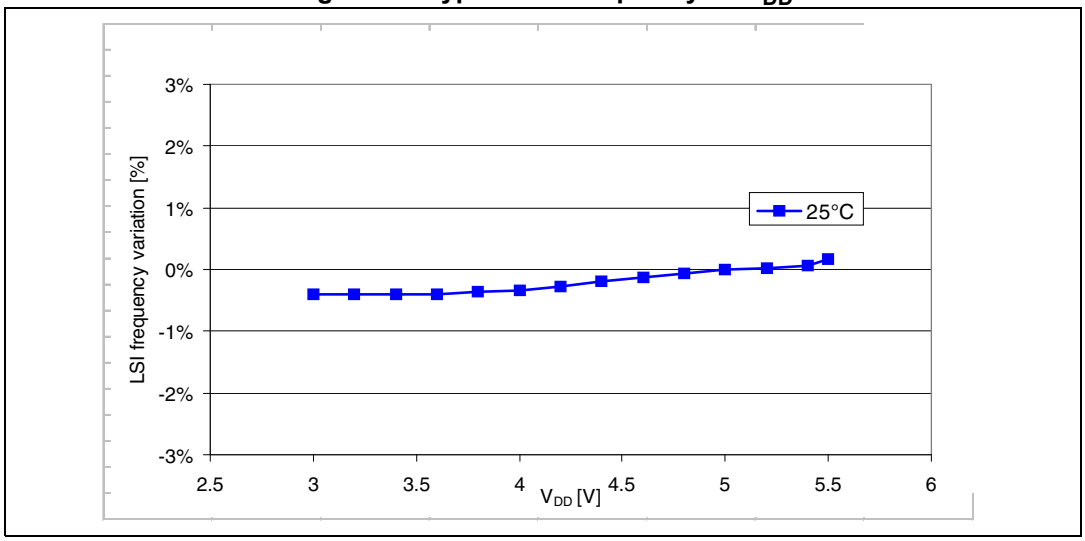
Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}



10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

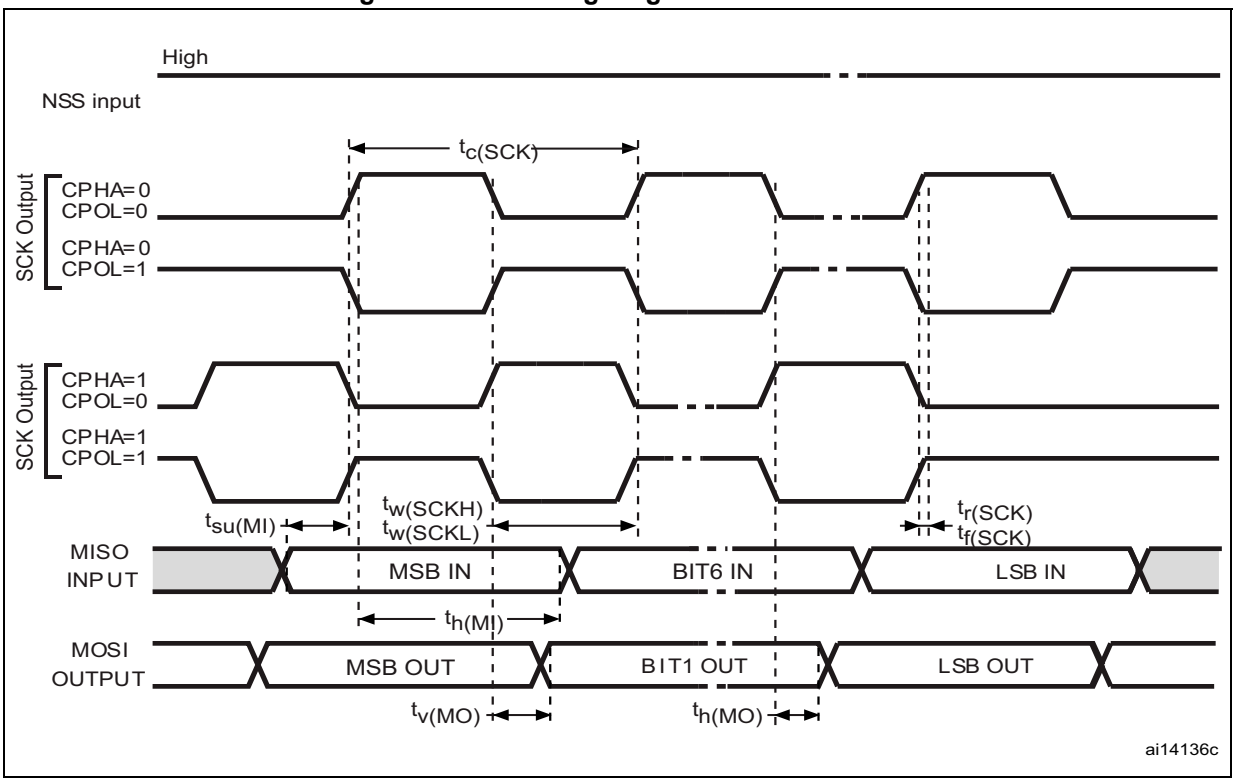
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 42. SPI timing diagram - master mode



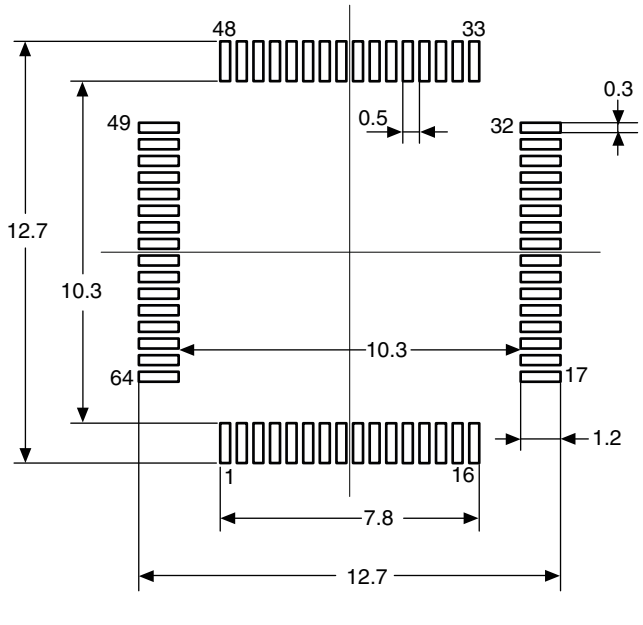
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

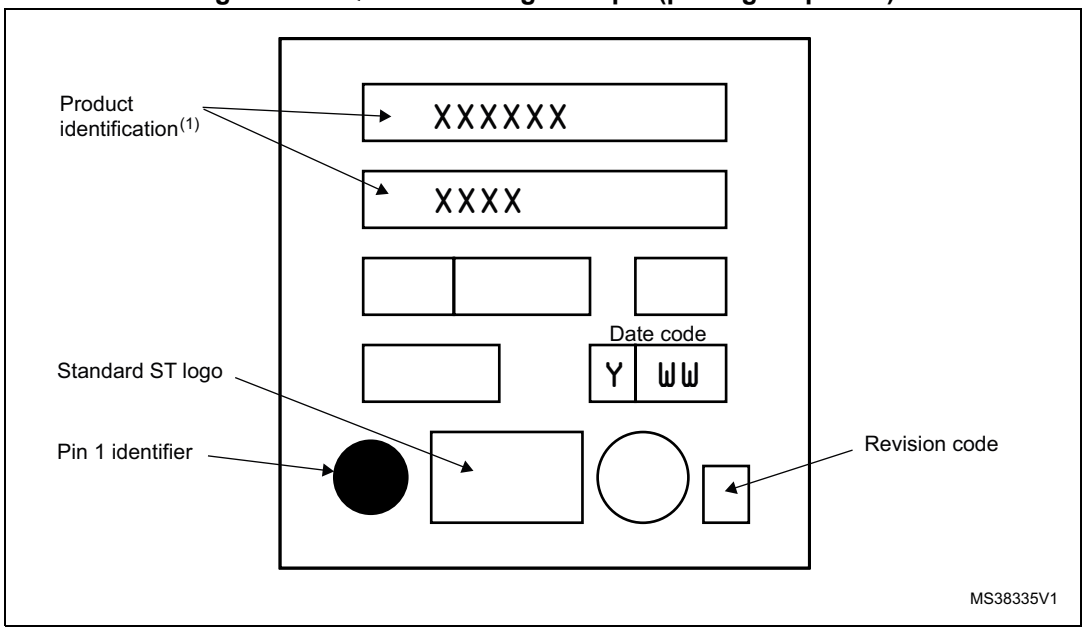
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Figure 53. LQFP48 marking example (package top view)



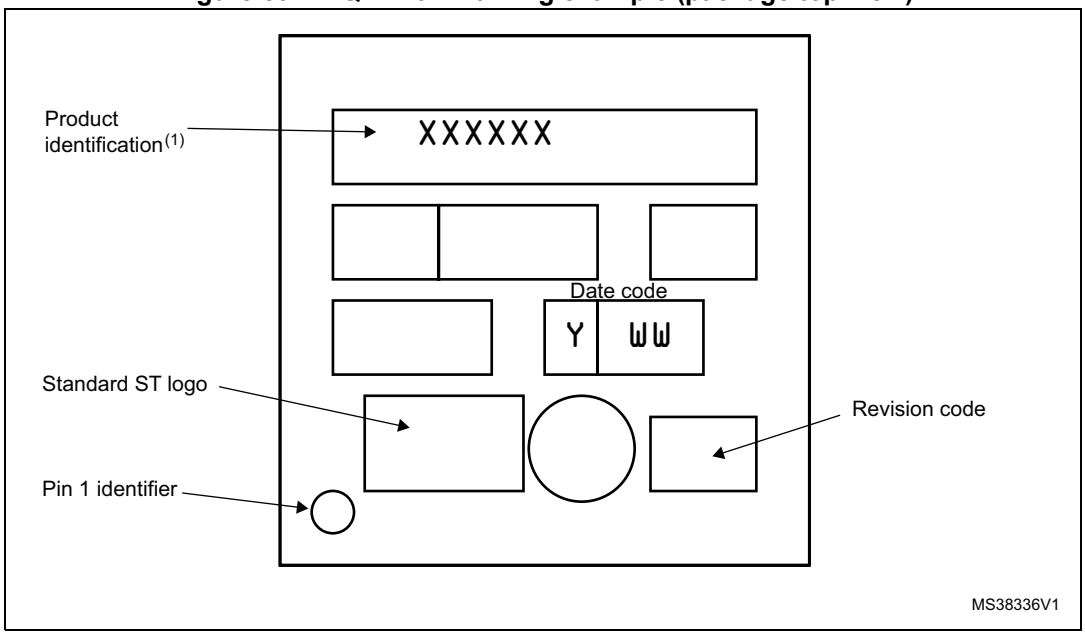
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. VFQFPN32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

13 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

13.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

13.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high-speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Aug-2008	2 (continued)	*Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers. *Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL) *Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU). *Table 23: Operating lifetime:* Amended footnotes. *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'. *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes. *Table 28: Oscillator current consumption*: Replaced. *Table 29: Programming current consumption*: Amended maximum data and footnotes. *Table 21: Current characteristics*: Replaced. *Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes. *Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes. *Figure 13* to *Figure 18*: info on peripheral activity added. *Table 33: HSI oscillator characteristics*: Modified f_{HSE_ext} data and added V_{HSEdhl} data. *Table 35: Flash program memory/data EEPROM memory*: Removed ACC_{HSI} parameters and replaced with ACC_{HS} parameters; amended data and footnotes. Amended data of '*RAM and hardware registers*' table. *Table 37: Data memory*: Updated names and data of N_{RW} and t_{RET} parameters. *Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added V_{OH} and V_{OL} parameters; Updated $I_{lkg\ ana}$ parameter. Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*. *Table 46: EMI data*: Updated f_{ADC}, t_S, and t_{CONV} data. *Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters. *Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2. *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for T_A = 145 °C. *Figure 53*: Updated memory size, pin count and package type information.

Table 55. Document revision history (continued)

Date	Revision	Changes
31-Mar-2014	10 (continued)	Added: – *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout;* – the caution in *Section 5.10: Input/output specifications,* – The table footnote “Not recommended for new designs” to *Table: STM8AF/H/P51xx product line-up with CAN* and *Table: STM8AF/H/P61xx product line-up without CAN.* – The figure footnotes to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* and *Figure: VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)*
13-Jun-2014	11	Added STM8AF52A6 part number.
09-Jun-2015	12	Added: – the third table footnote to *Table 25: Operating conditions at power-up/power-down*, – *Figure 47: LQFP80 marking example (package top view)*, – *Figure 50: LQFP64 marking example (package top view)*, – *Figure 53: LQFP48 marking example (package top view)*, – *Figure 56: LQFP32 marking example (package top view)*, – *Figure 59: VFQFPN32 marking example (package top view)*, – the footnote about the device marking to *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Removed STM8AF51xx and STM8AF61xx obsolete root part numbers, and consequently “H” products: – *Table 1: Device summary*, – *Section 1: Introduction*, – *Section 2: Description*, – *Section 3: Product line-up*, – *Table 12: Memory model 128K*, – *Section 10.3: Operating conditions*, – *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Moved *Section 11.6: Thermal characteristics* to *Section 11: Package information*. Updated: – the product naming in the document headers and captions, – the standard reference for EMI characteristics in *Table 46: EMI data*.
13-Jun-2016	13	Updated *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data*