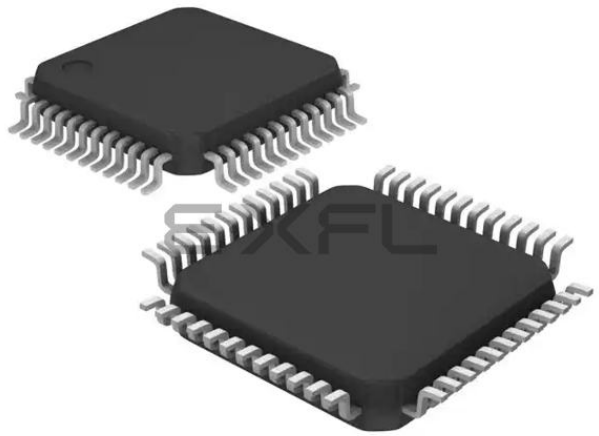

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a8tcx

List of tables

3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P5289		64 K						
STM8AF/P5269		32 K		1 K				
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K		1K				
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I²C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I²C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P6289		64 K		2 K				
STM8AF/P6269		32 K		1 K				
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P6288		64 K						
STM8AF/P6286	LQFP32 (7x7)				7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P62A6	VFQFPN32 (5x5)	128 K						

5.9.2 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

LIN mode

Master mode

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Table 14. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x40
0x00 5060 to 0x005061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART	UART1_SR	USART status register	0xC0
0x00 5231		UART1_DR	USART data register	0xXX
0x00 5232		UART1_BRR1	USART baud rate register 1	0x00
0x00 5233		UART1_BRR2	USART baud rate register 2	0x00
0x00 5234		UART1_CR1	USART control register 1	0x00
0x00 5235		UART1_CR2	USART control register 2	0x00
0x00 5236		UART1_CR3	USART control register 3	0x00
0x00 5237		UART1_CR4	USART control register 4	0x00
0x00 5238		UART1_CR5	USART control register 5	0x00
0x00 5239		UART1_GTR	USART guard time register	0x00
0x00 523A		UART1_PSCR	USART prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	LINUART	UART3_SR	LINUART status register	0xC0
0x00 5241		UART3_DR	LINUART data register	0xXX
0x00 5242		UART3_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART3_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART3_CR1	LINUART control register 1	0x00
0x00 5245		UART3_CR2	LINUART control register 2	0x00
0x00 5246		UART3_CR3	LINUART control register 3	0x00
0x00 5247		UART3_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

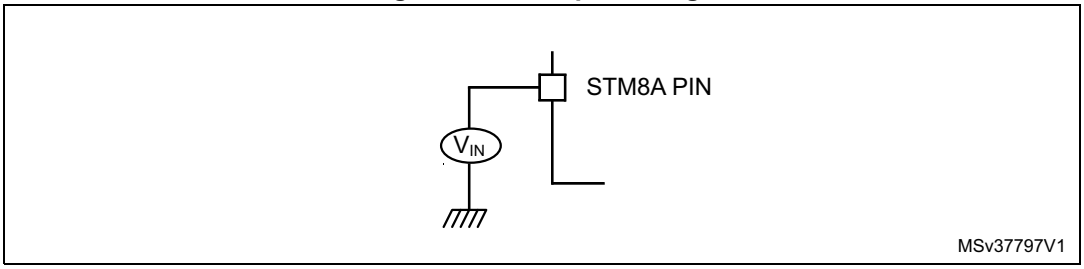
Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics* and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability. The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 20. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 88*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 21. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDDIO}	Total current into V_{DDIO} power lines (source)(1)(2)(3)	100	mA
I_{VSSIO}	Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(4)	Injected current on any pin	±10	
$I_{INJ(TOT)}$	Sum of injected currents	50	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. V_{DDIO} includes the sum of the positive injection currents. V_{SSIO} includes the sum of the negative injection currents.
4. This condition is implicitly insured if VIN maximum is respected. If VIN maximum cannot be respected, the injection current must be limited externally to the IINJ(PIN) value. A positive injection is induced by VIN > VDD while a negative injection is induced by VIN < VSS. For true open-drain pads, there is no positive injection current allowed and the corresponding VIN maximum must always be respected.

Table 22. Thermal characteristics

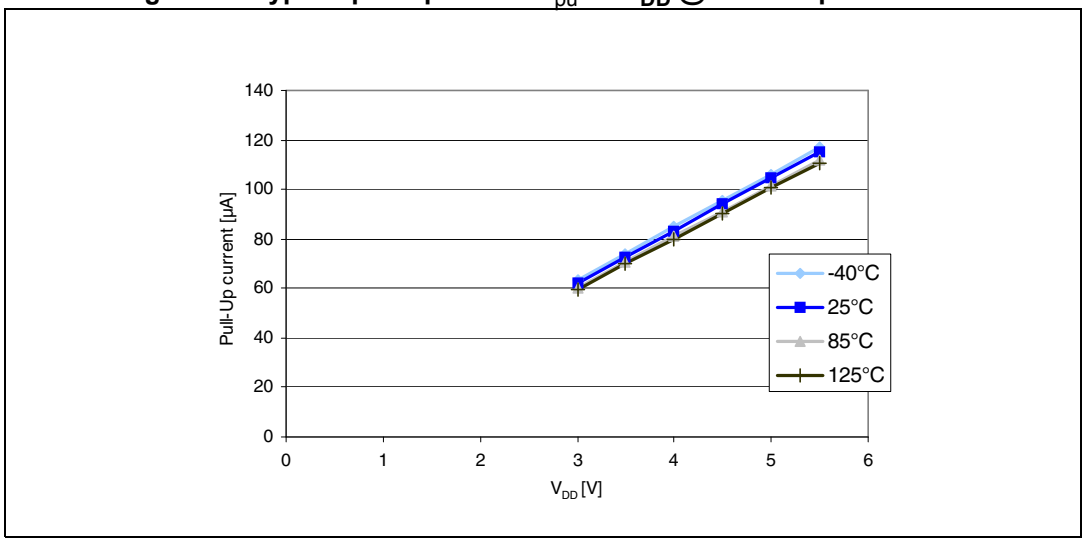
Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	160	

Table 23. Operating lifetime(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100 rev G	-40 to 125 °C	Grade 1
		-40 to 150 °C	Grade 0

1. For detailed mission profile analysis, please contact the nearest ST Sales Office.

Figure 25. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures(1)



1. The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 26 to *Figure 35* show typical output level curves measured with output on a single pin.

Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

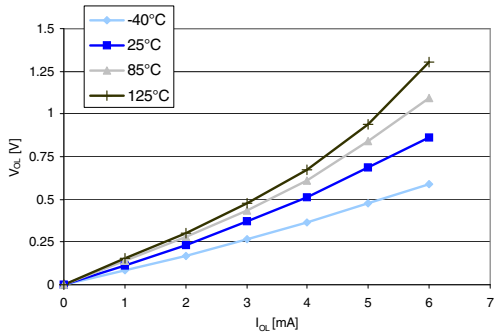


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

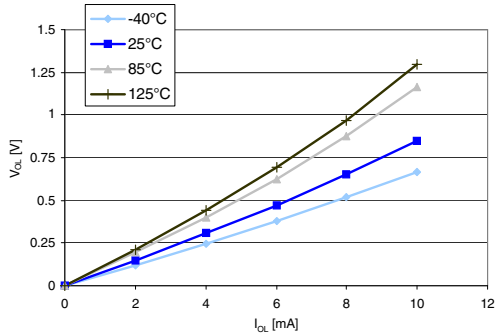


Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

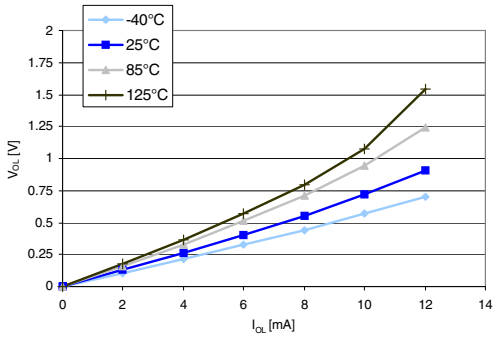


Figure 29. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

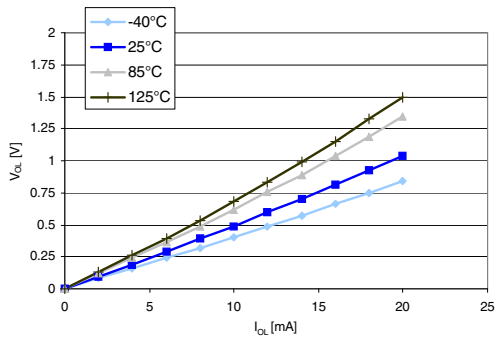


Figure 30. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

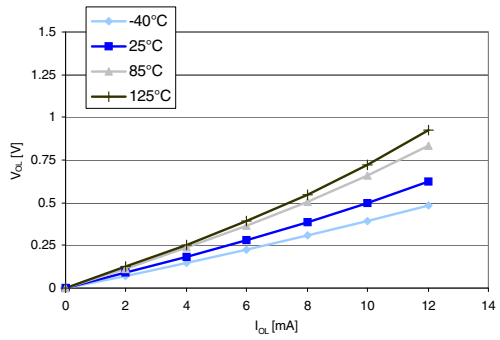


Figure 31. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

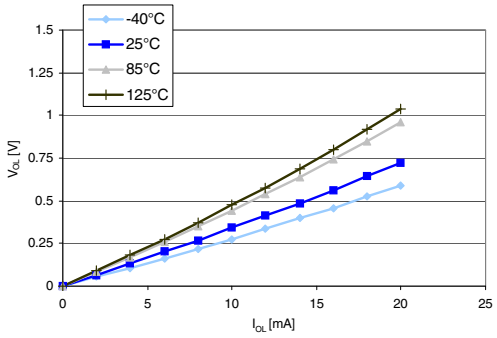


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

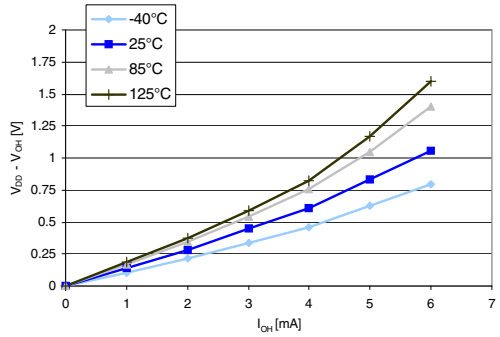


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

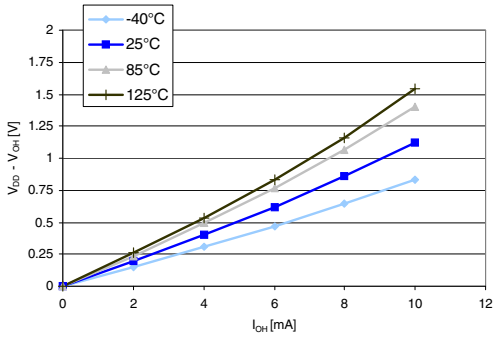


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

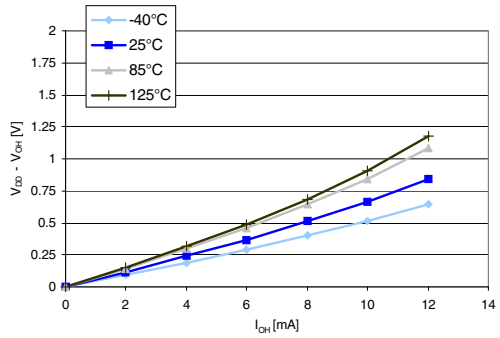
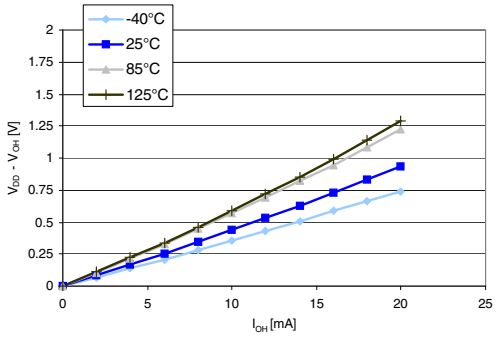


Figure 35. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency, and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

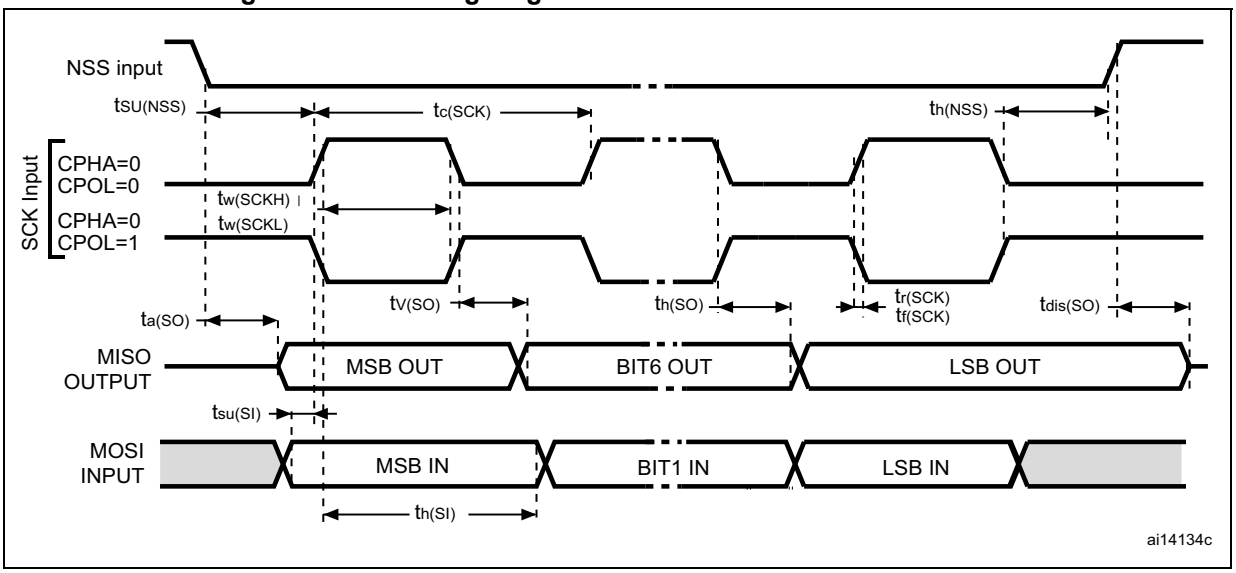
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

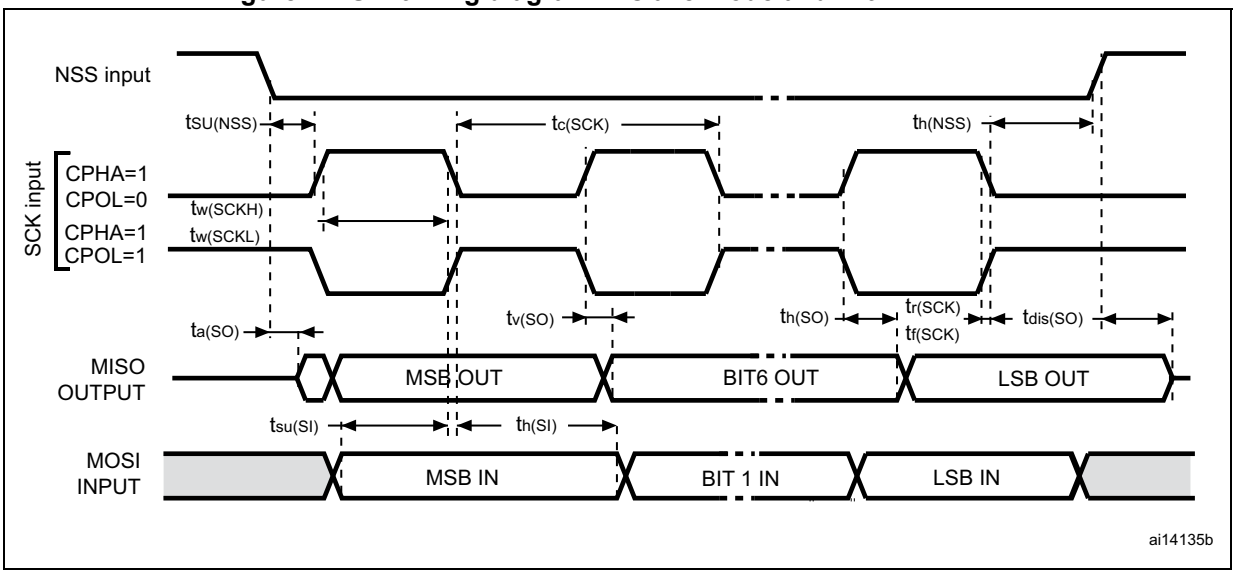
1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 40. SPI timing diagram in slave mode and with CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.11 10-bit ADC characteristics

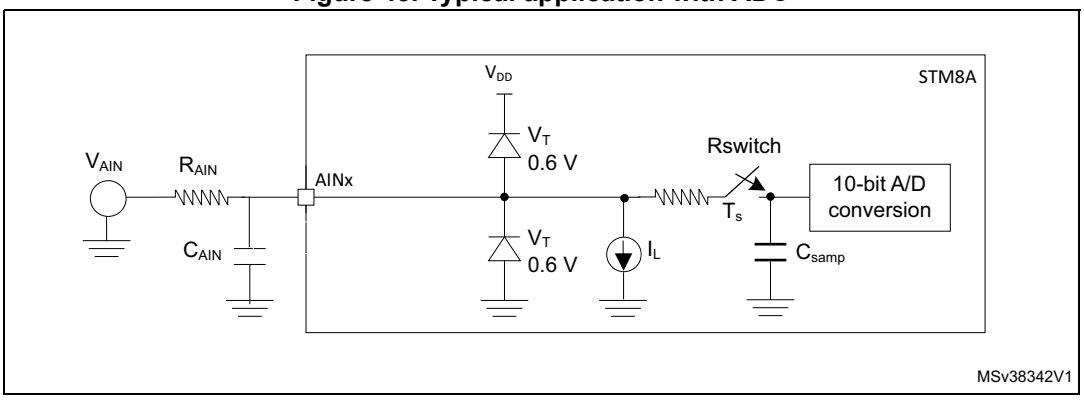
Subject to general operating conditions for V_{DDA}, f_{MASTER} and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 43. Typical application with ADC



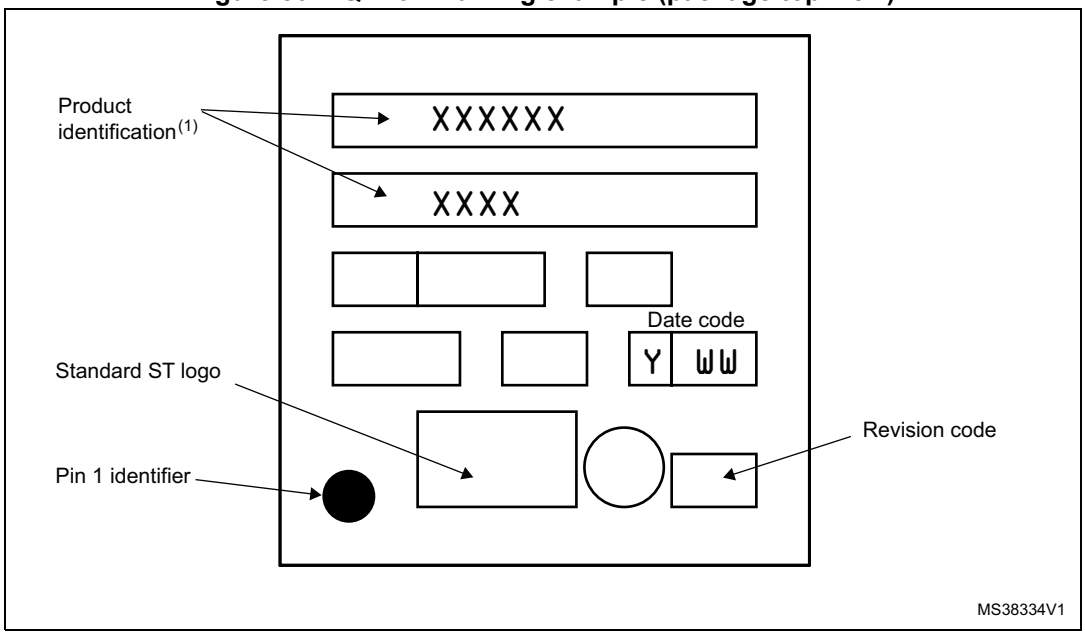
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP64 marking example (package top view)



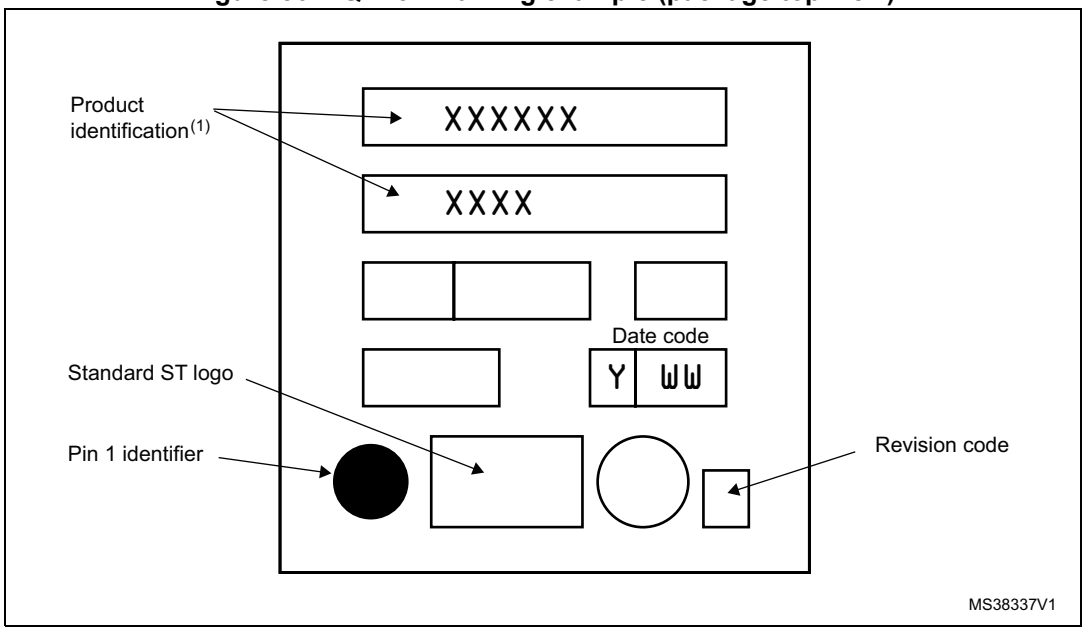
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

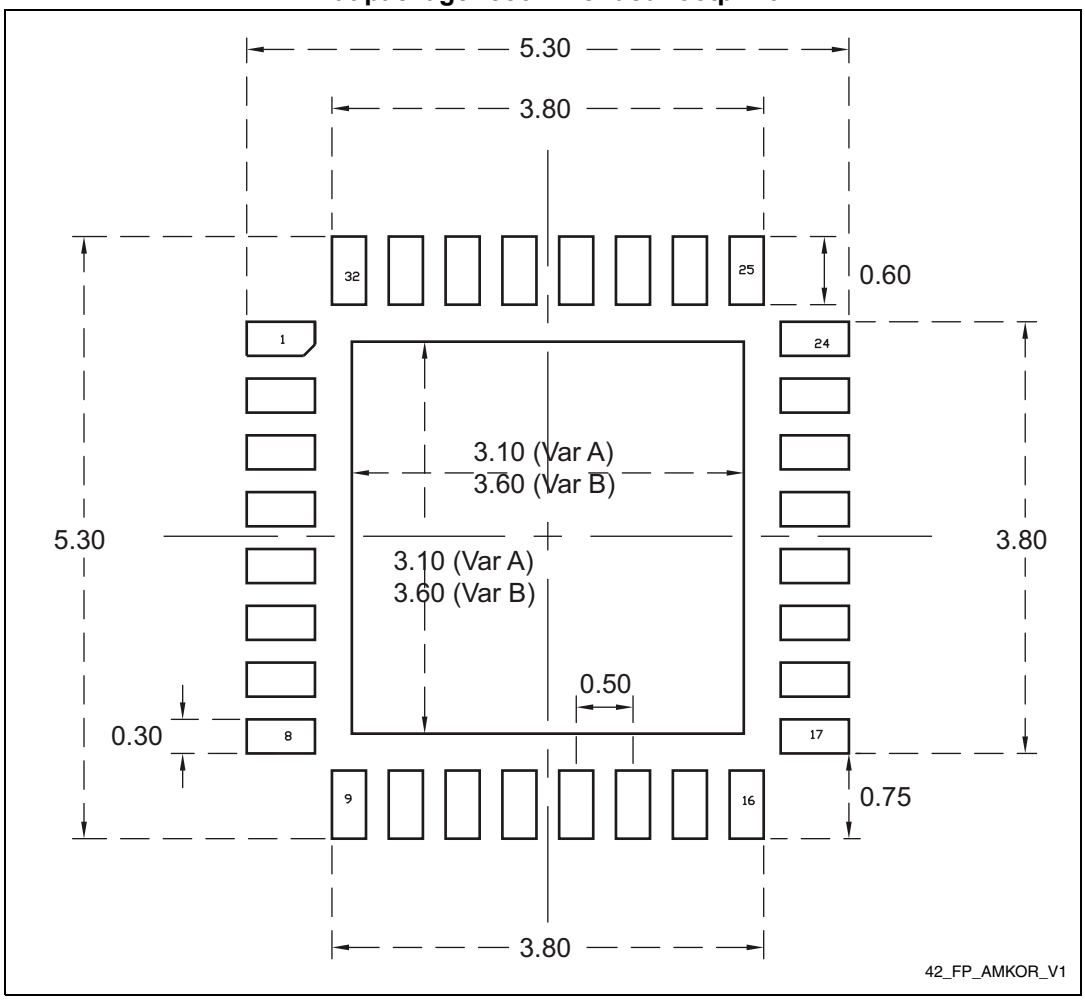
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP32 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Aug-2008	2 (continued)	*Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers. *Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL) *Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU). *Table 23: Operating lifetime:* Amended footnotes. *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'. *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes. *Table 28: Oscillator current consumption*: Replaced. *Table 29: Programming current consumption*: Amended maximum data and footnotes. *Table 21: Current characteristics*: Replaced. *Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes. *Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes. *Figure 13* to *Figure 18*: info on peripheral activity added. *Table 33: HSI oscillator characteristics*: Modified f_{HSE_ext} data and added V_{HSEdhl} data. *Table 35: Flash program memory/data EEPROM memory*: Removed ACC_{HSI} parameters and replaced with ACC_{HS} parameters; amended data and footnotes. Amended data of '*RAM and hardware registers*' table. *Table 37: Data memory*: Updated names and data of N_{RW} and t_{RET} parameters. *Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added V_{OH} and V_{OL} parameters; Updated $I_{lkg\ ana}$ parameter. Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*. *Table 46: EMI data*: Updated f_{ADC}, t_S, and t_{CONV} data. *Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters. *Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2. *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for T_A = 145 °C. *Figure 53*: Updated memory size, pin count and package type information.

Table 55. Document revision history (continued)

Date	Revision	Changes
31-Mar-2014	10 (continued)	Added: – *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout;* – the caution in *Section 5.10: Input/output specifications,* – The table footnote “Not recommended for new designs” to *Table: STM8AF/H/P51xx product line-up with CAN* and *Table: STM8AF/H/P61xx product line-up without CAN.* – The figure footnotes to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* and *Figure: VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)*
13-Jun-2014	11	Added STM8AF52A6 part number.
09-Jun-2015	12	Added: – the third table footnote to *Table 25: Operating conditions at power-up/power-down*, – *Figure 47: LQFP80 marking example (package top view)*, – *Figure 50: LQFP64 marking example (package top view)*, – *Figure 53: LQFP48 marking example (package top view)*, – *Figure 56: LQFP32 marking example (package top view)*, – *Figure 59: VFQFPN32 marking example (package top view)*, – the footnote about the device marking to *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Removed STM8AF51xx and STM8AF61xx obsolete root part numbers, and consequently “H” products: – *Table 1: Device summary*, – *Section 1: Introduction*, – *Section 2: Description*, – *Section 3: Product line-up*, – *Table 12: Memory model 128K*, – *Section 10.3: Operating conditions*, – *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Moved *Section 11.6: Thermal characteristics* to *Section 11: Package information*. Updated: – the product naming in the document headers and captions, – the standard reference for EMI characteristics in *Table 46: EMI data*.
13-Jun-2016	13	Updated *Table 53: VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data*