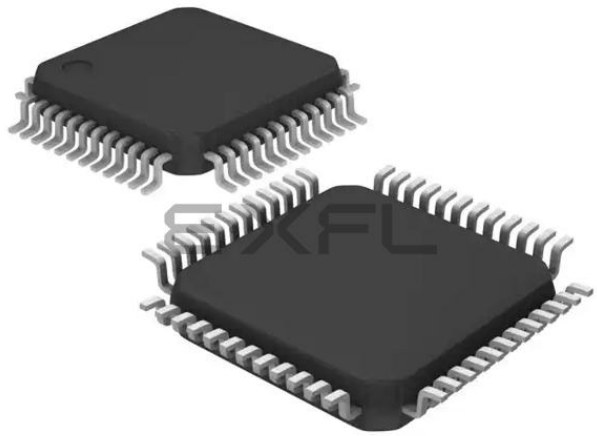

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a8tdx

Contents

5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

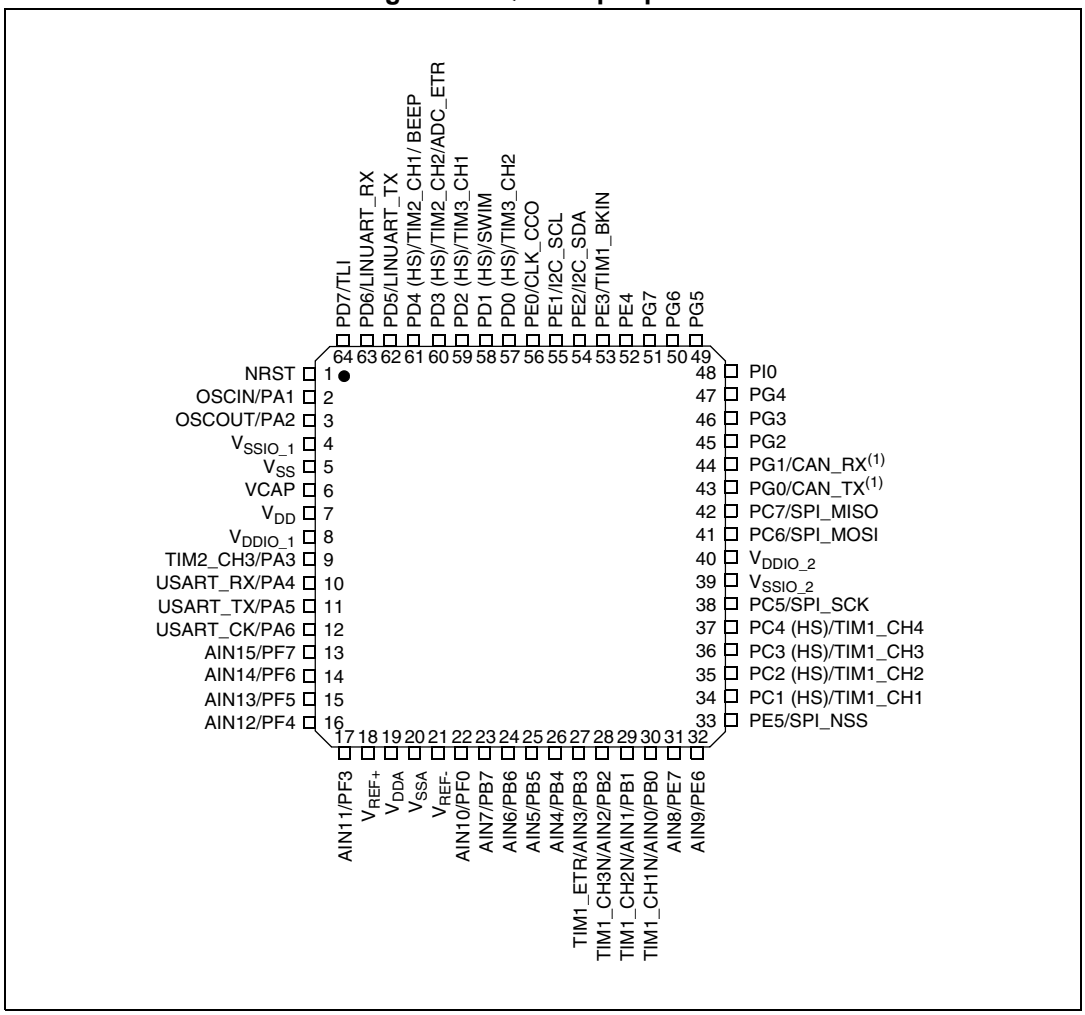
To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

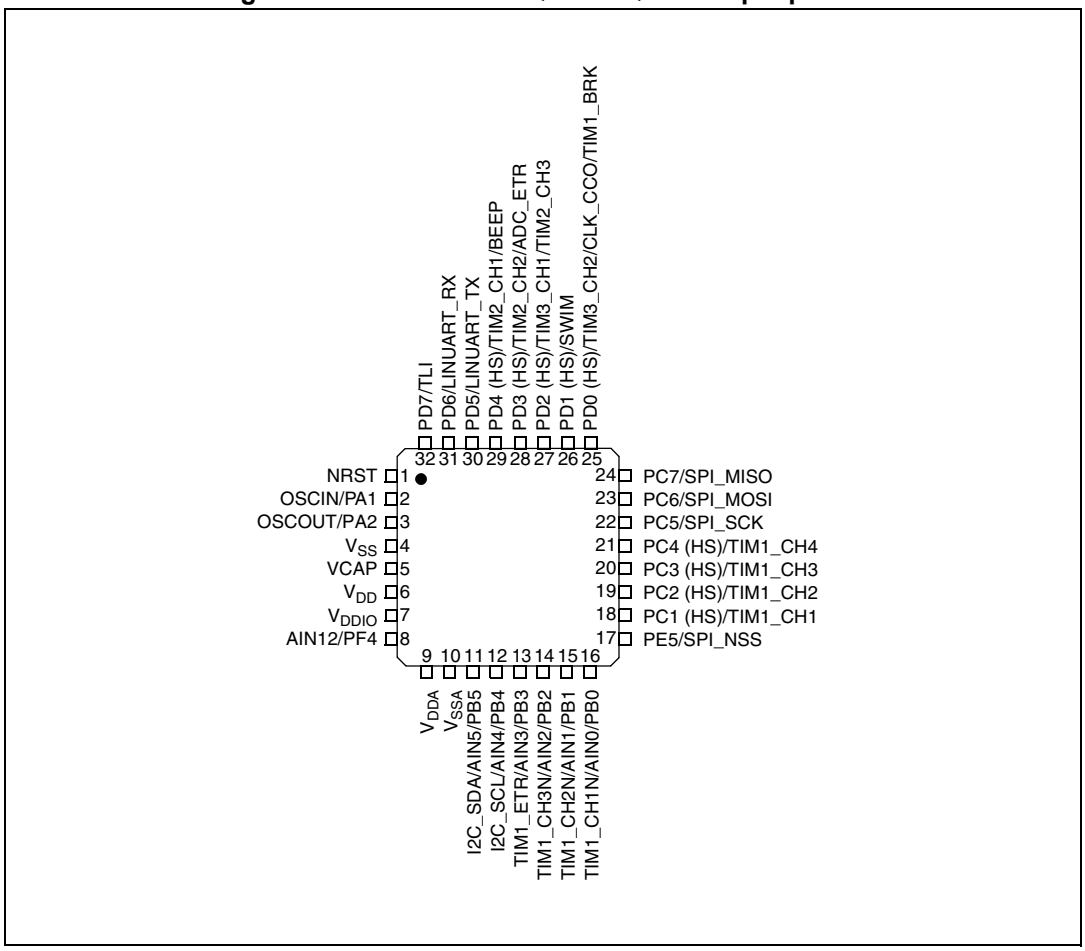
Caution: In STM8AF5286UC device, the following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7.
As a consequence, they must be put into one of the following configurations by software:
- configured as input with internal pull-up/down resistor,
- configured as output push-pull low.

Figure 4. LQFP 64-pin pinout



1. The CAN interface is only available on STM8AF52xx product lines.
2. HS stands for high sink capability.

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout



1. HS stands for high sink capability.

Table 10. Legend/abbreviation for the pin description table

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = high sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
55	46	-	-	-	PG3	I/O	**X**	X	-	-	O1	X	X	**Port G3**	-	-
56	47	-	-	-	PG4	I/O	**X**	X	-	-	O1	X	X	**Port G4**	-	-
57	48	-	-	-	PI0	I/O	**X**	X	-	-	O1	X	X	**Port I0**	-	-
58	-	-	-	-	PI1	I/O	**X**	X	-	-	O1	X	X	**Port I1**	-	-
59	-	-	-	-	PI2	I/O	**X**	X	-	-	O1	X	X	**Port I2**	-	-
60	-	-	-	-	PI3	I/O	**X**	X	-	-	O1	X	X	**Port I3**	-	-
61	-	-	-	-	PI4	I/O	**X**	X	-	-	O1	X	X	**Port I4**	-	-
62	-	-	-	-	PI5	I/O	**X**	X	-	-	O1	X	X	**Port I5**	-	-
63	49	-	-	-	PG5	I/O	**X**	X	-	-	O1	X	X	**Port G5**	-	-
64	50	-	-	-	PG6	I/O	**X**	X	-	-	O1	X	X	**Port G6**	-	-
65	51	-	-	-	PG7	I/O	**X**	X	-	-	O1	X	X	**Port G7**	-	-
66	52	-	-	-	PE4	I/O	**X**	X	X	-	O1	X	X	**Port E4**	-	-
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
68	54	38	-	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port E2**	I^2C data	-
69	55	39	-	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port E1**	I^2C clock	-
70	56	40	-	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
71	-	-	-	-	PI6	I/O	**X**	X	-	-	O1	X	X	**Port I6**	-	-
72	-	-	-	-	PI7	I/O	**X**	X	-	-	O1	X	X	**Port I7**	-	-
73	57	41	25	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
75	59	43	27	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	28	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]

Table 12. Memory model 128K

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
128 K	0x00 27FFF	6 K	0x00 17FF	0x00 1400
64 K	0x00 17FFF			
32 K	0x00 0FFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 13. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			

Table 26. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 °C to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 24 MHz 1 ws	8.7	16.8(2)	mA
			f_{CPU} = 16 MHz	7.4	14	
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM, HSE external clock (without resonator)	f_{CPU} = 24 MHz	4.4	6.0(2)	
			f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 24 MHz	2.4	3.1(2)	
			f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	External clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

Low-speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Guaranteed by characterization results, not tested in production.

Figure 22. Typical LSI frequency vs V_{DD}

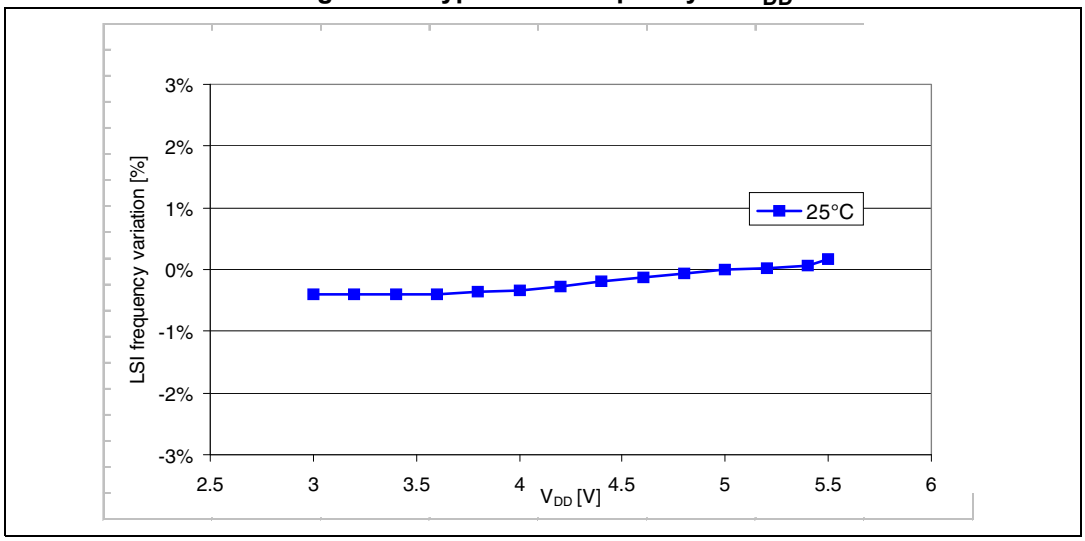
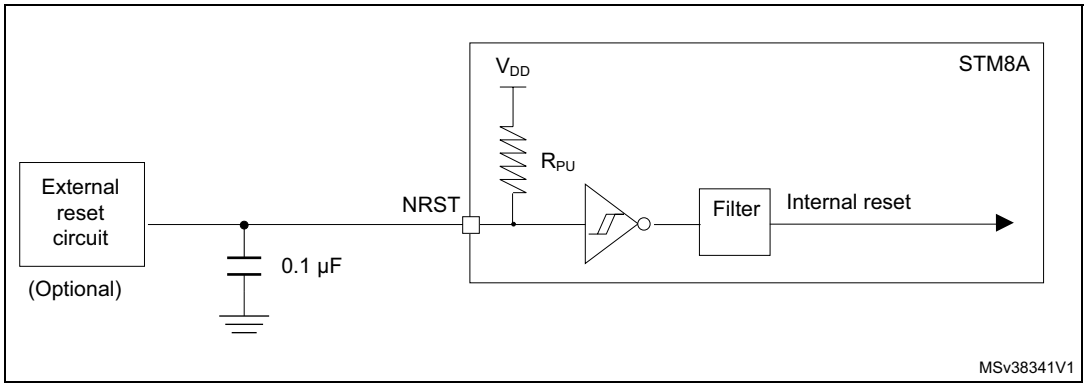


Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

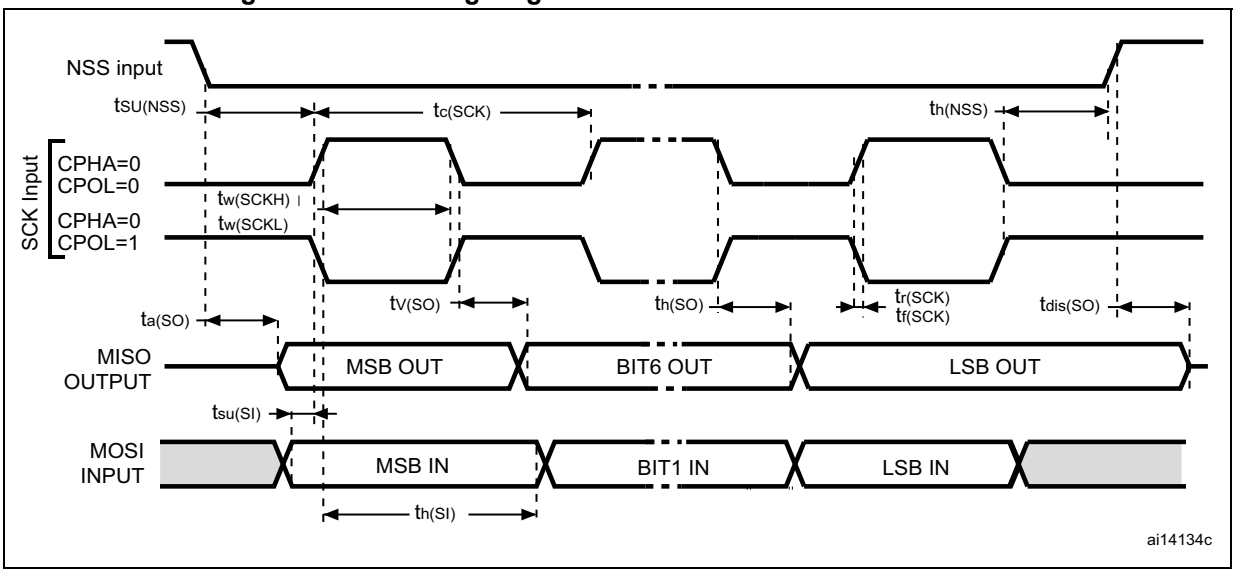
Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

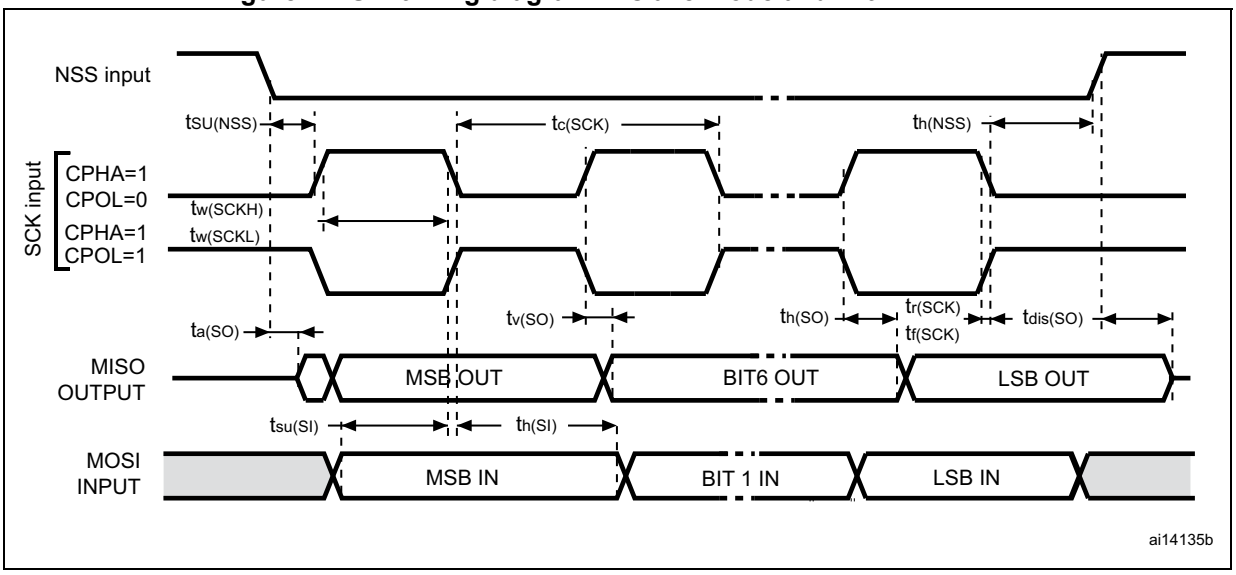
1. Not tested in production.

Figure 40. SPI timing diagram in slave mode and with CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



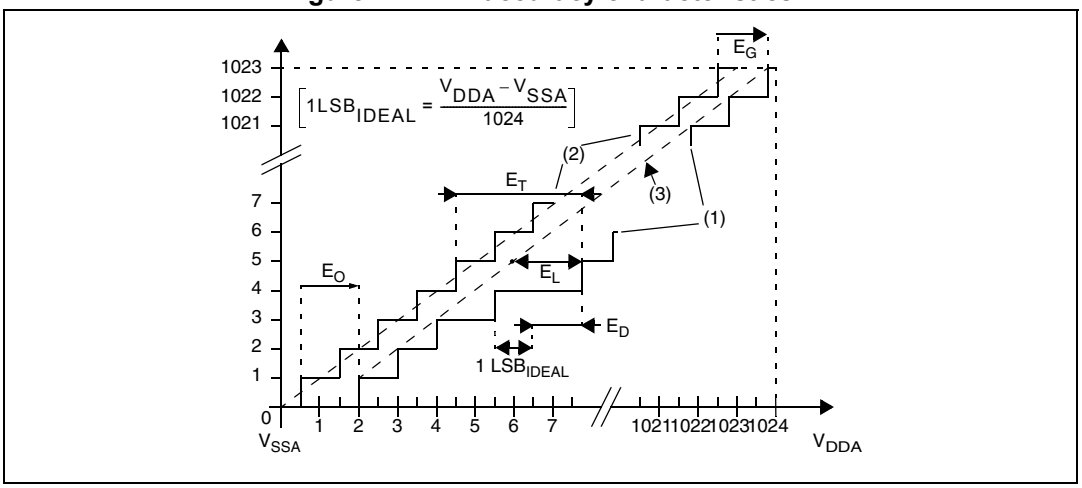
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 44. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 44. ADC accuracy characteristics



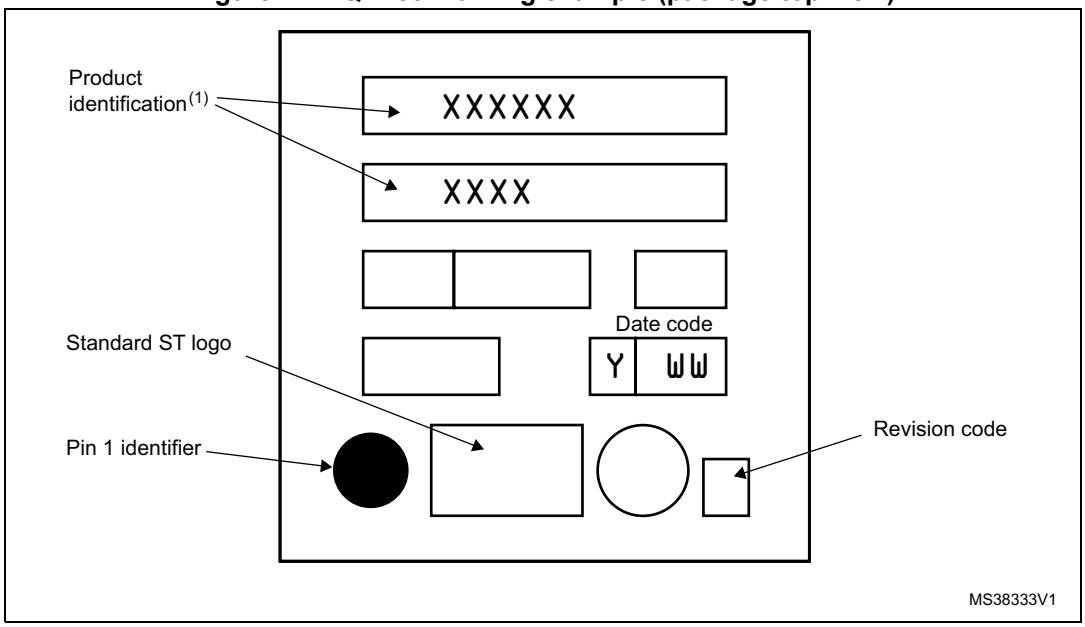
1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP80 marking example (package top view)



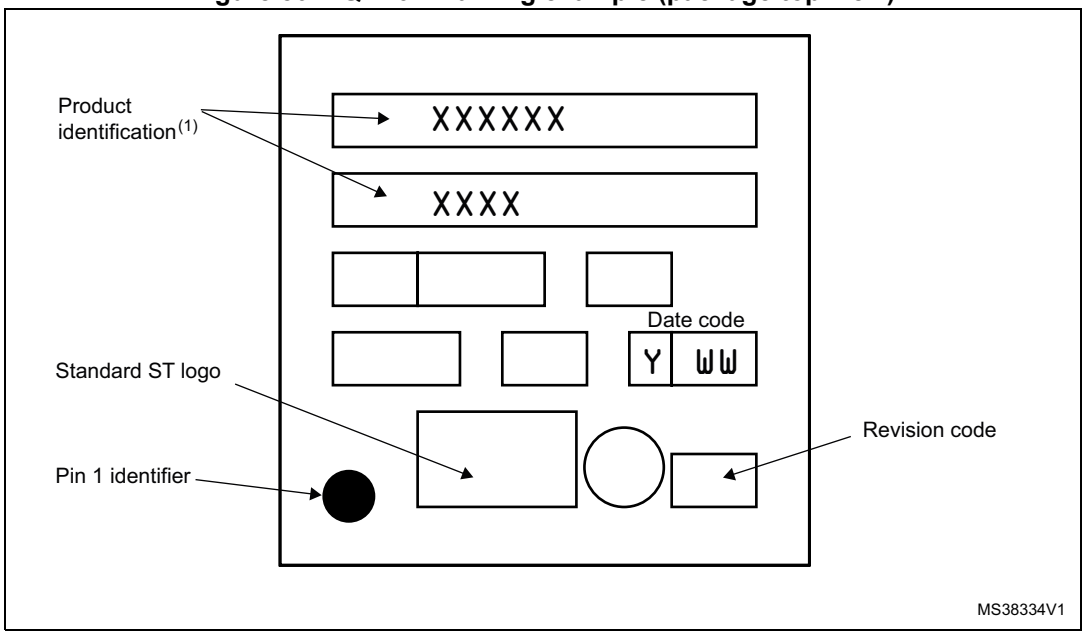
1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

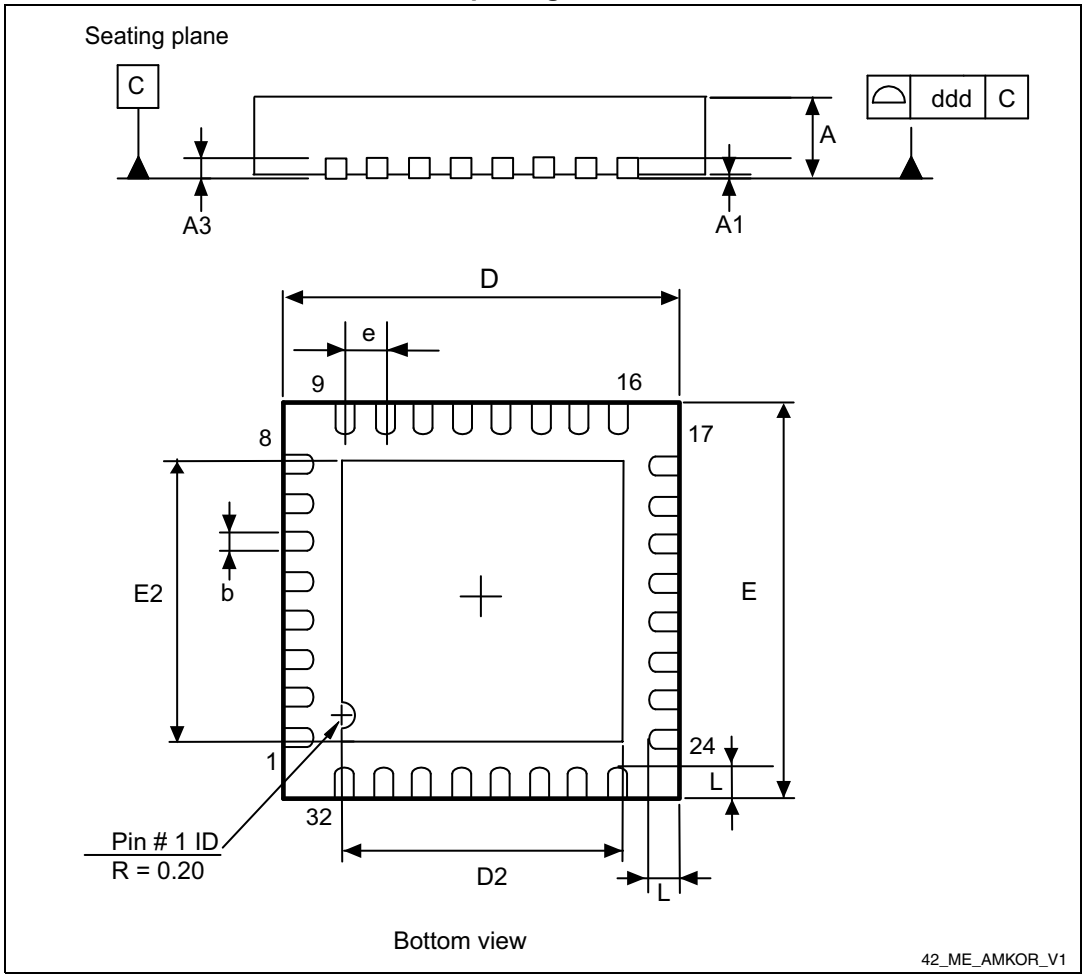
Figure 50. LQFP64 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

11.5 VFQFPN32 package information

Figure 57. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.

Table 53. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.6 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 24: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low- and high-level in the application.

Table 54. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	
	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	25	

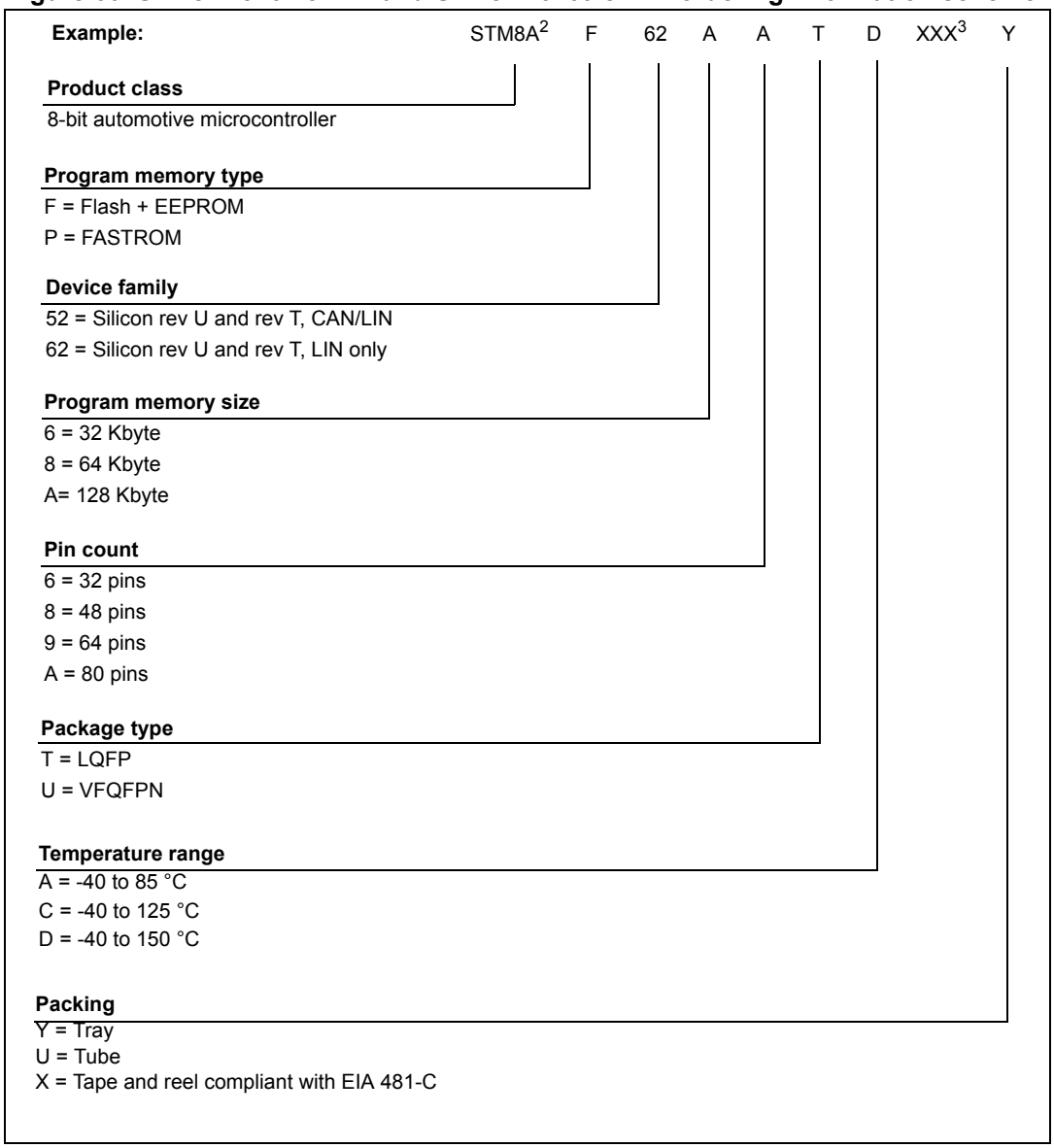
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12 Ordering information

Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme[1]



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.