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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62a9tdy

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3 Product line-up

Table 2. STM8AF526x/8x/Ax product line-up with CAN

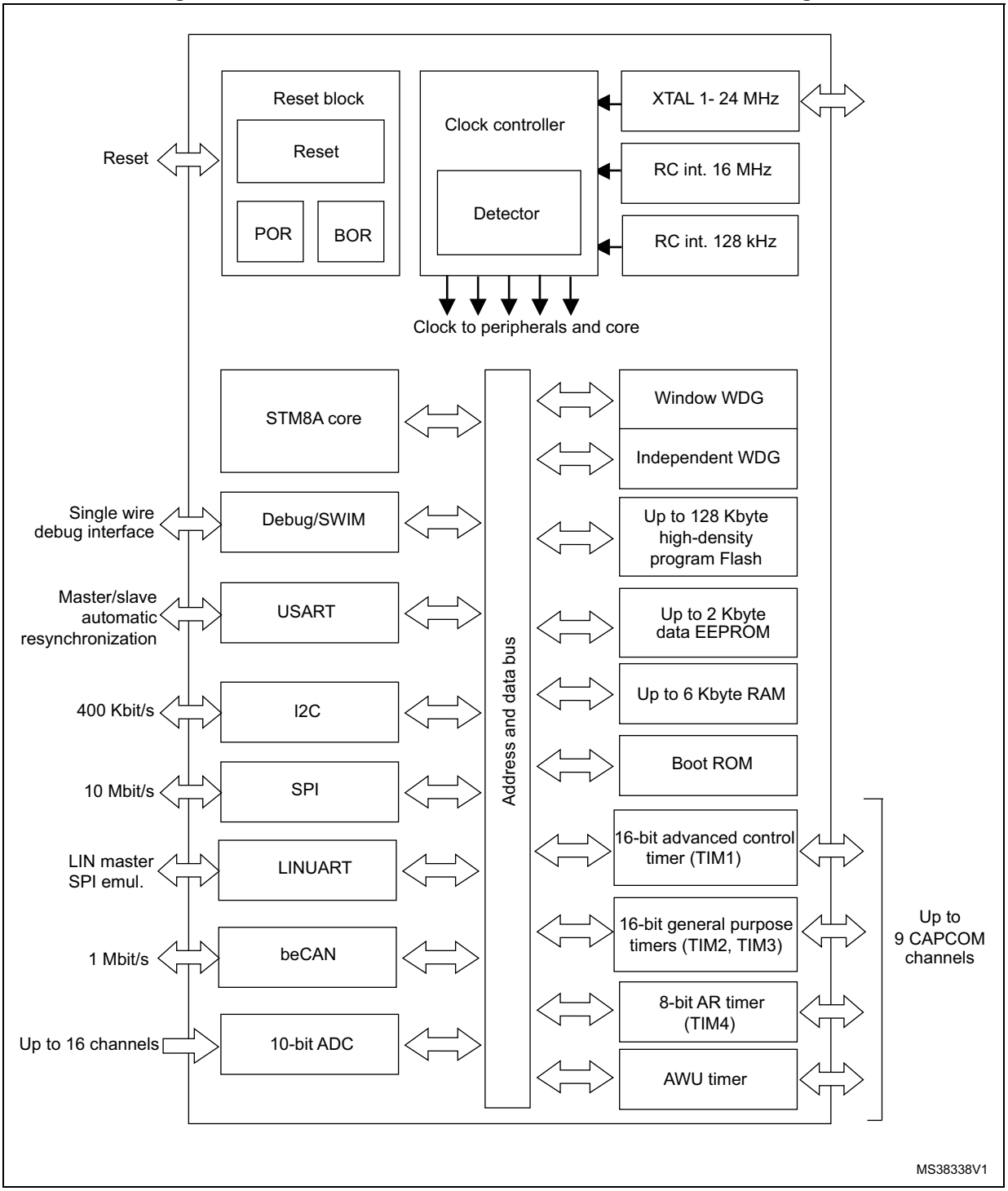
Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P52AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	68/37
STM8AF/P528A		64 K						
STM8AF/P52A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P5289		64 K						
STM8AF/P5269		32 K		1 K				
STM8AF/P52A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P5288		64 K						
STM8AF/P5268		32 K		1K				
STM8AF/P5286	VFQFPN32 (5x5)	64 K		2 K	6	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), I²C	25/24
STM8AF/P52A6		128 K						

Table 3. STM8AF6269/8x/Ax product line-up without CAN

Order code	Package	High density Flash program memory (bytes)	RAM (bytes)	Data EEPROM (bytes)	10-bit A/D chan.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P62AA	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I²C	68/37
STM8AF/P628A		64 K						
STM8AF/P62A9	LQFP64 (10x10)	128 K						52/36
STM8AF/P6289		64 K		2 K				
STM8AF/P6269		32 K		1 K				
STM8AF/P62A8	LQFP48 (7x7)	128 K		2 K	10			38/35
STM8AF/P6288		64 K						
STM8AF/P6286	LQFP32 (7x7)				7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P62A6	VFQFPN32 (5x5)	128 K						

4 Block diagram

Figure 1. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram



5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

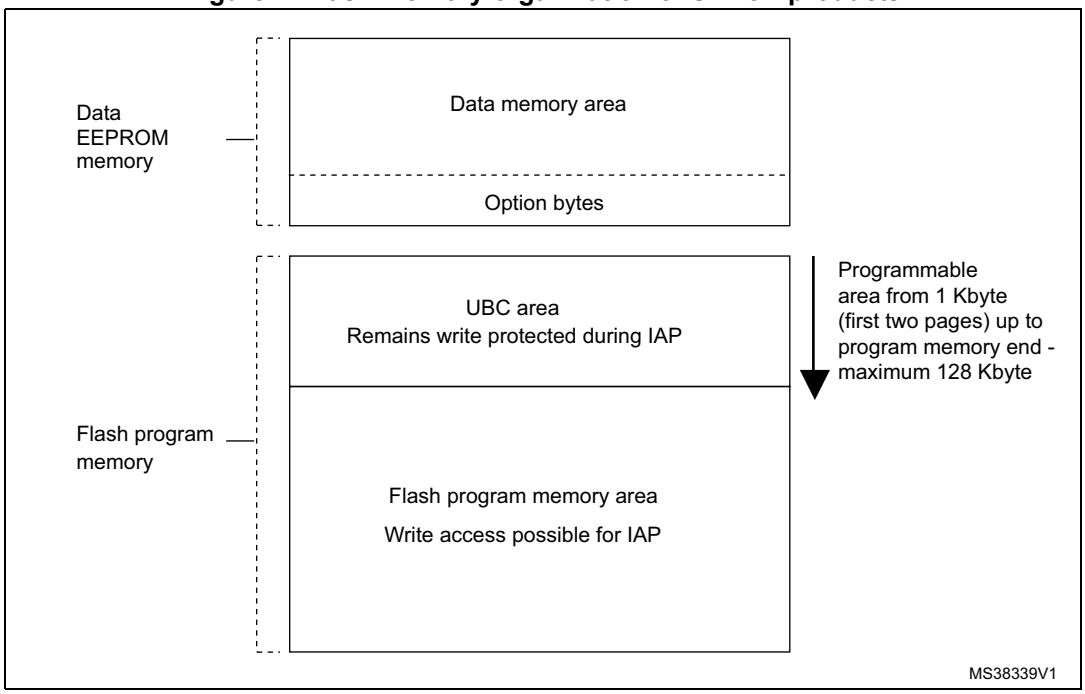
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 54*).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

Table 6. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

TIM1 - advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.5 Basic timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

Table 7. TIM4

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM4	8-bit	Up	2^n n = 0 to 7	0	None	No	No	No	No

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
55	46	-	-	-	PG3	I/O	**X**	X	-	-	O1	X	X	**Port G3**	-	-
56	47	-	-	-	PG4	I/O	**X**	X	-	-	O1	X	X	**Port G4**	-	-
57	48	-	-	-	PI0	I/O	**X**	X	-	-	O1	X	X	**Port I0**	-	-
58	-	-	-	-	PI1	I/O	**X**	X	-	-	O1	X	X	**Port I1**	-	-
59	-	-	-	-	PI2	I/O	**X**	X	-	-	O1	X	X	**Port I2**	-	-
60	-	-	-	-	PI3	I/O	**X**	X	-	-	O1	X	X	**Port I3**	-	-
61	-	-	-	-	PI4	I/O	**X**	X	-	-	O1	X	X	**Port I4**	-	-
62	-	-	-	-	PI5	I/O	**X**	X	-	-	O1	X	X	**Port I5**	-	-
63	49	-	-	-	PG5	I/O	**X**	X	-	-	O1	X	X	**Port G5**	-	-
64	50	-	-	-	PG6	I/O	**X**	X	-	-	O1	X	X	**Port G6**	-	-
65	51	-	-	-	PG7	I/O	**X**	X	-	-	O1	X	X	**Port G7**	-	-
66	52	-	-	-	PE4	I/O	**X**	X	X	-	O1	X	X	**Port E4**	-	-
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
68	54	38	-	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port E2**	I^2C data	-
69	55	39	-	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port E1**	I^2C clock	-
70	56	40	-	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
71	-	-	-	-	PI6	I/O	**X**	X	-	-	O1	X	X	**Port I6**	-	-
72	-	-	-	-	PI7	I/O	**X**	X	-	-	O1	X	X	**Port I7**	-	-
73	57	41	25	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
75	59	43	27	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	28	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
78	62	46	30	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-
79	63	47	31	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
80	64	48	32	32	PD7/TLI(5)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. SPI and USTART are not available in STM8AF5286UC, refer to *Figure 7: STM8AF52x6 VFQFPN32 32-pin pinout* for the pin names.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to V_{DD} are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after reset release.
5. If this pin is configured as interrupt pin, it will trigger the TLI.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		Reserved area (1 byte)		
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 18: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be changed in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

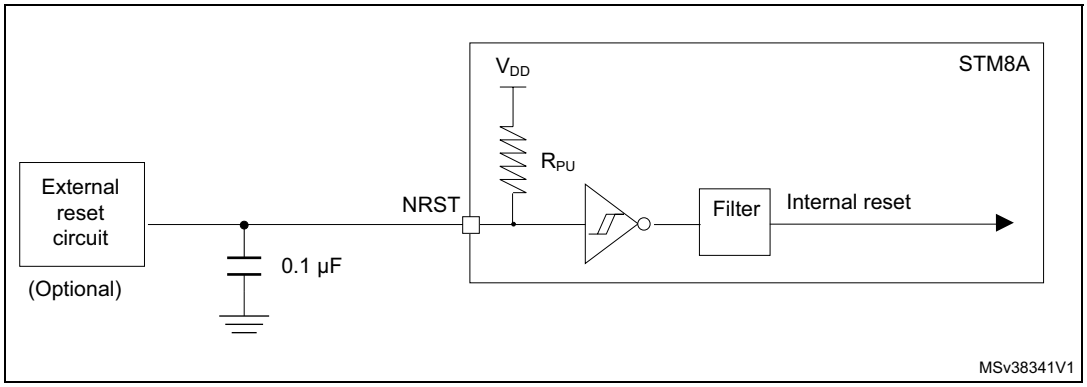
Table 18. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0x00
0x00 4801	User boot code (UBC)	OPT1	UBC[7:0]								0x00
0x00 4802		NOPT1	NUBC[7:0]								0xFF
0x00 4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x00 4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x00 4805	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	0x00
0x00 4806		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	0xFF
0x00 4807	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	0x00
0x00 4808		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	0xFF
0x00 4809	HSE clock startup	OPT5	HSECNT[7:0]								0x00
0x00 480A		NOPT5	NHSECNT[7:0]								0xFF

Table 19. Option byte description (continued)

Option byte no.	Description
OPT12	**TMU_KEY 5 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	**TMU_KEY 6 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	**TMU_KEY 7 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	**TMU_KEY 8 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	**BL[7:0]: Bootloader enable** If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

Figure 39. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 electrical specifications

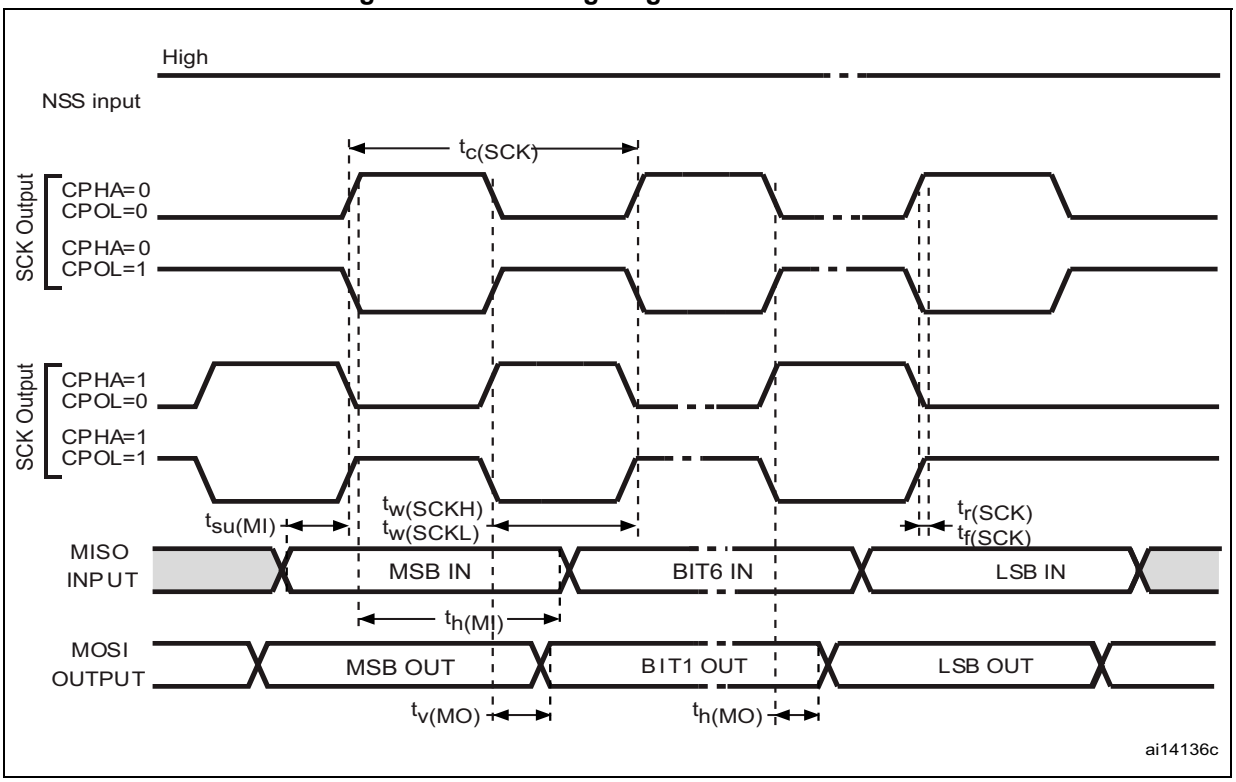
Subject to general operating conditions for V_{DD}, f_{MASTER} and T_A.

Table 40. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	24	MHz

1. Not tested in production.

Figure 42. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.10 I²C interface characteristics

Table 42. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} 3 V to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} 3 V to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- ***ESD***: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- ***FTB***: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

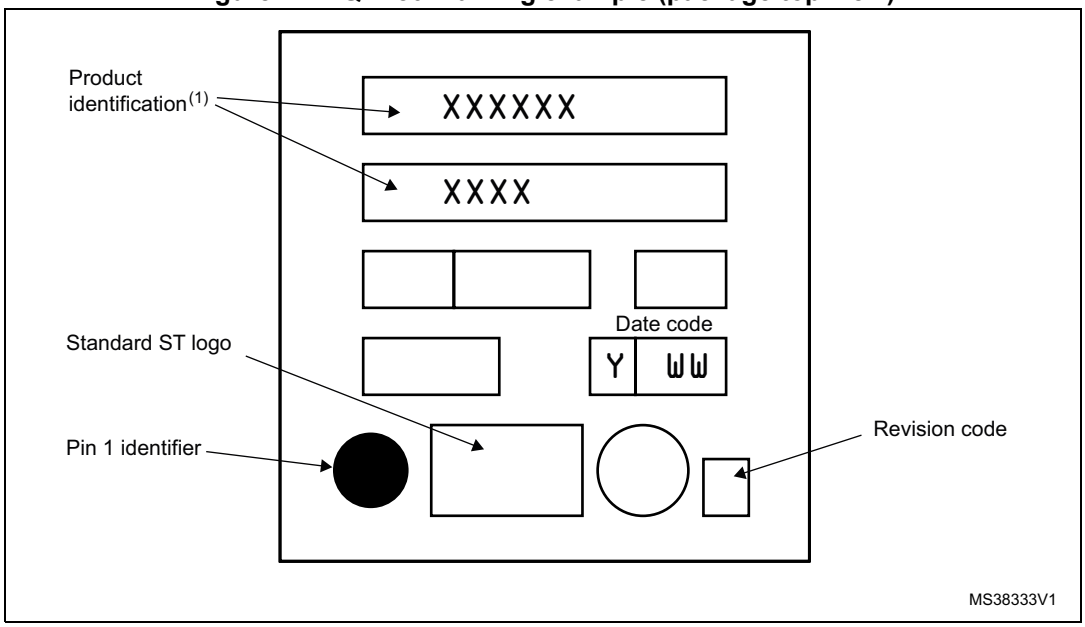
Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

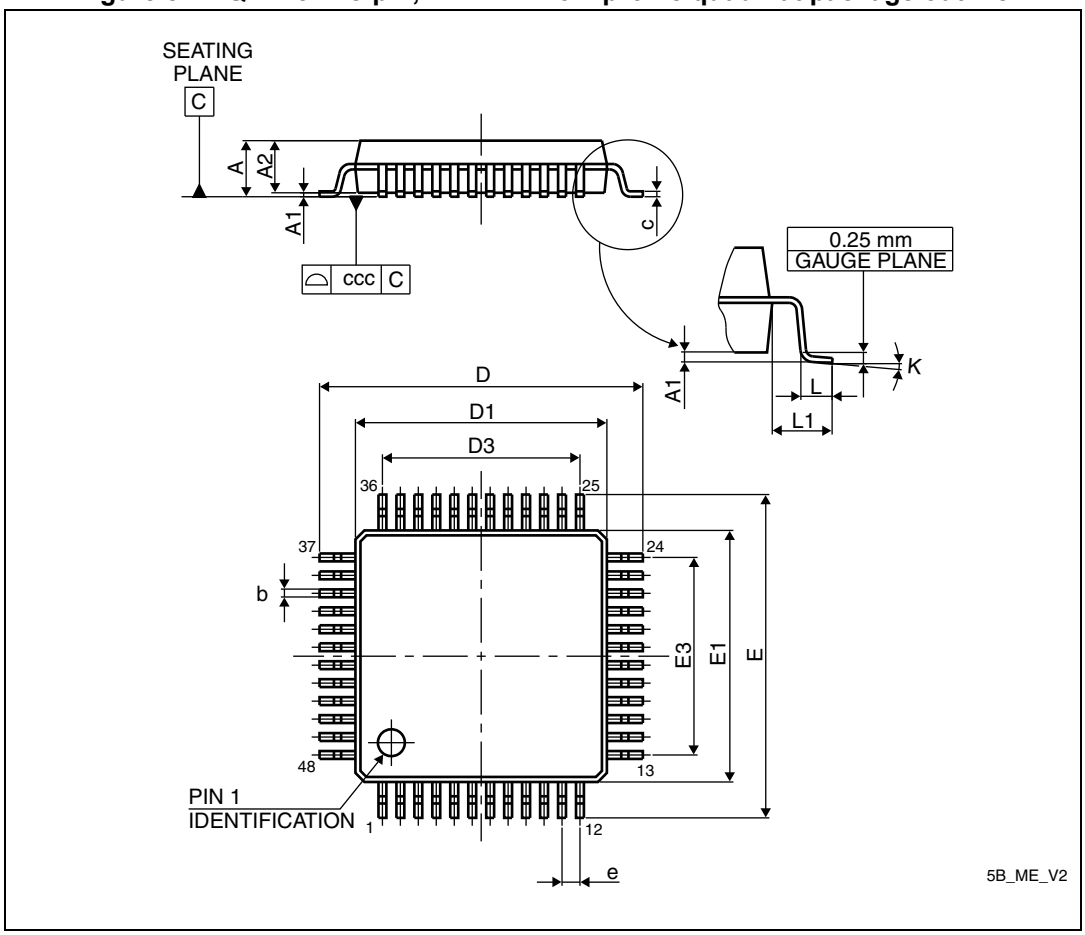
Figure 47. LQFP80 marking example (package top view)



1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

11.3 LQFP48 package information

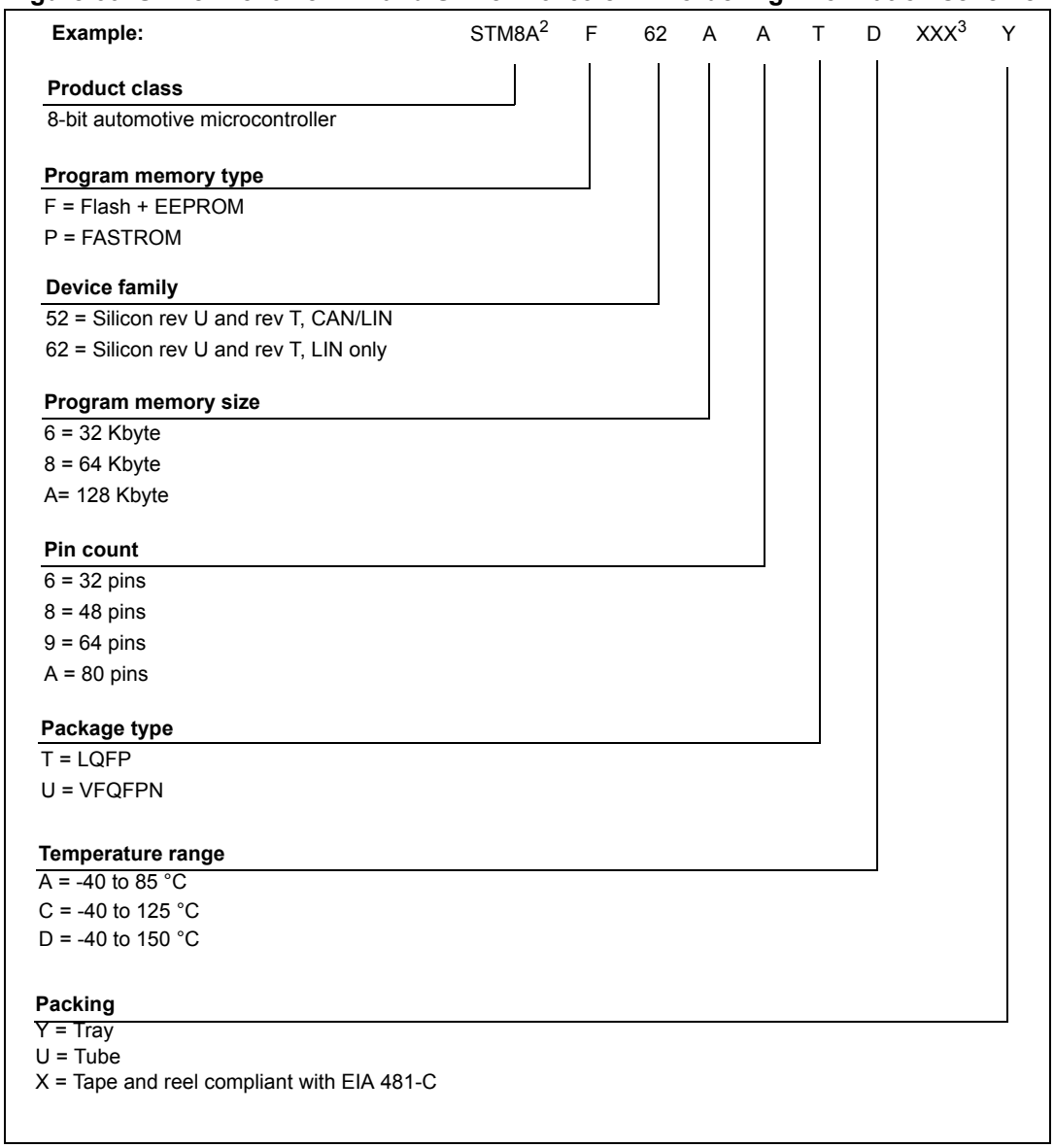
Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

12 Ordering information

Figure 60. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme[1]



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Aug-2008	2 (continued)	*Table 18: Typ. IDD(WFI)HSI vs. VDD @ fCPU = 16 MHz, peripherals = off*: Replaced the source blocks 'simple USART', 'very low-end timer (timer 4)', and 'EEPROM' with 'LINUART', 'timer4' and 'reserved' respectively, added TMU registers. *Table 20: HSE oscillator circuit diagram*: Updated OPT6 and NOPT6, added OPT7 to 17 (TMU, BL) *Table 21: Typical HSI frequency vs VDD*: Updated OPT1 UBC[7:0], OPT4 CKAWUSEL, OPT4 PRSC [1:0], and OPT6, added OPT7 to 16 (TMU). *Table 23: Operating lifetime:* Amended footnotes. *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C:* Added parameter 'voltage and current operating conditions'. *Table 27: Total current consumption in Halt and Active-halt modes. General conditions for VDD applied. TA = -40 °C to 55 °C unless otherwise stated*: Amended footnotes. *Table 28: Oscillator current consumption*: Replaced. *Table 29: Programming current consumption*: Amended maximum data and footnotes. *Table 21: Current characteristics*: Replaced. *Table 22: Thermal characteristics:* Added and amended $I_{DD(RUN)}$ data; amended $I_{DD(WFI)}$ data; amended footnotes. *Table 32: HSE oscillator characteristics*: Filled in, amended maximum data and footnotes. *Figure 13* to *Figure 18*: info on peripheral activity added. *Table 33: HSI oscillator characteristics*: Modified f_{HSE_ext} data and added V_{HSEdhl} data. *Table 35: Flash program memory/data EEPROM memory*: Removed ACC_{HSI} parameters and replaced with ACC_{HS} parameters; amended data and footnotes. Amended data of '*RAM and hardware registers*' table. *Table 37: Data memory*: Updated names and data of N_{RW} and t_{RET} parameters. *Table 40: TIM 1, 2, 3, and 4 electrical specifications*: Added V_{OH} and V_{OL} parameters; Updated $I_{lkg\ ana}$ parameter. Removed: *Output driving current (standard ports), Output driving current (true open drain ports)*, and *Output driving current (high sink ports)*. *Table 46: EMI data*: Updated f_{ADC}, t_S, and t_{CONV} data. *Table: ADC accuracy for VDDA = 3.3 V*: removed the 4-MHz condition from all parameters. *Table 47: ESD absolute maximum ratings*: Removed the 4-MHz condition from all parameters; updated footnote 1 and removed footnote 2. *Table 51: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*: Added data for T_A = 145 °C. *Figure 53*: Updated memory size, pin count and package type information.