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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af62aatay

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

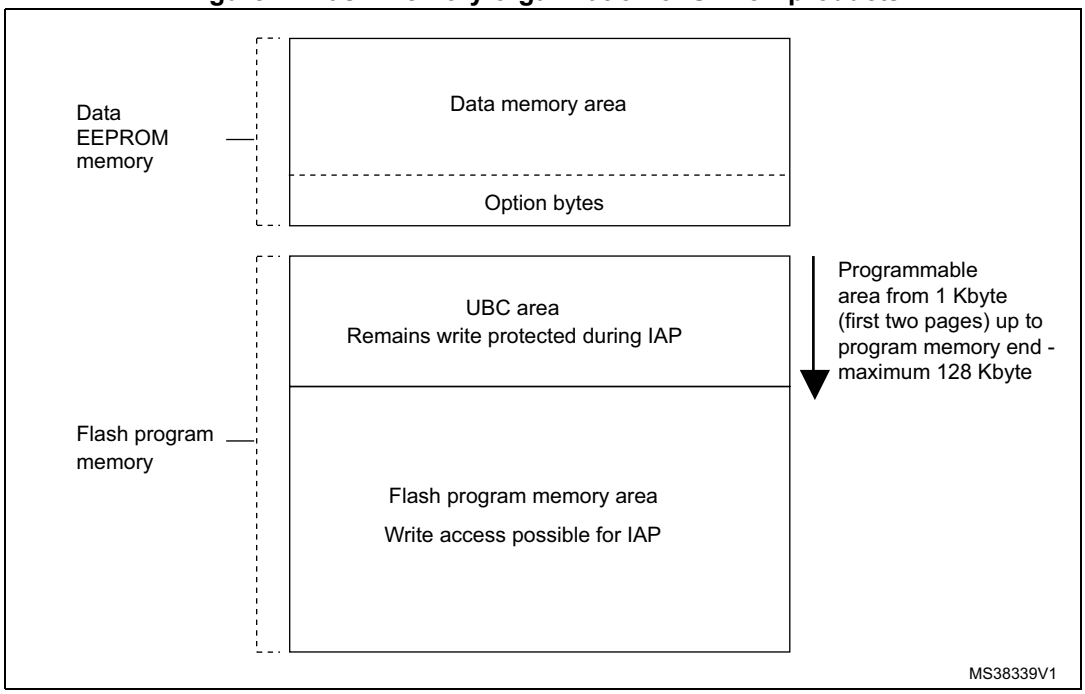
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 54*).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with two trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

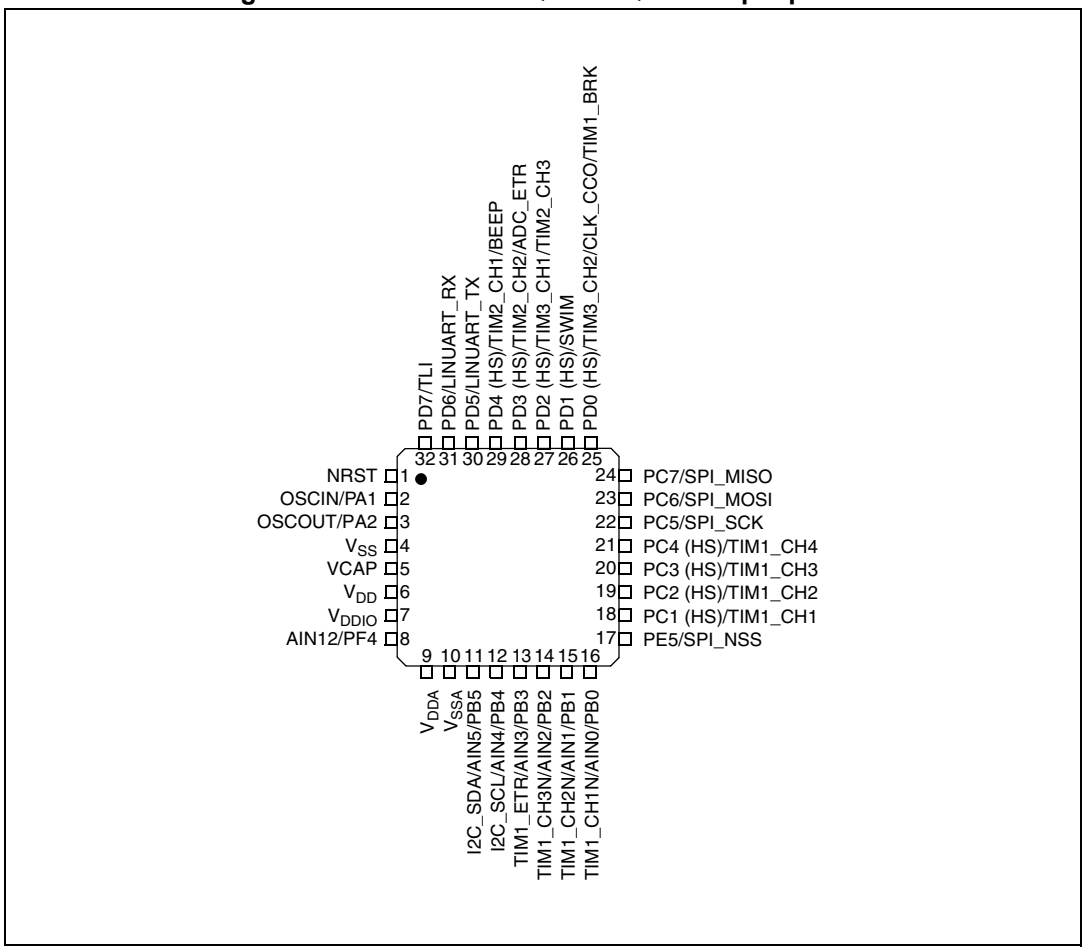
5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

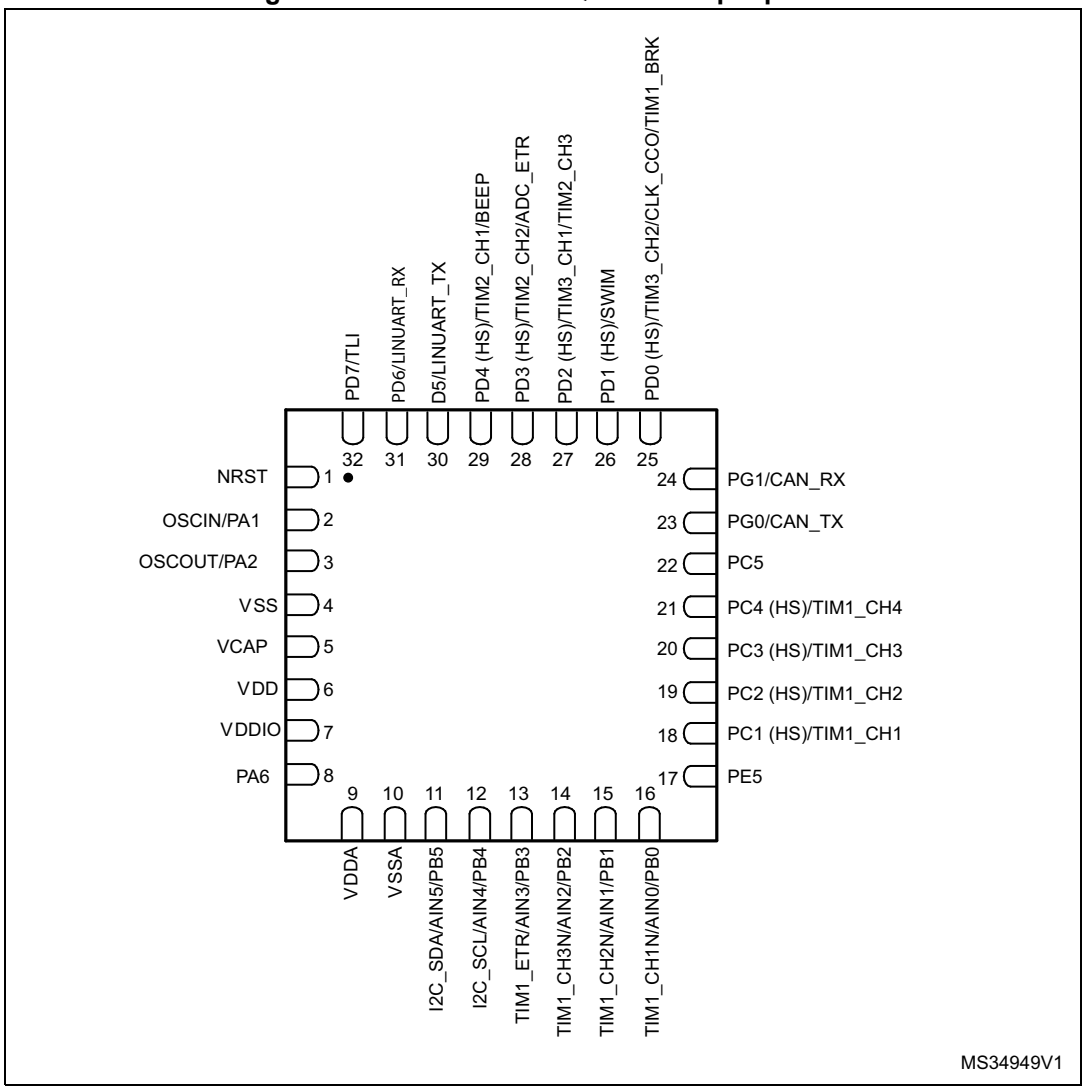
STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout



1. HS stands for high sink capability.

Figure 7. STM8AF52x6 VFQFPN32 32-pin pinout



1. The following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7. As a consequence, they must be put into one of the following configurations by software:
   - configured as input with internal pull-up/down resistor,
   - configured as output push-pull low.
2. HS stands for high sink capability.

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	2	2	2	PA1/OSCIN(1)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/ crystal in	-
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	4	4	-	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	5	5	4	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	6	6	5	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	7	7	6	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	8	8	7	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	10	10	-	-	PA4/USART_RX	I/O	**X**	X	X	-	O3	X	X	**Port A4**	USART receive	-
11	11	11	-	-	PA5/USART_TX	I/O	**X**	X	X	-	O3	X	X	**Port A5**	USART transmit	-
12	12	12	-	8	PA6/USART_CK (2)	I/O	**X**	X	X	-	O3	X	X	**Port A6**	USART synchro nous clock	-
13	-	-	-	-	PH0	I/O	X	X	-	HS	O3	X	X	**Port H0**	-	-
14	-	-	-	-	PH1	I/O	**X**	X	-	HS	O3	X	X	**Port H1**	-	-
15	-	-	-	-	PH2	I/O	**X**	X	-	-	O1	X	X	**Port H2**	-	-
16	-	-	-	-	PH3	I/O	**X**	X	-	-	O1	X	X	**Port H3**	-	-
17	13	-	-	-	PF7/AIN15	I/O	**X**	X	-	-	O1	X	X	**Port F7**	Analog input 15	-
18	14	-	-	-	PF6/AIN14	I/O	**X**	X	-	-	O1	X	X	**Port F6**	Analog input 14	-
19	15	-	-	-	PF5/AIN13	I/O	**X**	X	-	-	O1	X	X	**Port F5**	Analog input 13	-
20	16	-	8	-	PF4/AIN12	I/O	**X**	X	-	-	O1	X	X	**Port F4**	Analog input 12	-
21	17	-	-	-	PF3/AIN11	I/O	**X**	X	-	-	O1	X	X	**Port F3**	Analog input 11	-

Table 11. STM8AF526x/8x/Ax and STM8AF6269/8x/Ax pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	STM8AF62xx LQFP32/VFQFPN32	STM8AF52x6 VFQFPN32			Floating	Wpu	Ext. interrupt	High sink	Speed	OD	PP			
22	18	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC positive reference voltage		-
23	19	13	9	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
24	20	14	10	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
25	21	-	-	-	V_{REF-}	S	-	-	-	-	-	-	-	ADC negative reference voltage		-
26	22	-	-	-	PF0/AIN10	I/O	**X**	X	-	-	O1	X	X	**Port F0**	Analog input 10	-
27	23	15	-	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
28	24	16	-	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
29	25	17	11	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_CH3N [AFR5]
33	29	21	15	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_CH2N [AFR5]
34	30	22	16	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X	-	-	O1	X	X	**Port H4**	Timer 1 - trigger input	-
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X	-	-	O1	X	X	**Port H5**	Timer 1 - inverted channel 3	-
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X	-	-	O1	X	X	**Port H6**	Timer 1 - inverted channel 2	-

Table 13. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX(1)
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX(1)
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX(1)
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

1. Depends on the external circuitry.

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		Reserved area (1 byte)		
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			

Table 14. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART	UART1_SR	USART status register	0xC0
0x00 5231		UART1_DR	USART data register	0xXX
0x00 5232		UART1_BRR1	USART baud rate register 1	0x00
0x00 5233		UART1_BRR2	USART baud rate register 2	0x00
0x00 5234		UART1_CR1	USART control register 1	0x00
0x00 5235		UART1_CR2	USART control register 2	0x00
0x00 5236		UART1_CR3	USART control register 3	0x00
0x00 5237		UART1_CR4	USART control register 4	0x00
0x00 5238		UART1_CR5	USART control register 5	0x00
0x00 5239		UART1_GTR	USART guard time register	0x00
0x00 523A		UART1_PSCR	USART prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	LINUART	UART3_SR	LINUART status register	0xC0
0x00 5241		UART3_DR	LINUART data register	0xXX
0x00 5242		UART3_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART3_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART3_CR1	LINUART control register 1	0x00
0x00 5245		UART3_CR2	LINUART control register 2	0x00
0x00 5246		UART3_CR3	LINUART control register 3	0x00
0x00 5247		UART3_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 27. Total current consumption in Halt and Active-halt modes. General conditions for V_{DD} applied. T_A = -40 °C to 55 °C unless otherwise stated

Symbol	Parameter	Conditions			Typ	Max	Unit
		Main voltage regulator (MVR)(1)	Flash mode(2)	Clock source and temperature condition			
$I_{DD(H)}$	Supply current in Halt mode	Off	Power-down	Clocks stopped	5	35(3)	µA
				Clocks stopped, T_A = 25 °C	5	25	
$I_{DD(AH)}$	Supply current in Active-halt mode with regulator on	On	Power-down	External clock 16 MHz f_{MASTER} = 125 kHz	770	900(3)	
				LSI clock 128 kHz	150	230(3)	
	Supply current in Active-halt mode with regulator off	Off	Power-down	LSI clock 128 kHz	25	42(3)	
				LSI clock 128 kHz, T_A = 25 °C	25	30	
$t_{WU(AH)}$	Wakeup time from Active-halt mode with regulator on	On	Operating mode	T_A = -40 to 150 °C	10	30(3)	µs
	Wakeup time from Active-halt mode with regulator off	Off			50	80(3)	

1. Configured by the REGAH bit in the CLK_ICKR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.
3. Guaranteed by characterization results, not tested in production.

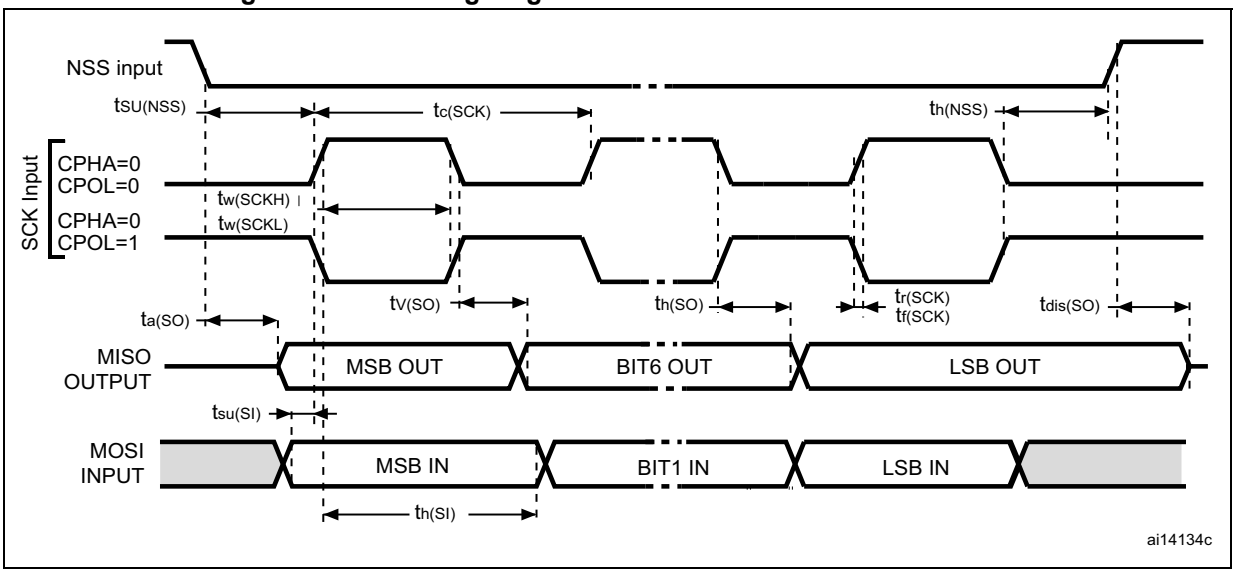
Current consumption for on-chip peripherals

Table 28. Oscillator current consumption

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 5 V	f_{OSC} = 24 MHz	1	2.0(3)	mA
			f_{OSC} = 16 MHz	0.6	-	
			f_{OSC} = 8 MHz	0.57	-	
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 3.3 V	f_{OSC} = 24 MHz	0.5	1.0(3)	
			f_{OSC} = 16 MHz	0.25	-	
			f_{OSC} = 8 MHz	0.18	-	

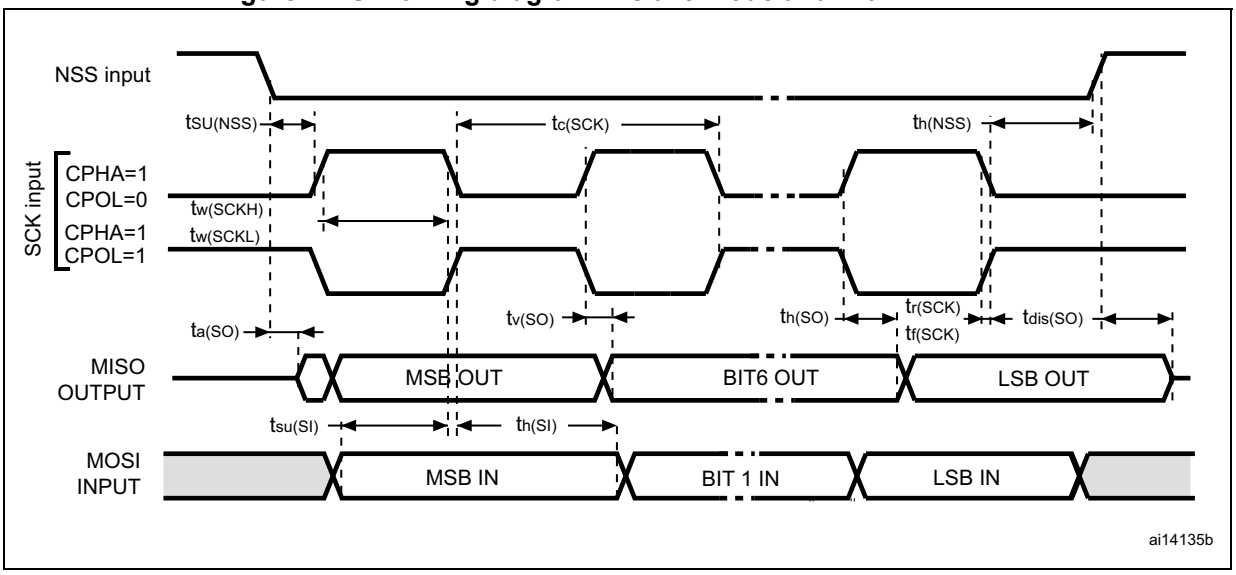
1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Informative data.

Figure 40. SPI timing diagram in slave mode and with CPHA = 0



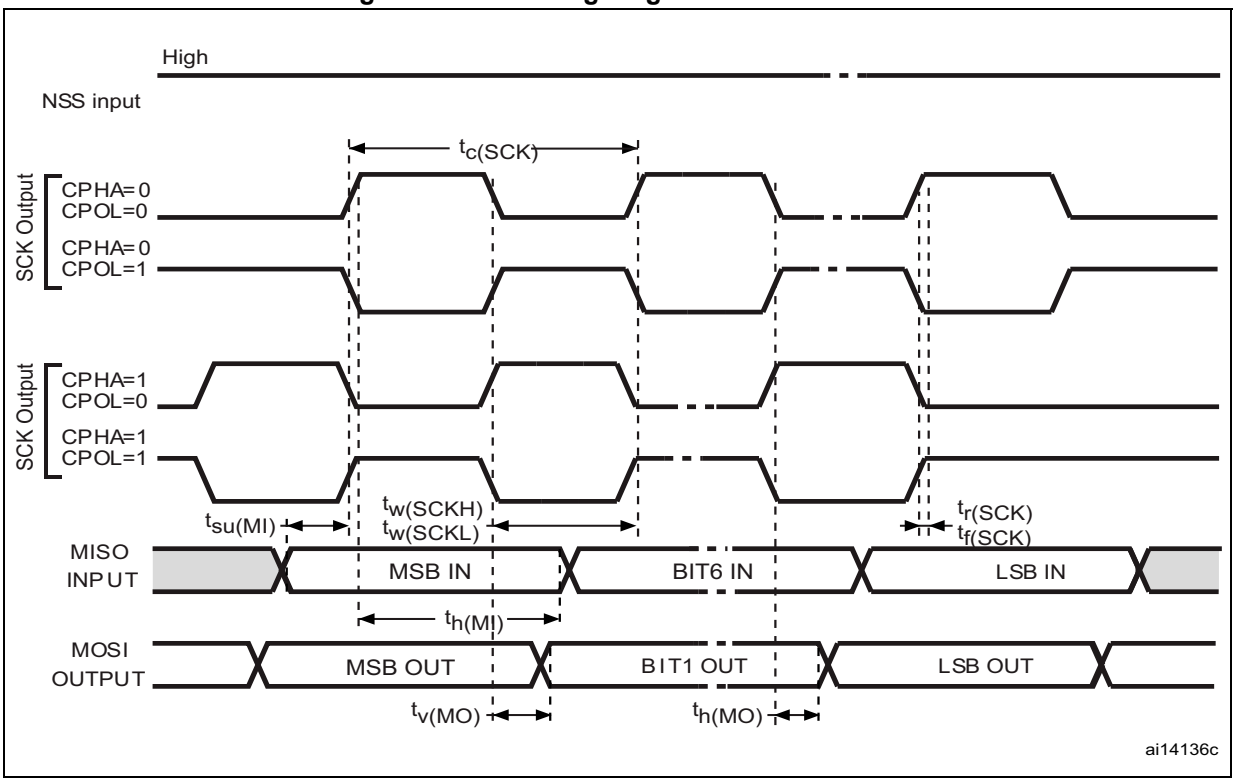
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram in slave mode and with CPHA = 1



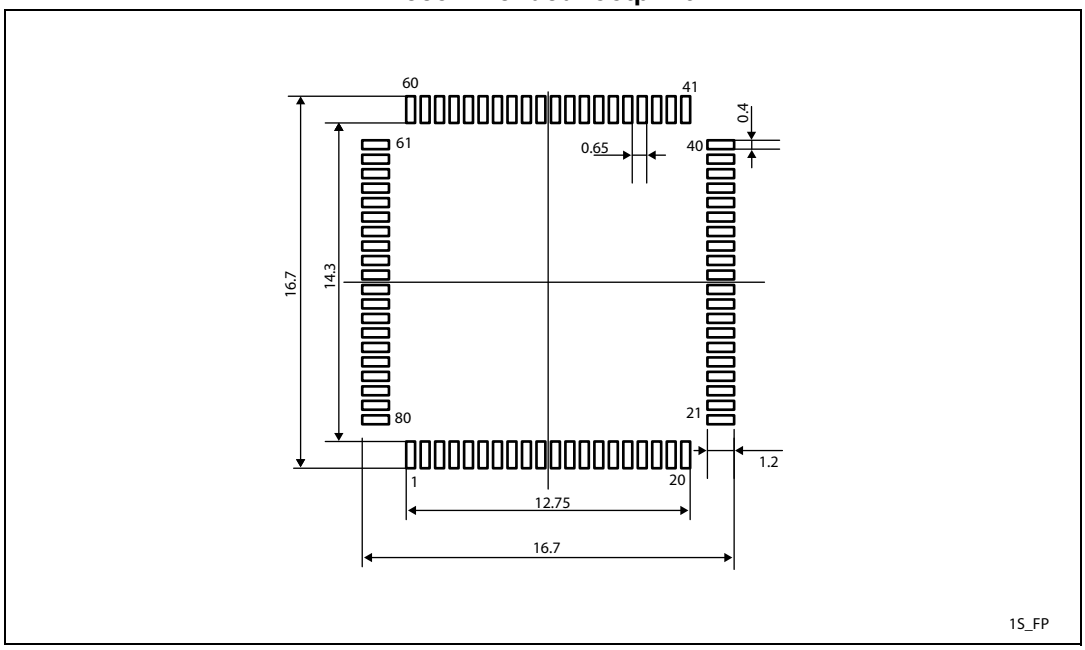
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 42. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

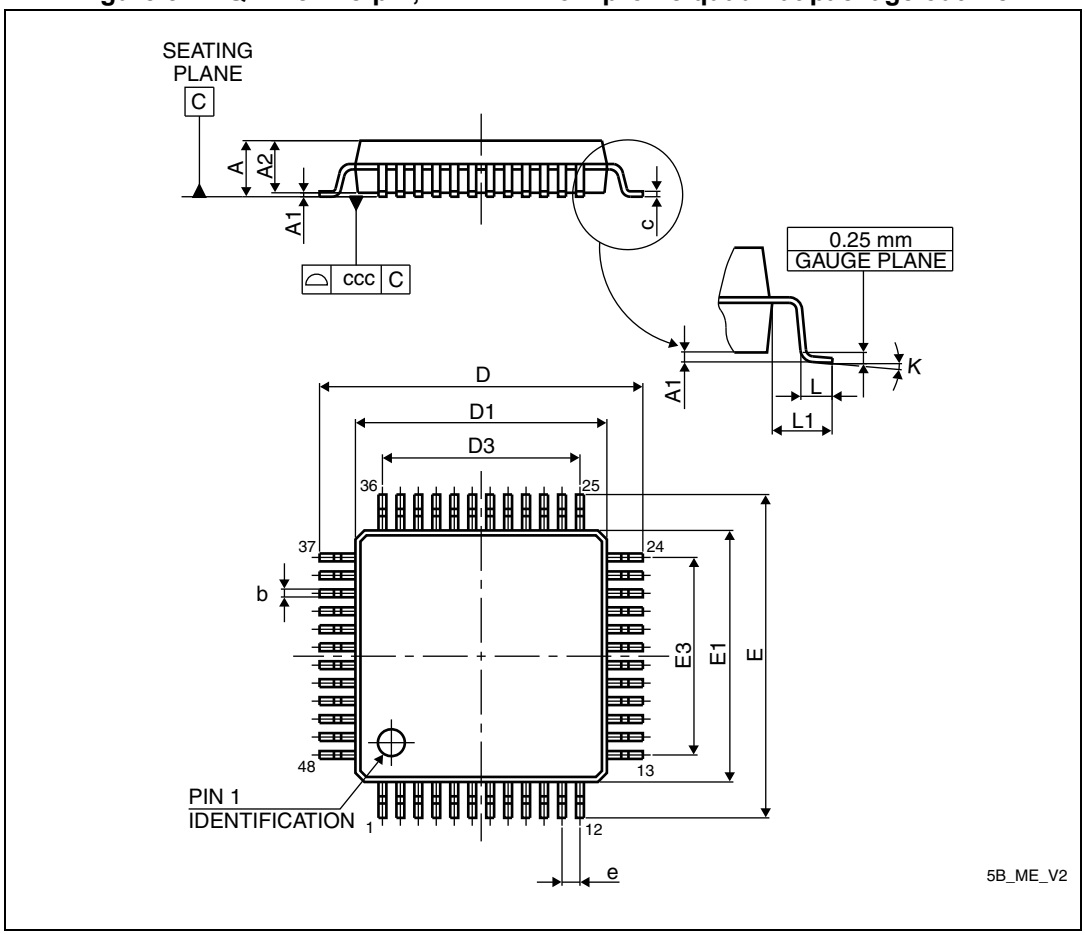
Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

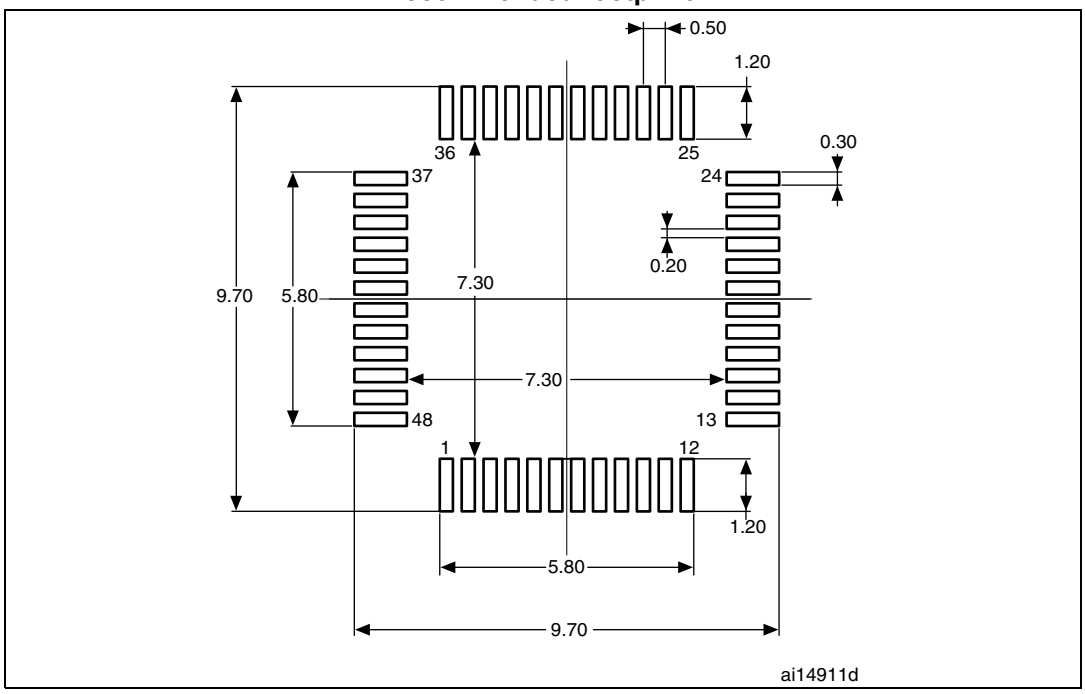
11.3 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



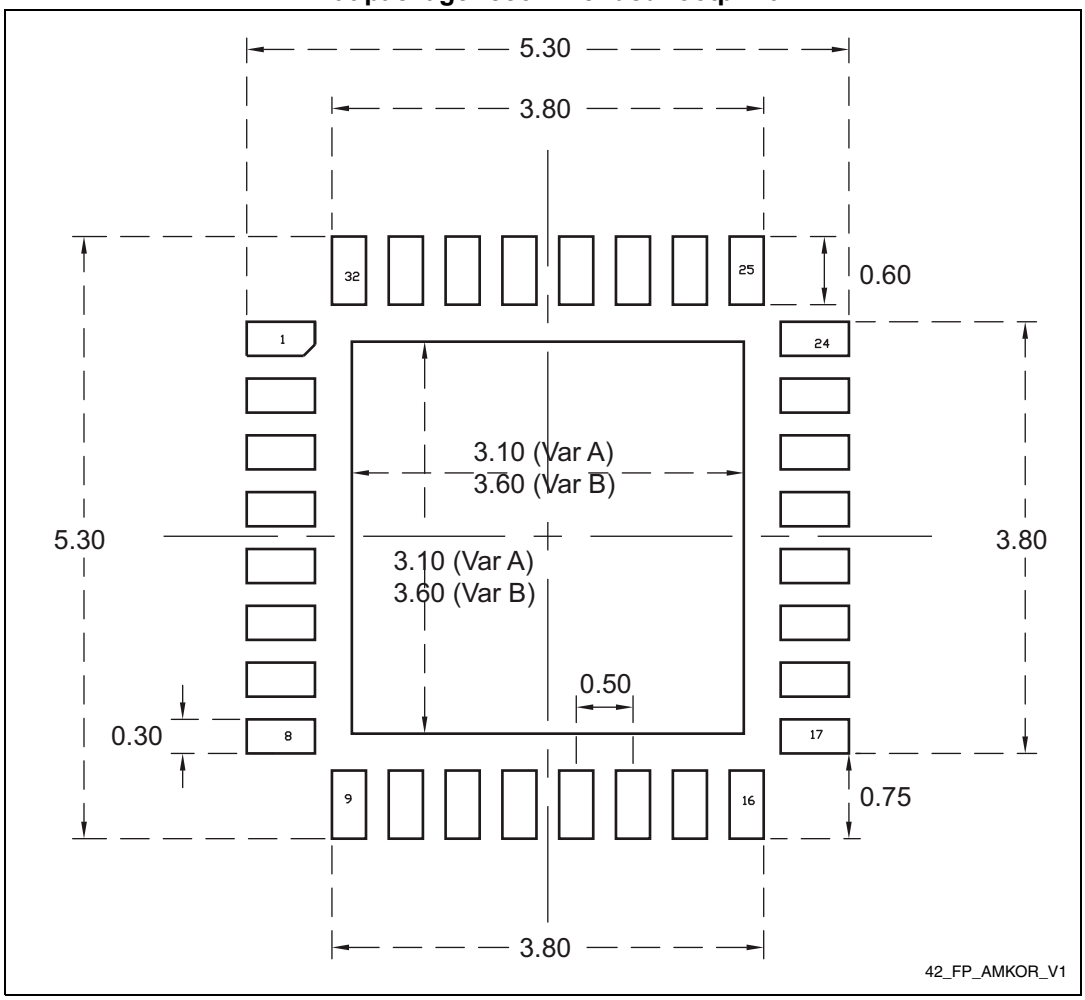
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1 on page 111*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2)
- I_{DDmax} = 8 mA
- V_{DD} = 5 V
- maximum 20 I/Os used at the same time in output at low-level with I_{OL} = 8 mA
- V_{OL} = 0.4 V

P_{INTmax} = 8 mA x 5 V = 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives:

P_{INTmax} = 400 mW and P_{IOmax} 64 mW

P_{Dmax} = 400 mW + 64 mW

Thus:

P_{Dmax} = 464 mW.

Using the values obtained in *Table 54: Thermal characteristics* T_{Jmax} is calculated as follows:

For LQFP64 46 °C/W

$$T_{jmax} = 82\ °C + (46\ °C/W \times 464\ mW) = 82\ °C + 21\ °C = 103\ °C$$

This is within the range of the suffix C version parts (-40 °C < T_j < 125 ° C).

Parts must be ordered at least with the temperature range suffix C.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Jan-2011	8 (continued)	Removed note 1 in *Table 24: General operating conditions* and note 1 below *Figure 11: fCPUmax versus VDD*. Removed note 3 in *Table 26: Total current consumption in Run, Wait and Slow mode. General conditions for VDD apply, TA = -40 °C to 150 °C*. Removed note 2 in *Table 31: HSE external clock characteristics* and *Table 35: Flash program memory/data EEPROM memory* Removed note 1 in *Table 37: Data memory*. Modified T_{WE} maximum value in *Table 36: Flash program memory* and *Table 37: Data memory*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table 39: NRST pin characteristics*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 39: Recommended reset pin protection,* and updated external capacitor value. Updated *Note 1* in *Table 40: TIM 1, 2, 3, and 4 electrical specifications.* Updated *Note 1* in *Table 41: SPI characteristics.* Moved know limitations to separate errata sheet. Added “not recommended for new design” note to device family 51, memory size 7 and 9, and temperature range B, in *Figure 60: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax ordering information scheme1*. Added Raisonance compiler in *Section 13.2: Software tools.*
18-Jul-2012	9	Updated wildcards of document part numbers. Added VFQFPN package. Added STM8AF62A6 part number. *Table 1: Device summary* updated footnote *1* and added footnote *2*. *Table: STM8AF52xx product line-up with CAN* and *Table: STM8AF62xx product line-up without CAN*: added “P” version for all order codes; updated size of data EEPROM for 64K devices to 2K instead of 1.5K; updated RAM. *Figure 1: STM8AF526x/8x/Ax and STM8AF6269/8x/Ax block diagram*: updated POR, BOR and WDG; removed PDR; added legend. *Section 5.4: Flash program and data EEPROM*: removed non relevant bullet points and added a sentence about the factory program. Added *Table 4: Peripheral clock gating bits (CLK_PCKENR1)* and updated *Table 5: Peripheral clock gating bits (CLK_PCKENR2)* *Section : ADC features*: updated ADC input range. *Table 12: Memory model 128K:* updated RAM size, RAM end addresses, and stack roll-over addresses; updated footnote *1* *Table 18: Option bytes:* updated factory default setting for NOPT17; updated footnotes. *Table 20: Voltage characteristics:* updated V_{DDX} - V_{DD} to V_{DDX} - V_{SS}. *Table 24: General operating conditions:* updated V_{CAP}.